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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

August 2016

FDP12N50NZ / FDPF12N50NZ
N-Channel UniFET^{TM} II MOSFET
500 V, 11.5 A, 520 mΩ

Features

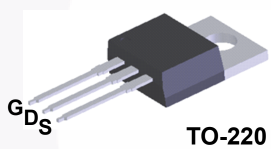
- $R_{DS(on)}$ = 460 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 5.75 A
- Low Gate Charge (Typ. 23 nC)
- Low C_{rss} (Typ. 14 pF)
- 100% Avalanche Tested
- ESD Improved Capability
- RoHS Compliant

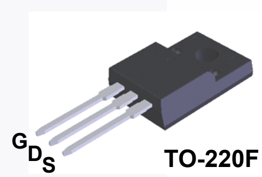
Applications

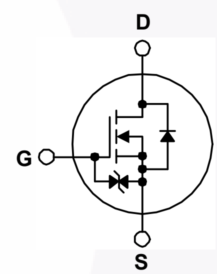
- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

Description

UniFET^{TM} II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.







MOSFET Maximum Ratings T_C = 25^{o}C unless otherwise noted.

Symbol	Parameter			FDP12N50NZ	FDPF12N50NZ	Unit
V_{DSS}	Drain to Source Voltage			500		V
V_{GSS}	Gate to Source Voltage			±25		V
I_D	Drain Current	- Continuous (T_C = 25^{o}C)		11.5	11.5*	A
		- Continuous (T_C = 100^{o}C)		6.9	6.9*	
I_{DM}	Drain Current	- Pulsed	(Note 1)	46	46*	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	560		mJ
I_{AR}	Avalanche Current		(Note 1)	11.5		A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	17		mJ
dv/dt	MOSFET dv/dt Ruggedness			20		V/ns
	Peak Diode Recovery dv/dt		(Note 3)	10		V/ns
P_D	Power Dissipation	(T_C = 25^{o}C)		170	42	W
		- Derate above 25^{o}C		1.37	0.33	W/^{o}C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150		^{o}C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds			300		^{o}C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP12N50NZ	FDPF12N50NZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.73	3.0	^{o}C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP12N50NZ	FDP12N50NZ	TO-220	Tube	N/A	50 units
FDPF12N50NZ	FDPF12N50NZ	TO-220F	Tube	N/A	50 units

Electrical Characteristics T_C = 25^{o}C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, T_J = 25^{o}C	500	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25^{o}C	-	0.5	-	V/^{o}C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 400V, T_C = 125^{o}C	-	-	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±25V, V_{DS} = 0V	-	-	±10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 5.75A	-	0.46	0.52	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 5.75A	-	12	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V f = 1MHz	-	945	1235	pF
C_{oss}	Output Capacitance		-	155	205	pF
C_{rss}	Reverse Transfer Capacitance		-	14	20	pF
Q_g	Total Gate Charge at 10V	V_{DS} = 400V, I_D = 11.5A V_{GS} = 10V (Note 4)	-	23	30	nC
Q_{gs}	Gate to Source Gate Charge		-	5.5	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	9.6	-	nC

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 11.5A R_G = 25Ω (Note 4)	-	20	50	ns
t_r	Turn-On Rise Time		-	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		-	60	130	ns
t_f	Turn-Off Fall Time		-	45	100	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	11.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	46	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 11.5A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 11.5A dI_F/dt = 100A/μs	-	315	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.0	-	μC

Notes:
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 8.5mH, I_{AS} = 11.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. I_{SD} ≤ 11.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

Figure 1. On-Region Characteristics

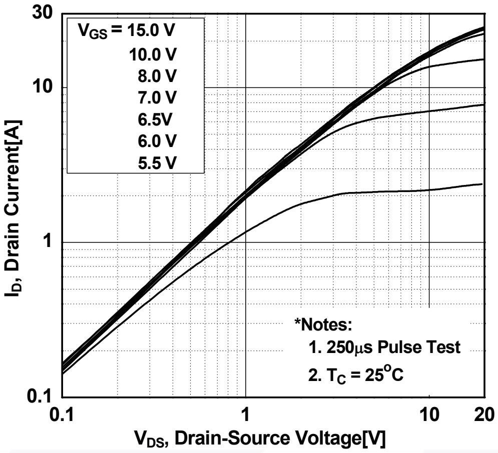


Figure 2. Transfer Characteristics

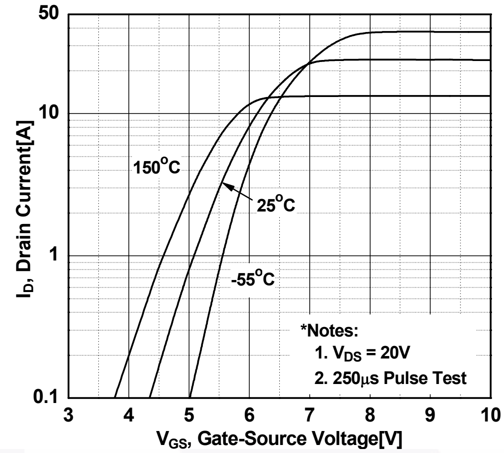


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

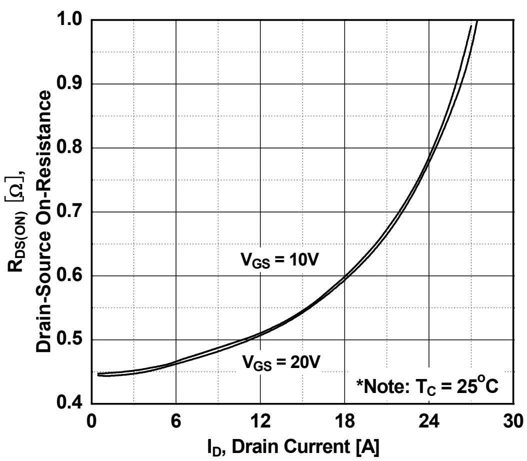


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

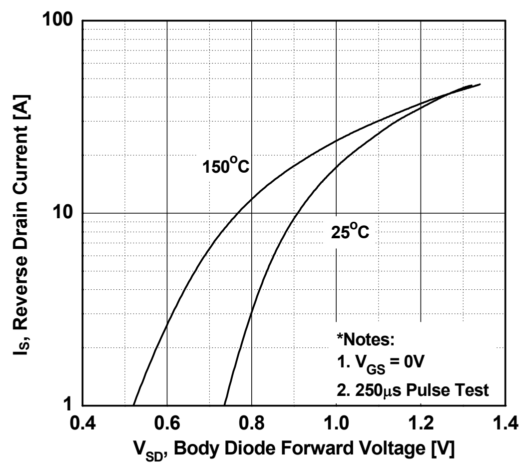


Figure 5. Capacitance Characteristics

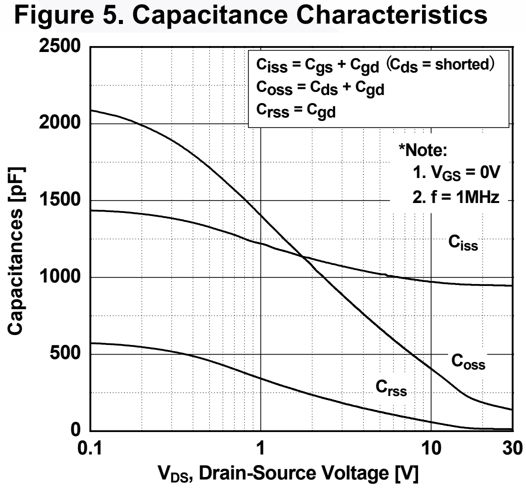
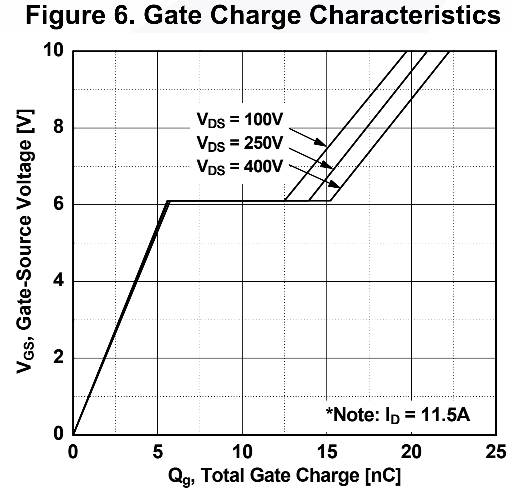


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

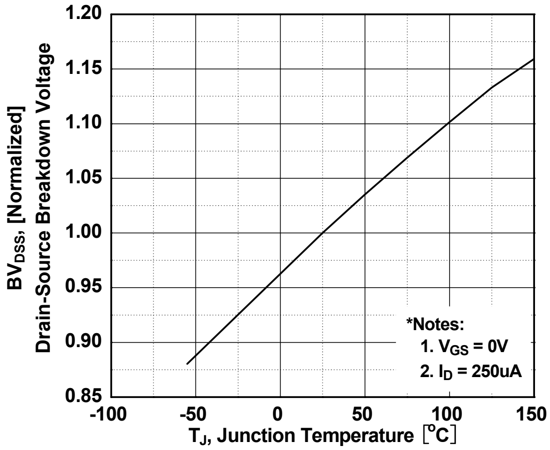


Figure 8. On-Resistance Variation vs. Temperature

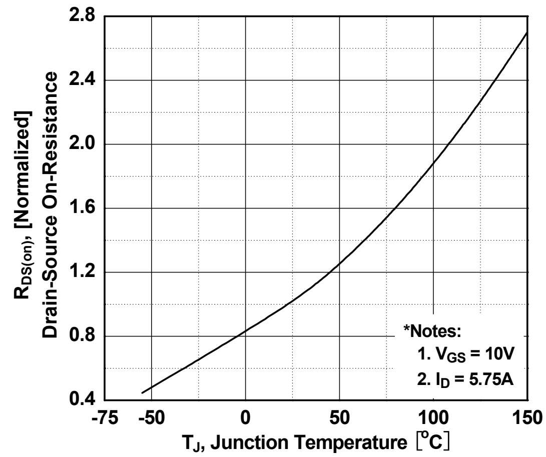


Figure 9. Maximum Safe Operating Area - FDPF12N50NZ

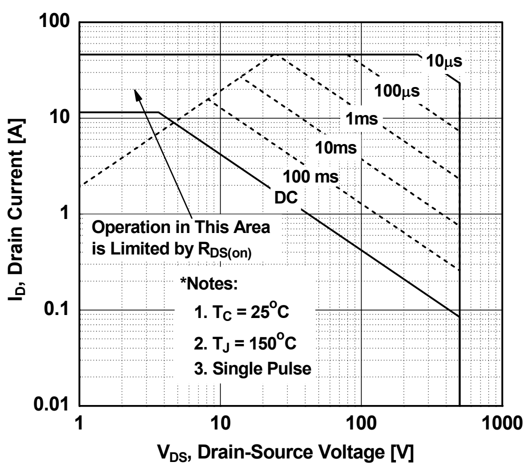


Figure 10.Maximum Safe Operating Area - FDP12N50NZ

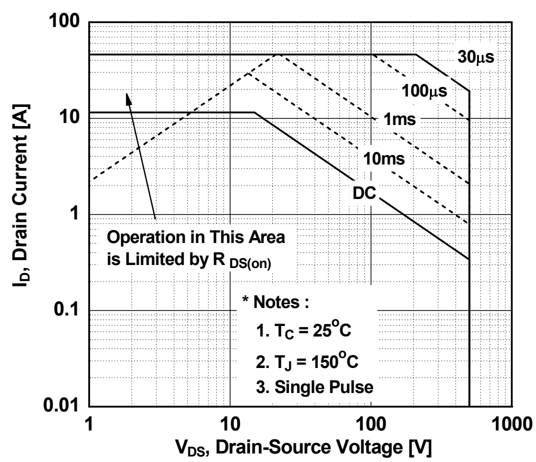
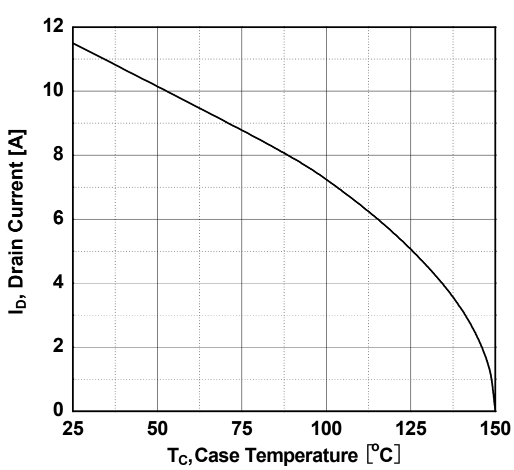


Figure 11. Maximum Drain Current vs. Case Temperature



Typical Characteristics (Continued)

Figure 12. Transient Thermal Response Curve - FDP12N50NZ

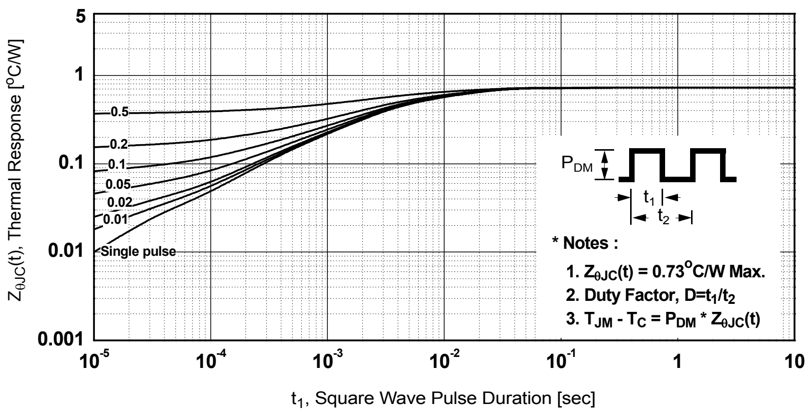


Figure 13. Transient Thermal Response Curve - FDPF12N50NZ

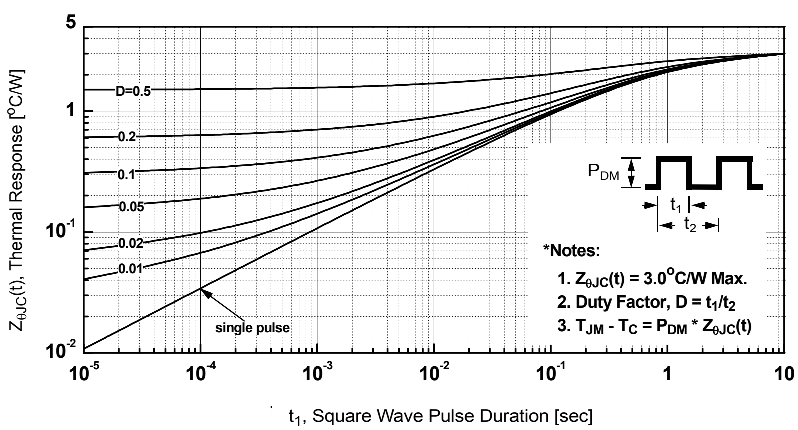


Figure 14. Gate Charge Test Circuit & Waveform

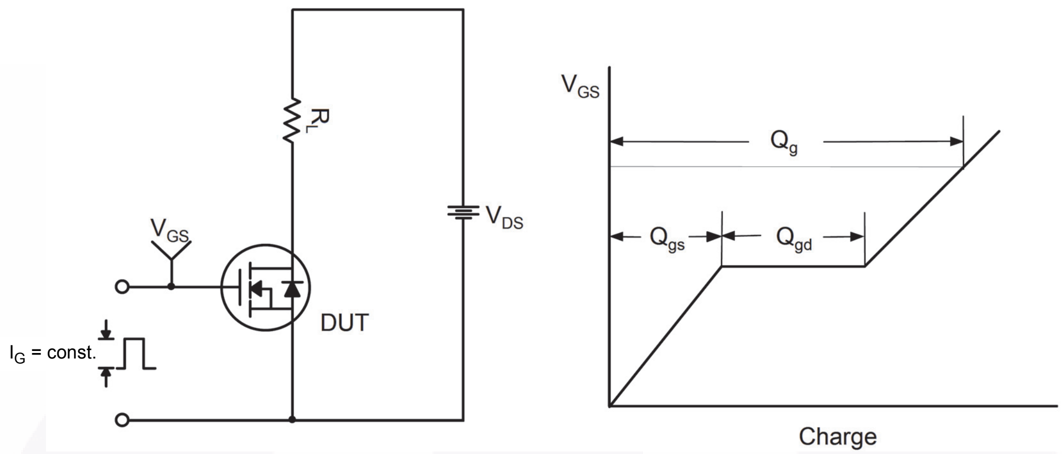


Figure 15. Resistive Switching Test Circuit & Waveforms

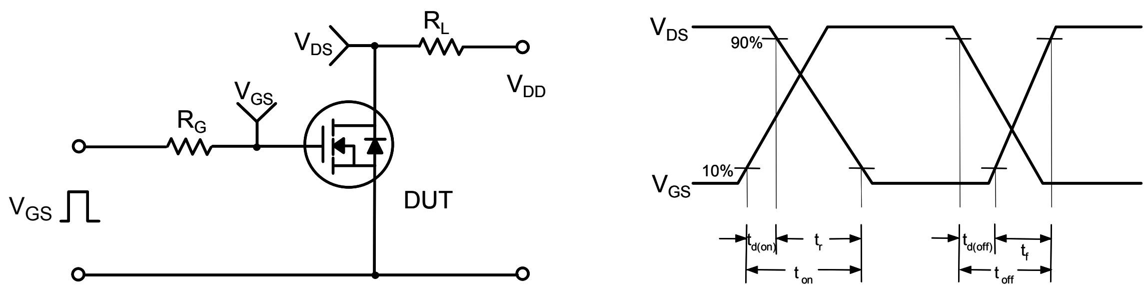


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

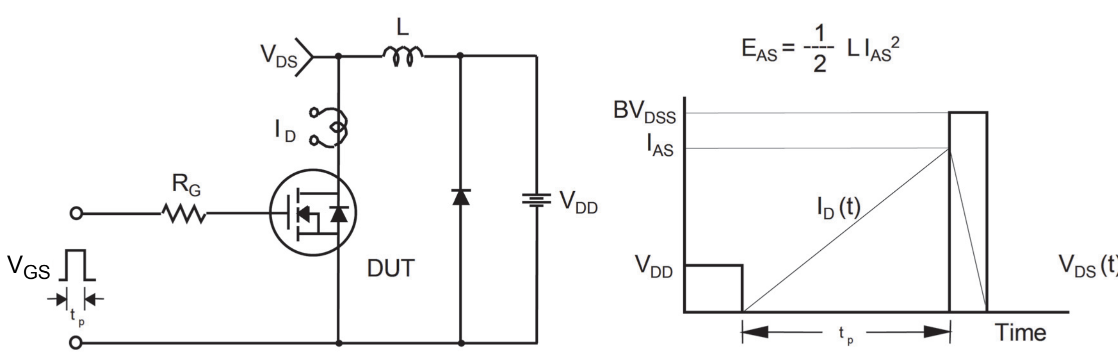
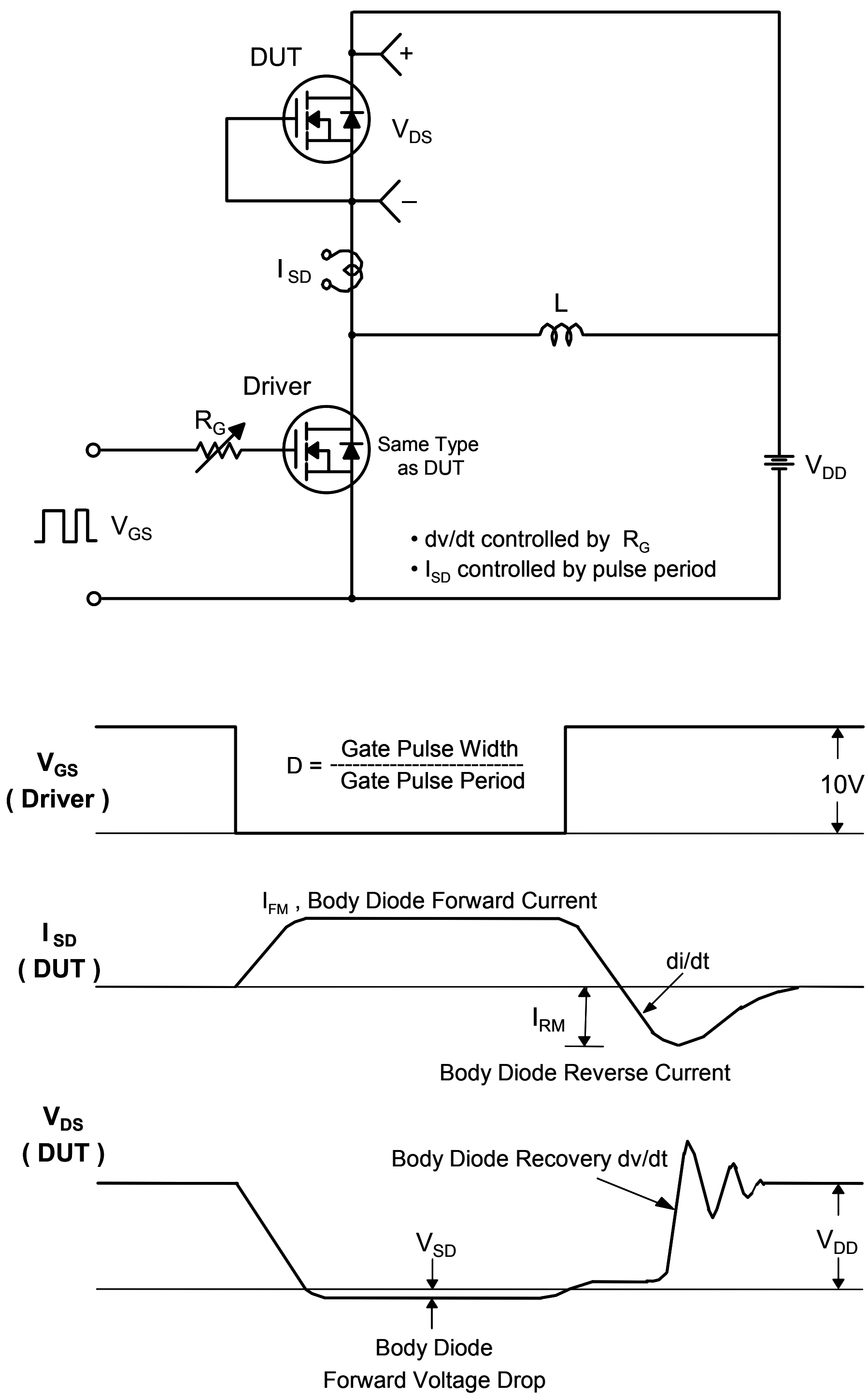
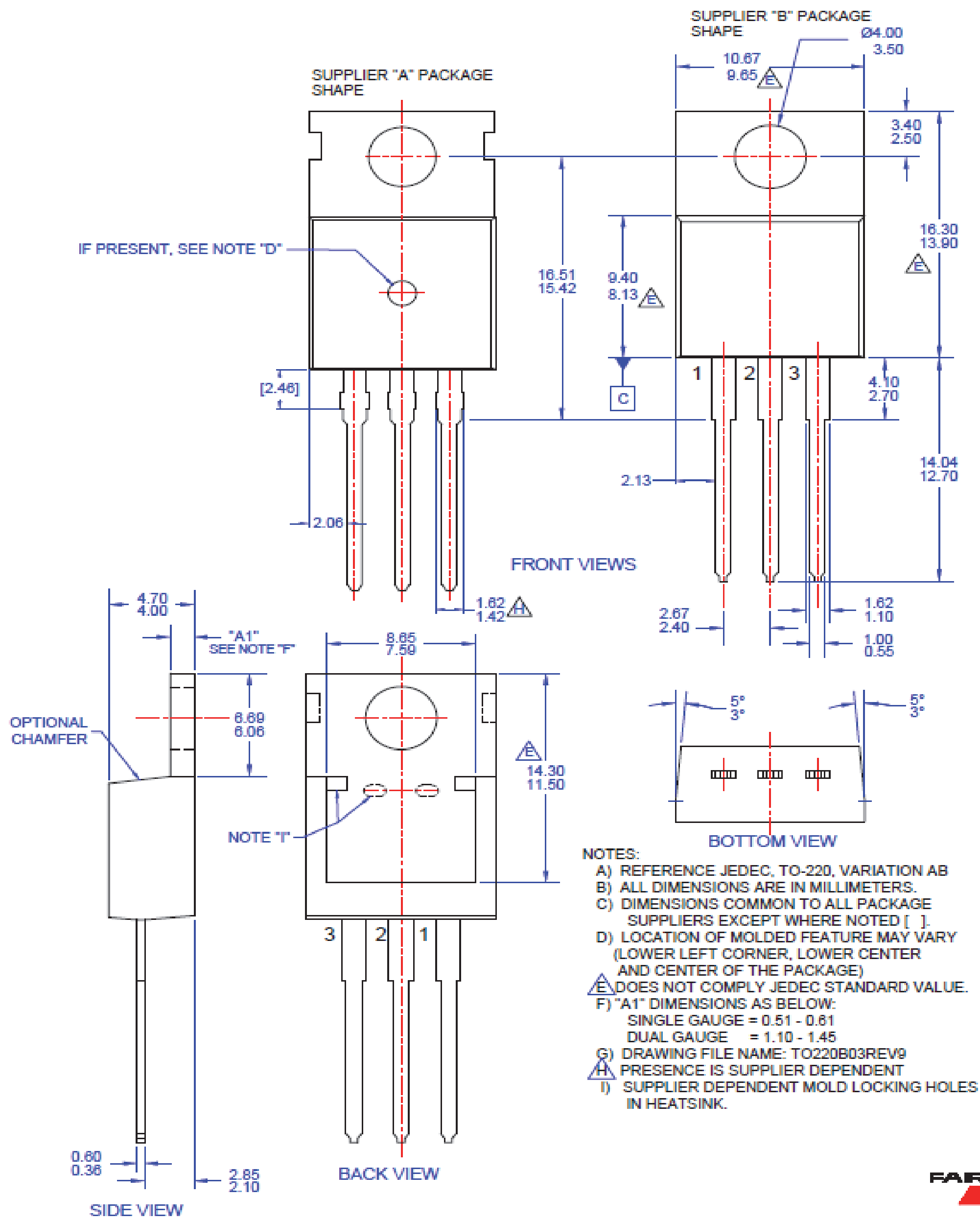


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms



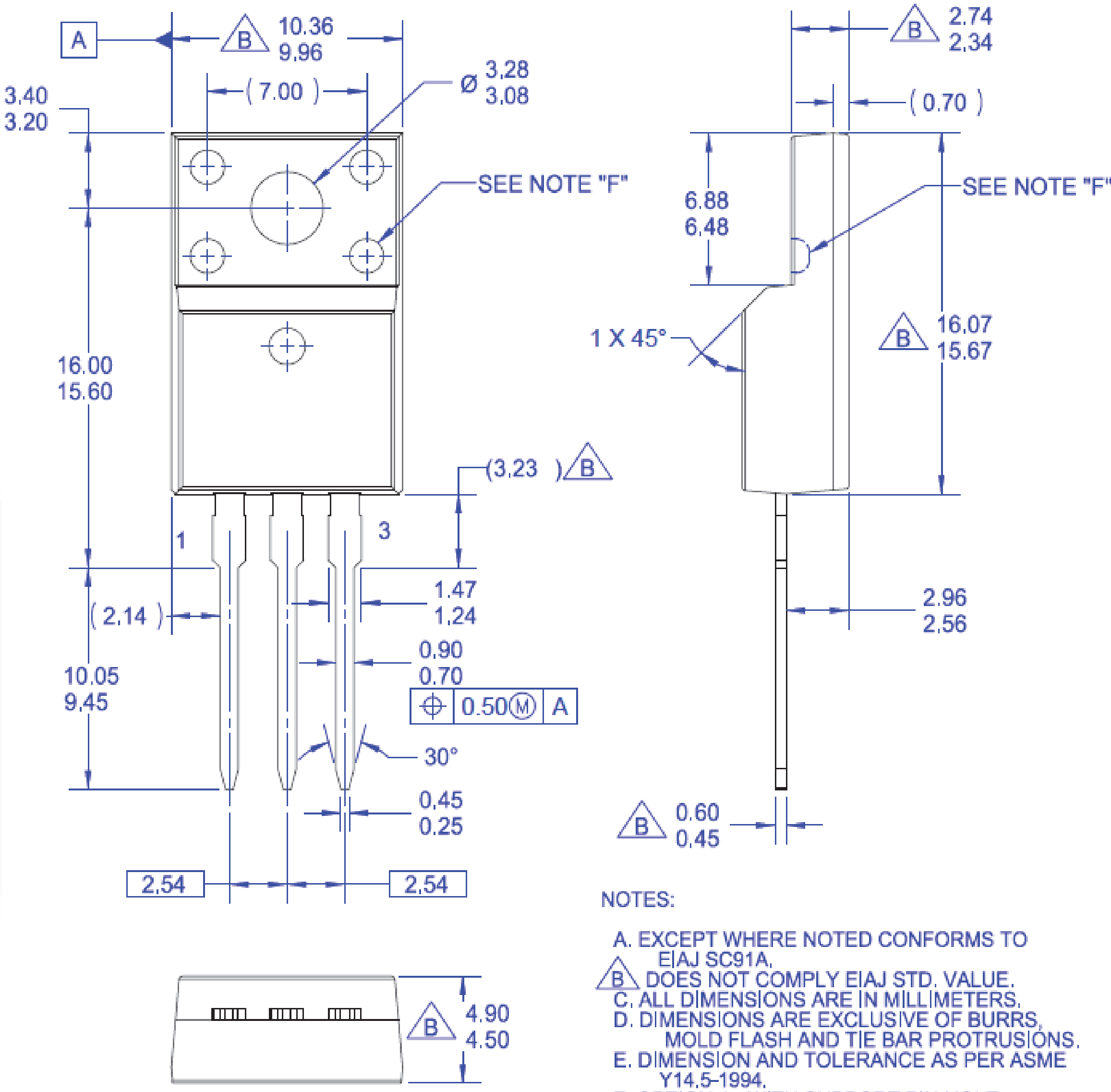
Mechanical Dimensions

TO-220 3L



Mechanical Dimensions

TO-220F 3L



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B. DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV4

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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