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ON Semiconductor®

FDP085N10A

N-Channel PowerTrench[®] MOSFET 100 V, 96 A, 8.5 m Ω

Features

- $R_{DS(on)}$ = 7.35 m Ω (Typ.) @ V_{GS} = 10 V, I_D = 96 A
- · Fast Switching Speed
- Low Gate Charge, Q_G = 31 nC (Typ.)
- High Performance Trench Technology for Extremely Low $R_{\mbox{\footnotesize{DS}}(\mbox{\footnotesize{on}})}$
- · High Power and Current Handling Capability
- · RoHS Compliant

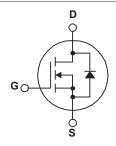
Description

This N-Channel MOSFET is produced using ON Semiconductor's PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- · Motor Drives and Uninterruptible Power Supplies





MOSFET Maximum Ratings $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol		Parameter		FDP085N10A-F102	Unit
V _{DSS}	Drain to Source Voltage			100	V
V_{GSS}	Gate to Source Voltage			±20	V
I_	Drain Current	96	Α		
ID	Diain Current	- Continuous (T _C = 100°C)	- Continuous (T _C = 100°C)		
I _{DM}	Drain Current	- Pulsed	(Note 1)	384	Α
E _{AS}	Single Pulsed Avalanche	Energy	(Note 2)	269	mJ
dv/dt	Peak Diode Recovery dv/	dt	(Note 3)	6.0	V/ns
D.	Power Dissipation	(T _C = 25°C)		188	W
P_{D}	1 Ower Dissipation	- Derate Above 25°C	- Derate Above 25°C		W/°C
T _J , T _{STG}	Operating and Storage Te	mperature Range		-55 to +175	°C
T_L	Maximum Lead Temperat	ure for Soldering, 1/8" from Case for 5 Se	econds	300	°C

Thermal Characteristics

Symbol	Parameter	FDP085N10A-F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDP085N10A-F102	FDP085N10A	TO-220	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_C = 25^{\circ} C$	100	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.07	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V	-	-	1	
I _{DSS} Zero Gate voltage Drain Curr	Zero Gate voltage Drain Current	$V_{DS} = 80 \text{ V}, T_{C} = 150^{\circ}\text{C}$	-	-	500	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 96 \text{ A}$	-	7.35	8.5	mΩ
9 _{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 96 \text{ A}$	1	72	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V - 50 V V - 0 V		-	2025	2695	pF
C _{oss}	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		-	468	620	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		-	20	-	pF
C _{oss(er)}	Energy Releted Output Capacitance	V _{DS} = 50 V, V _{GS} = 0 V		-	752	-	pF
Q _{g(tot)}	Total Gate Charge at 10V			-	31	40	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V, V _{DS} = 50 V,		-	9.7	-	nC
Q _{gs2}	Gate Charge Threshoid to Plateau	I _D = 96 A		-	5.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Not	te 4)	-	7.5	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz		-	0.97	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	18	46	ns
t _r		$V_{DD} = 50 \text{ V}, I_{D} = 96 \text{ A},$	-	22	54	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	29	68	ns
t _f	Turn-Off Fall Time	(Note 4)	-	8	26	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	96	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	384	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 96 A	-	-	1.3	V
t _{rr}	Reverse Recovery Time	$V_{DD} = 50 \text{ V}, V_{GS} = 0 \text{ V}, I_{SD} = 96 \text{ A},$	-	59	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	80	-	nC

Notes:

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. L = 3 mH, I_{AS} = 13.4 A, R_G = 25 Ω , starting T_J = 25°C.
- 3. $I_{SD} \le 96$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le BV_{DSS}$, starting $T_J = 25^{\circ}C$.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

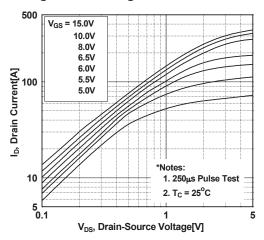


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

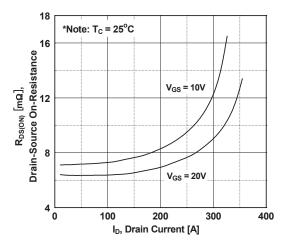


Figure 5. Capacitance Characteristics

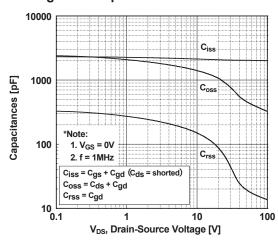


Figure 2. Transfer Characteristics

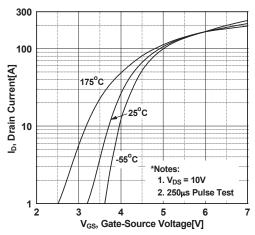


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

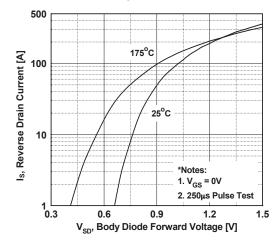
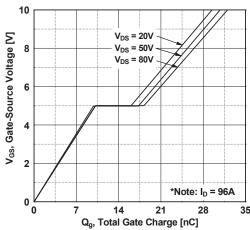


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

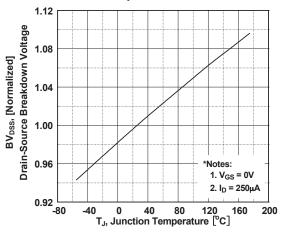


Figure 9. Maximum Safe Operating Area

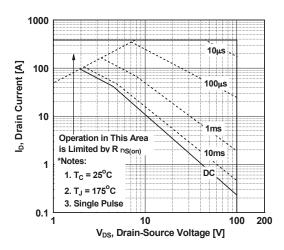


Figure 11. Eoss vs. Drain to Source Voltage

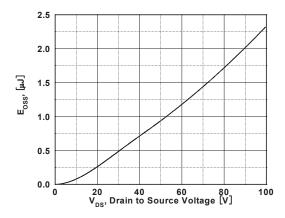


Figure 8. On-Resistance Variation vs. Temperature

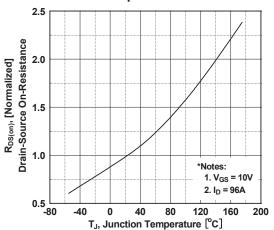


Figure 10. Maximum Drain Current vs. Case Temperature

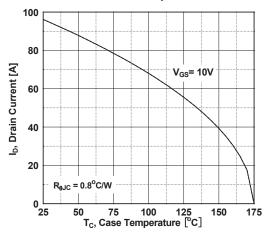
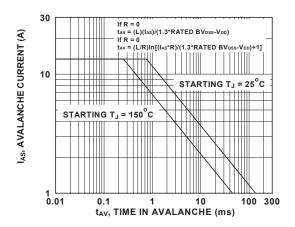
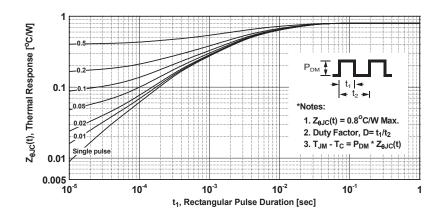


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



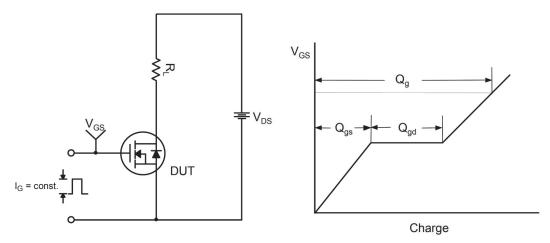


Figure 14. Gate Charge Test Circuit & Waveform

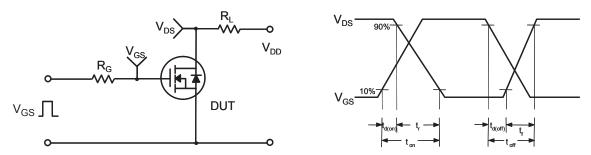


Figure 15. Resistive Switching Test Circuit & Waveforms

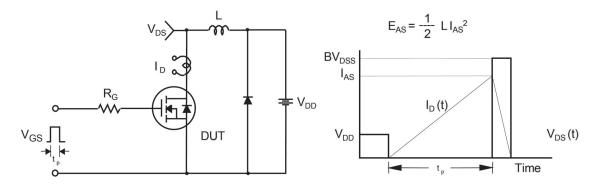
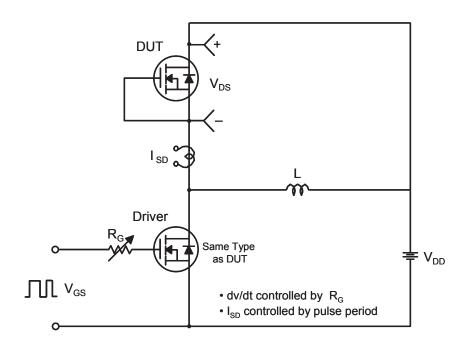


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms



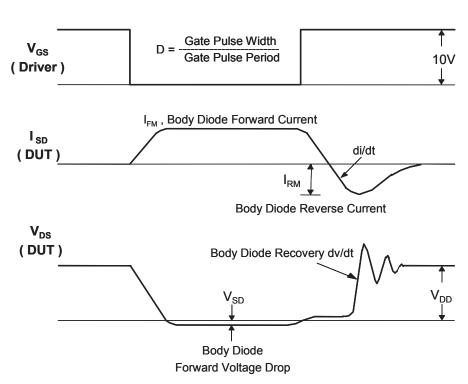
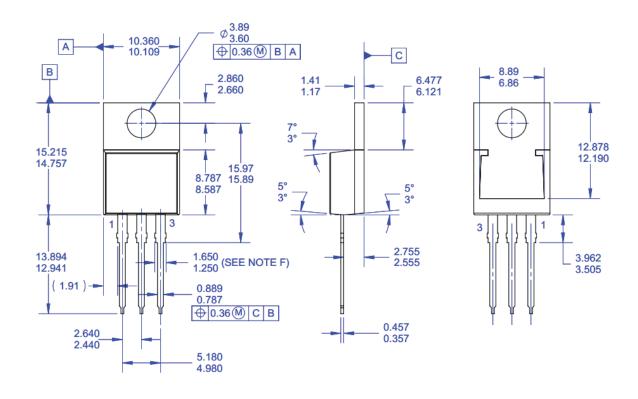
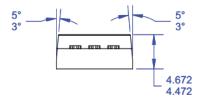


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions





NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 **VARIATION AB**
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS,
- MOLD FLASH AND TIE BAR PROTRUSIONS.
 THIS PACKAGE IS FSZZ INTERNAL PRODUCTION
- AND INTENDED FOR DELTA CUSTOMER ONLY.
- F. MAX WIDTH FOR F102 DEVICE = 1.35mm. G. DRAWING FILE NAME: T0220T03REV3

Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB (Delta)

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