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November 2013

FDP032N08B N-Channel PowerTrench[®] MOSFET 80 V, 211 A, 3.3 mΩ

Features

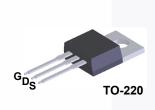
- $R_{DS(on)}$ = 2.85 m Ω (Typ.) @ V_{GS} = 10 V, I_{D} = 50 A
- Low FOM R_{DS(on)} * Q_G
- Low Reverse-Recovery Charge, Qrr
- Soft Reverse-Recovery Body Diode
- Enables High Efficiency in Synchronous Rectification
- · Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

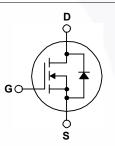
Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FDP032N08B_F102	Unit
V _{DSS}	Drain to Source Voltage	80	V	
V _{GSS}	Gate to Source Voltage		±20	V
I _D		- Continuous (T _C = 25°C, Silicon Limited)	211*	
	Drain Current	- Continuous (T _C = 100 ^o C, Silicon Limited)	149*	A
		- Continuous (T _C = 25°C, Package Limited)	120	
I _{DM}	Drain Current	- Pulsed (Note 1)	844	Α
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		649	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P _D	Power Discipation	(T _C = 25 ^o C)	263	W
	Power Dissipation	- Derate Above 25°C	1.75	W/ºC
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

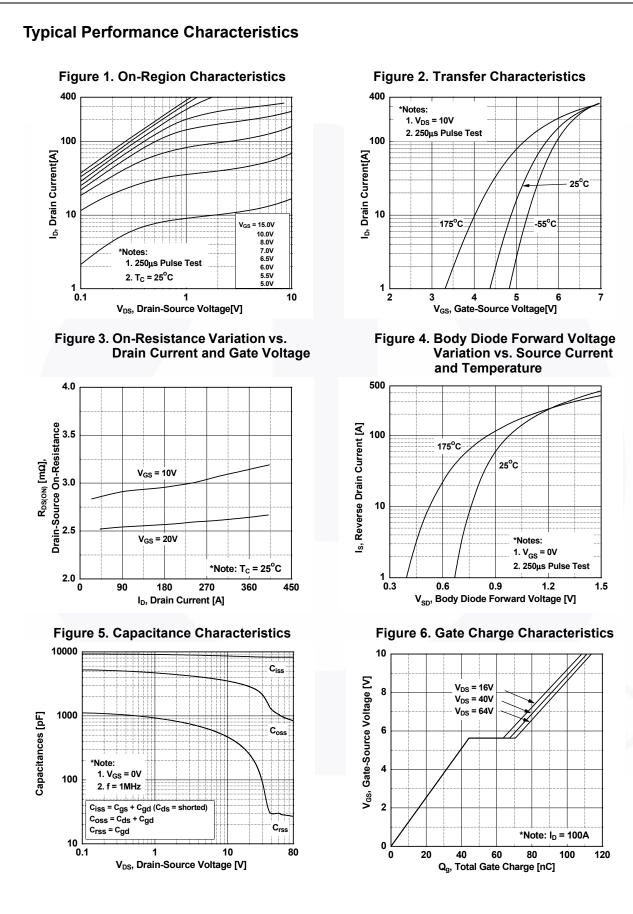
* Package limitation current is 120A.

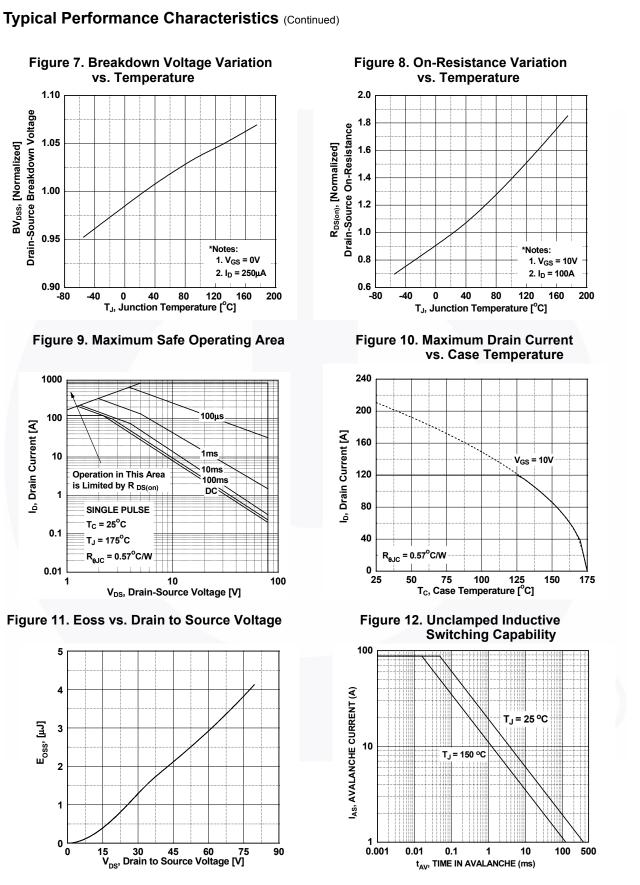
Thermal Characteristics

Symbol	Parameter FDP032N08B_		Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.57	°C/W
R _{0JA} Thermal Resistance, Junction to Ambient, Max. 62.5		0.00	

Part Number Top Mark Pack		Package	e Packing Method Reel Size		Тар	e Width	Qua	ntity	
		TO-220	Tube	N/A		N/A	50 units		
Electrica	I Chara	acteristics T_c =	25°C unless	otherwise noted.					
Symbol	Parameter			Test Conditions		Min.	Тур.	Max.	Unit
Off Charac	teristics	5							
BV _{DSS}	Drain to	Source Breakdown V	/oltage	I _D = 250 μA, V _{GS} = 0 V		80	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient		-	$I_D = 250 \ \mu$ A, Referenced to 25° C		-	0.04	-	V/ºC
DSS	Zero Ga	te Voltage Drain Curr	ent	$V_{DS} = 64 V, V_{GS} = 0 V$ $V_{DS} = 64 V, T_{C} = 150^{\circ}C$		-	-	1 500	μA
I _{GSS}	Gate to I	Body Leakage Currer	nt	$V_{\text{GS}} = \pm 20 \text{ V}, \text{ V}_{\text{DS}} = 0$		-	-	±100	nA
				VGS 120 V, VDS 0	•			100	10.0
On Charac				V - V 250 ···	•	0.5		4.5	V
V _{GS(th)}		reshold Voltage rain to Source On Res	istance	$V_{GS} = V_{DS}, I_D = 250 \mu$		2.5	-	4.5	V
R _{DS(on)}		Transconductance	sistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 100 \text{ A}$ $V_{DS} = 10 \text{ V}, \text{ I}_{D} = 100 \text{ A}$		-	2.85	3.3	mΩ S
9 _{FS}			-	$v_{\rm DS} = 10 v, r_{\rm D} = 100 F$	`	-	168	-	5
Dynamic C							1		
C _{iss}	Input Ca	pacitance		V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz		-	8245	10965	pF
C _{oss}	Output C	Capacitance				-	1250	1660	pF
C _{rss}	Reverse	Transfer Capacitance	e			-	28	-	pF
C _{oss(er)}	Energy F	Energy Related Output Capacitance		V _{DS} = 40 V, V _{GS} = 0 V		-	2337	-	pF
Q _{g(tot)}	Total Ga	te Charge at 10V				-	111	144	nC
Q _{gs}	Gate to S	Source Gate Charge		$V_{DS} = 40 \text{ V}, \text{ I}_{D} = 100 \text{ A},$ $V_{GS} = 10 \text{ V}$ (Note 4)		-	44	-	nC
Q _{gd}	Gate to I	Drain "Miller" Charge				-	23	-	nC
V _{plateau}	Gate Pla	ateau Volatge				-	5.6	-	V
Q _{sync}	Total Ga	te Charge Sync.	Charge Sync. $V_{DS} = 0 V, I_D = 50 A$		-	98.2	-	nC	
Q _{oss}	Output Charge			V _{DS} = 40 V, V _{GS} = 0 V		-	114	-	nC
ESR	Equivale	ent Series Resistance	(G-S)	f = 1 MHz		-	2.3	-	Ω
Switching	Charact	eristics							
t _{d(on)}	Т	Delay Time					38	86	ns
t _r	Turn-On	Rise Time		$V_{DD} = 40 \text{ V}, \text{ I}_{D} = 100 \text{ A},$ $V_{GS} = 10 \text{ V}, \text{ R}_{G} = 4.7 \Omega$		-	44	97	ns
t _{d(off)}	Turn-Off	Delay Time				-	71	152	ns
t _f	_	Fall Time		_	(Note 4)	-	31	72	ns
Drain-Sour	ce Diod	le Characteristic	s						
I _S		n Continuous Drain to		e Forward Current		-	-	211	Α
I _{SM}	Maximum Pulsed Drain to Source Diode					-	-	844	Α
V _{SD}	Drain to Source Diode Forward Voltage $V_{GS} = 0 \text{ V}, I_{SD} = 100$		4	-	-	1.3	V		
t _{rr}		Recovery Time	Ŭ	$V_{GS} = 0 V, V_{DD} = 40 V$		-	75	-	ns
Q _{rr}		Recovery Charge		dl _F /dt = 100 A/μs	, 30,	-	102		nC
Notes:		, <u></u>							-

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1.10

1.05

1.00

0.95

0.90

1000

100

10

1

0.1

0.01

1

5

4

2

1

0 L 0

E_{oss}, [µJ] 3

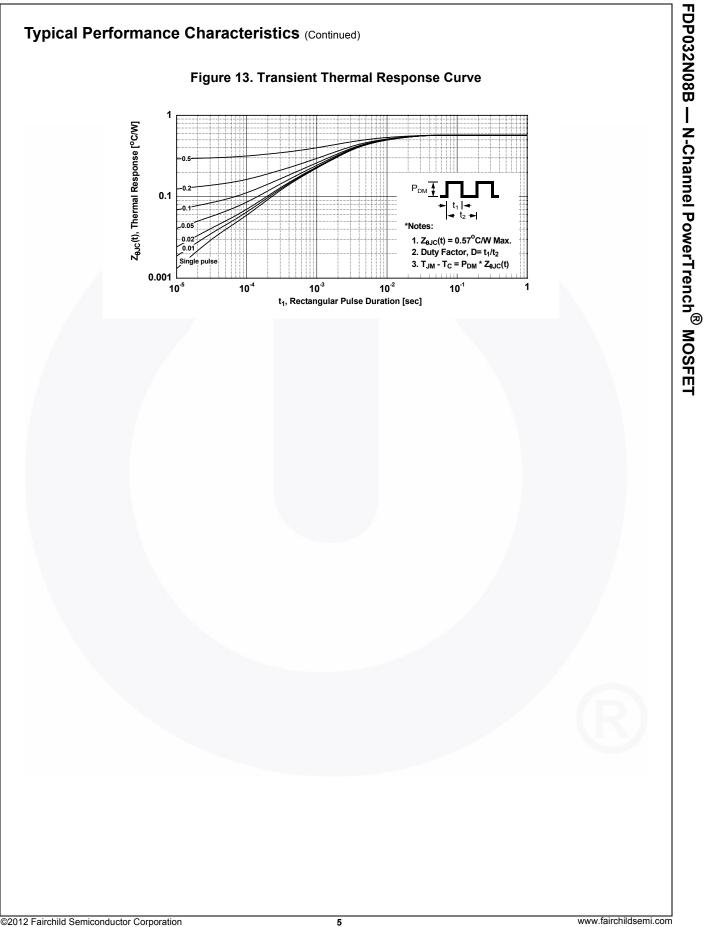
l_b, Drain Current [A]

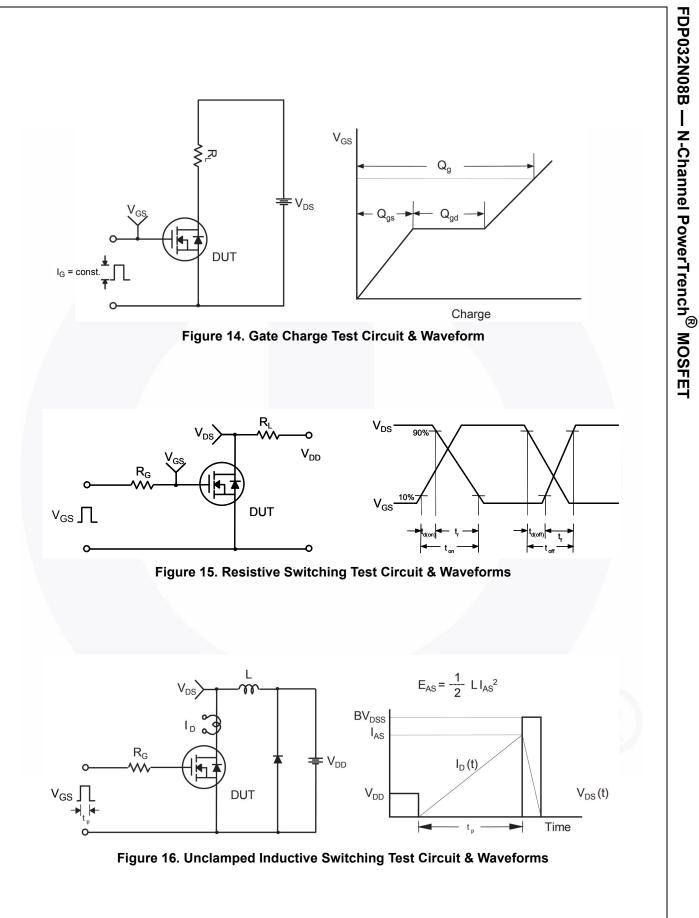
-80

-40

Drain-Source Breakdown Voltage

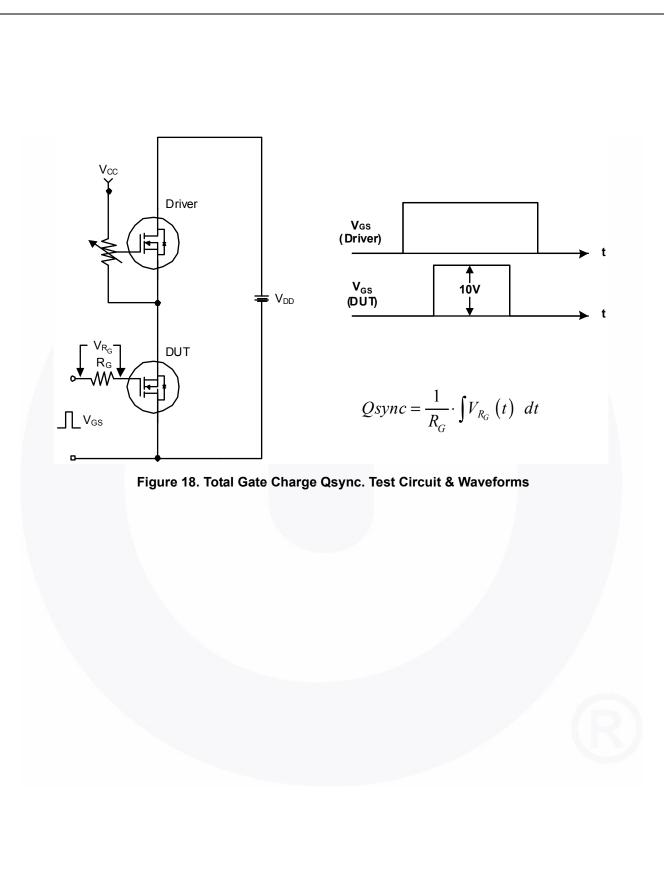
BV_{DSS}, [Normalized]

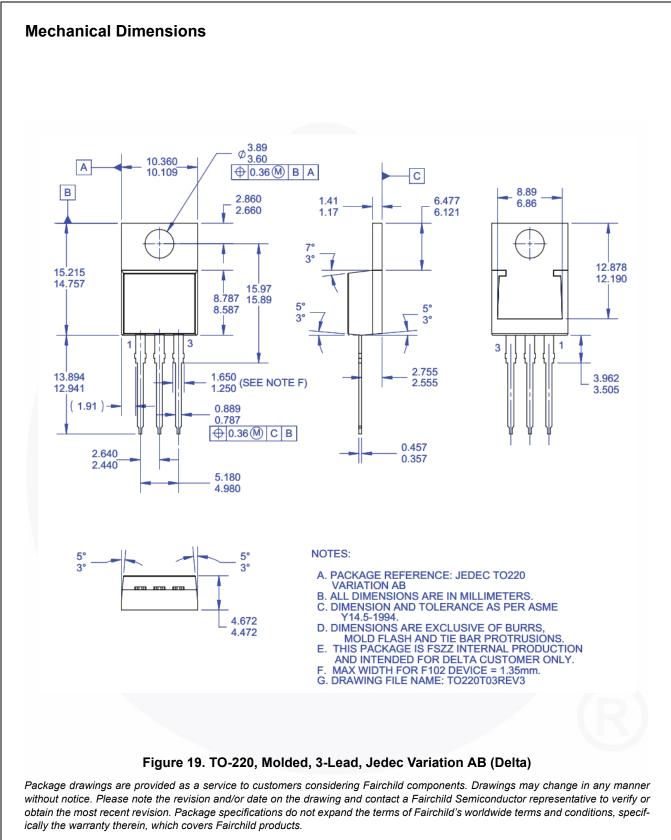




DUT + v_{DS} a ۱_{SD} م L Driver R_G, Same Type as DUT L F ∨_{DD} $\prod V_{GS}$ • dv/dt controlled by R_{G} • I_{SD} controlled by pulse period Î Gate Pulse Width V_{GS} D = Gate Pulse Period 10V (Driver) I_{FM}, Body Diode Forward Current I _{SD} di/dt (DUT) I_{RM} Body Diode Reverse Current V_{DS} (DUT) Body Diode Recovery dv/dt V_{SD} V_{DD} Body Diode Forward Voltage Drop Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

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