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# FDMS030N06B

## N-Channel PowerTrench® MOSFET

60 V, 100 A, 3 mΩ

### Features

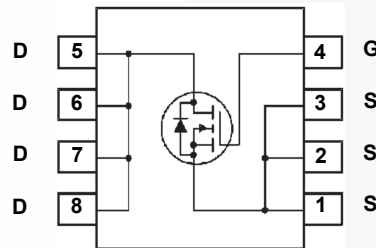
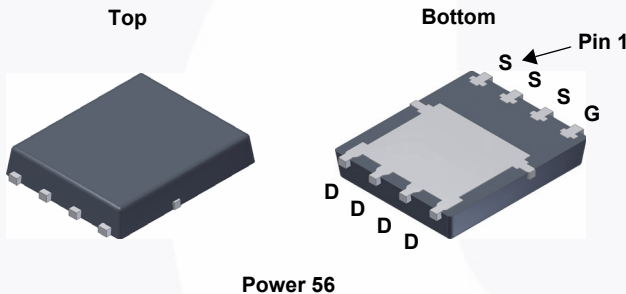
- $R_{DS(on)} = 2.4 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 50 \text{ A}$
- Advanced Package and Silicon Combination for Low  $R_{DS(on)}$  and High Efficiency
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor drives and Uninterruptible Power Supplies
- Renewable system



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDMS030N06B	Unit
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ ) (Note 1)	100
		- Continuous ( $T_A = 25^\circ\text{C}$ ) (Note 2a)	22.1
$I_{DM}$	Drain Current	- Pulsed (Note 3)	400
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 4)	248
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	104
		( $T_A = 25^\circ\text{C}$ ) (Note 2a)	2.5
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FDMS030N06B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2a)	50	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS030N06B	FDMS030N06B	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0\text{V}$	60	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.03	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.5	3.3	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 50\text{A}$	-	2.4	3.0	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 50\text{A}$	-	119	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	5685	7560	pF
$C_{oss}$	Output Capacitance		-	1720	2290	pF
$C_{rss}$	Reverse Transfer Capacitance		-	59	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	2504	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 30\text{V}, I_D = 50\text{A}$ $V_{GS} = 0\text{V to } 10\text{V}$	-	75	-	nC
$Q_{gs}$	Gate to Source Gate Charge		-	30	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	14	-	nC
$V_{plateau}$	Gate Plateau Voltage		(Note 5)	-	5.4	-
$Q_{sync}$	Total Gate Charge Sync.	$V_{DS} = 0\text{V}, I_D = 50\text{A}$	-	66.2	-	nC
$Q_{oss}$	Output Charge	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$	-	174	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{MHz}$	-	1.05	-	$\Omega$

### Switching Characteristics

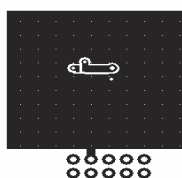
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}, I_D = 50\text{A}$ $V_{GS} = 10\text{V}, R_G = 4.7\Omega$	-	39	88	ns
$t_r$	Turn-On Rise Time		-	20	50	ns
$t_{d(off)}$	Turn-Off Delay Time		-	52	114	ns
$t_f$	Turn-Off Fall Time		(Note 5)	-	16	42

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	100	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	400	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 50\text{A}$	-	-	1.25	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 50\text{A}$	-	71	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$	-	85	-	nC

#### Notes:

- Silicon limited  $I_D$  rating = 147 A.
- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.

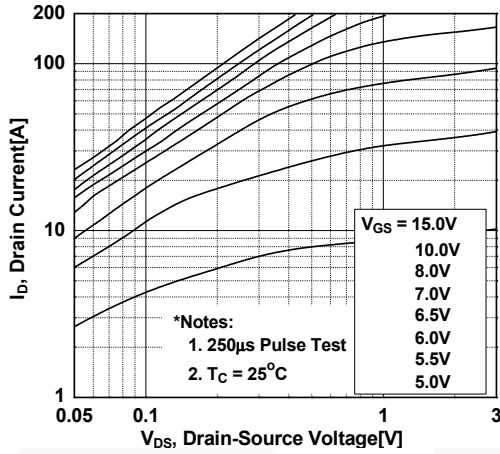


b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

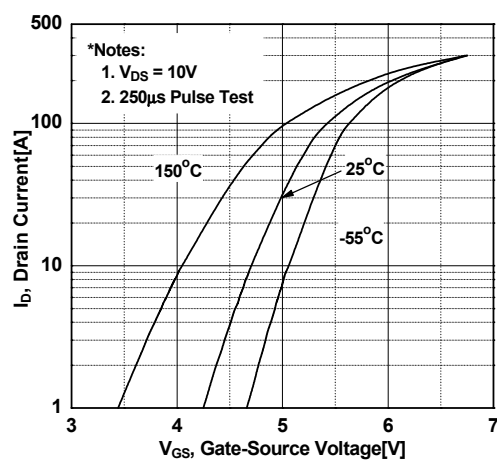
- Repetitive rating: pulse-width limited by maximum junction temperature.
- $L = 0.3\text{mH}, I_{AS} = 40.7\text{A}, V_{DD} = 50\text{V}, V_{GS} = 10\text{V}$ , starting  $T_J = 25^\circ\text{C}$ .
- Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

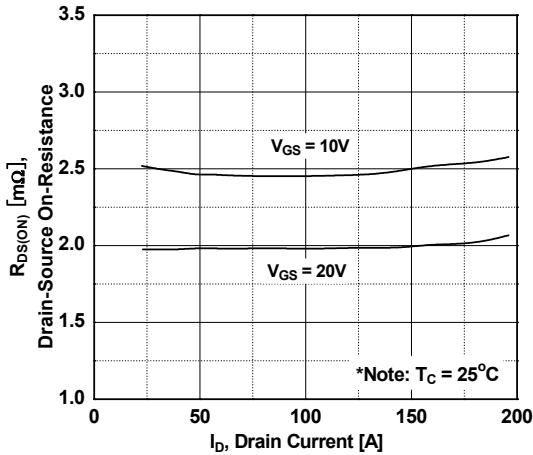
**Figure 1. On-Region Characteristics**



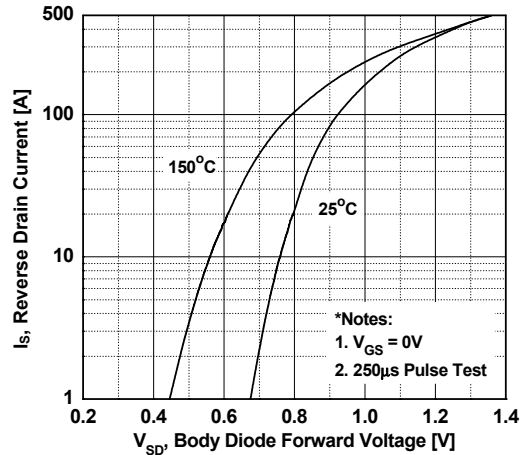
**Figure 2. Transfer Characteristics**



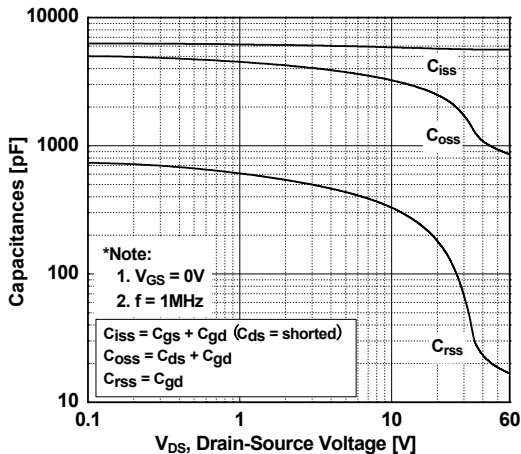
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



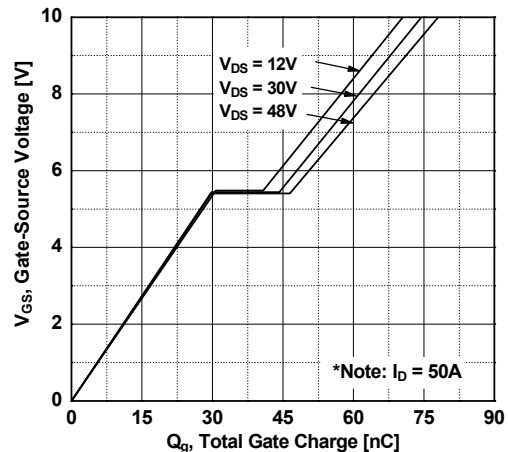
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

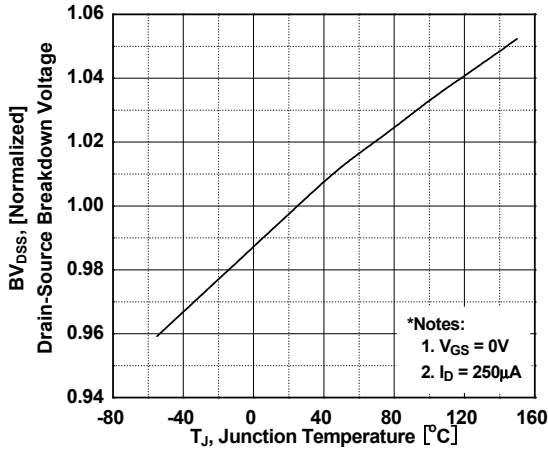


Figure 8. On-Resistance Variation vs. Temperature

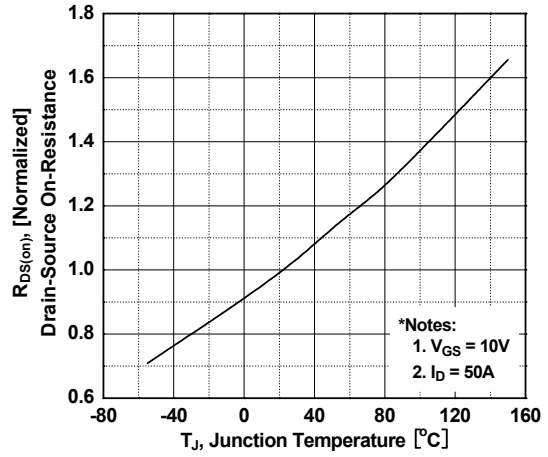


Figure 9. Maximum Safe Operating Area

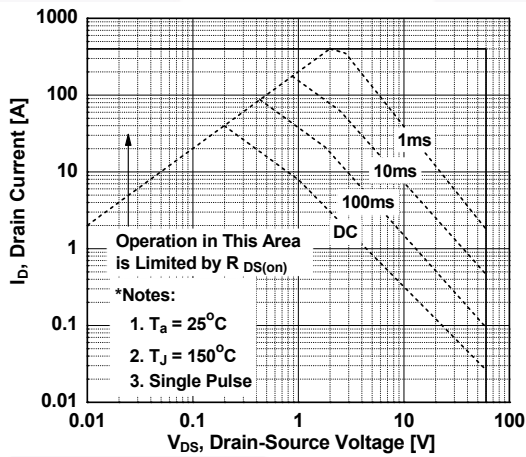


Figure 10. Maximum Drain Current vs. Case Temperature

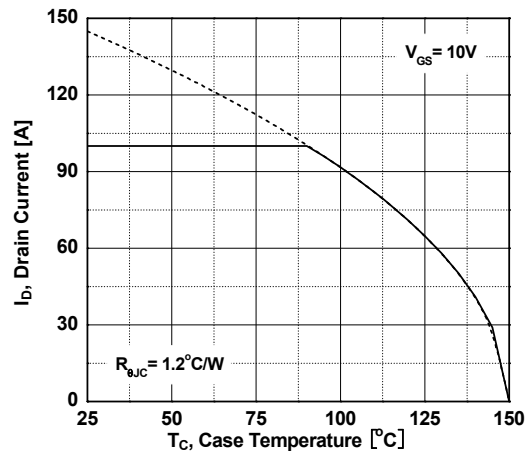


Figure 11. E\_oss vs. Drain to Source Voltage

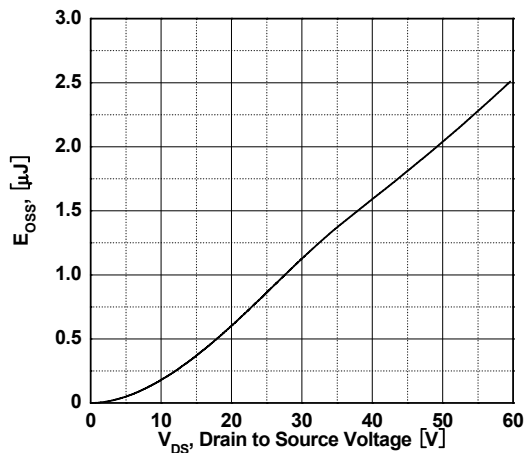
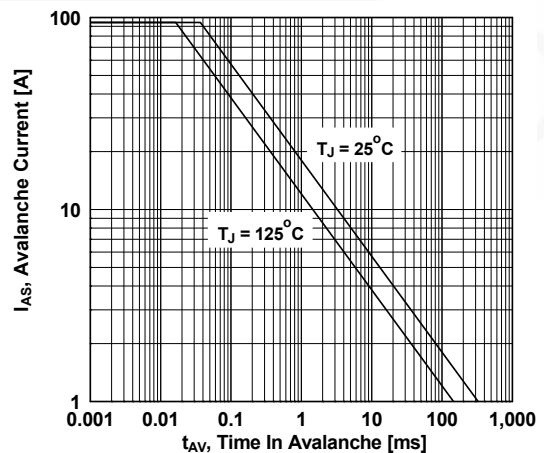
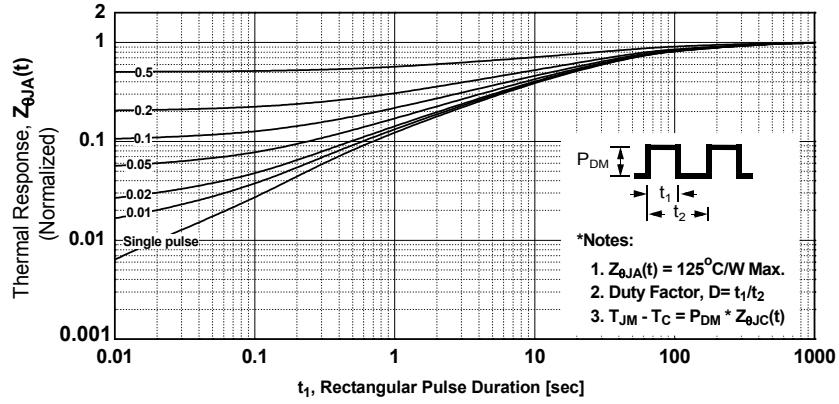


Figure 12. Unclamped Inductive Switching Capability

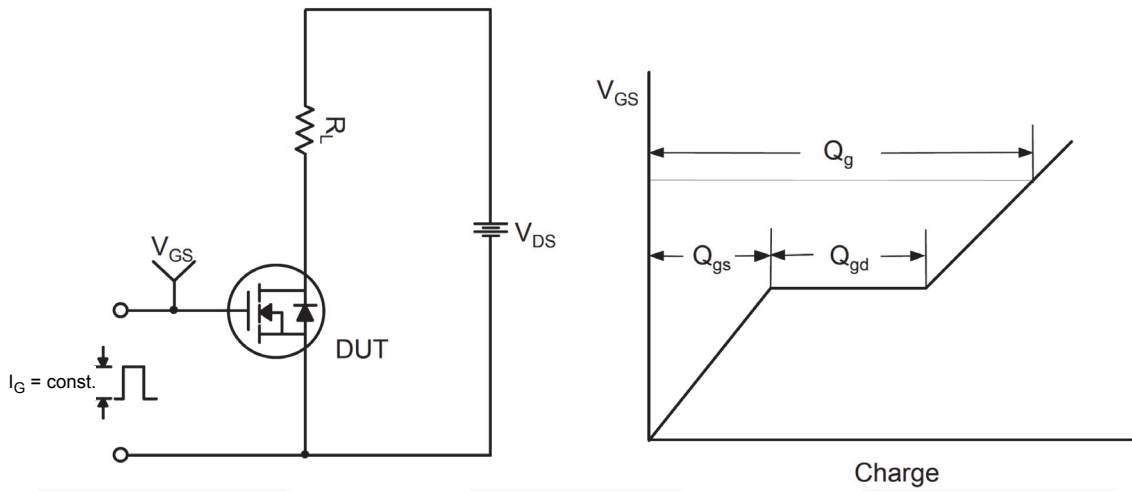


Typical Performance Characteristics (Continued)

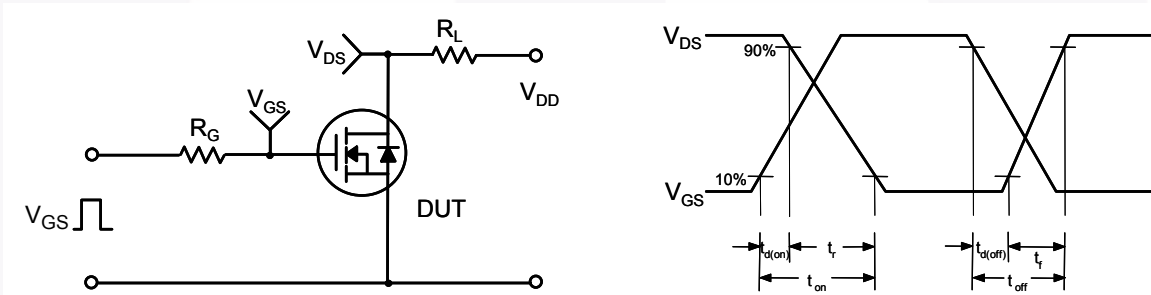
Figure 13. Transient Thermal Response Curve



**Figure 14. Gate Charge Test Circuit & Waveform**



**Figure 15. Resistive Switching Test Circuit & Waveforms**



**Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms**

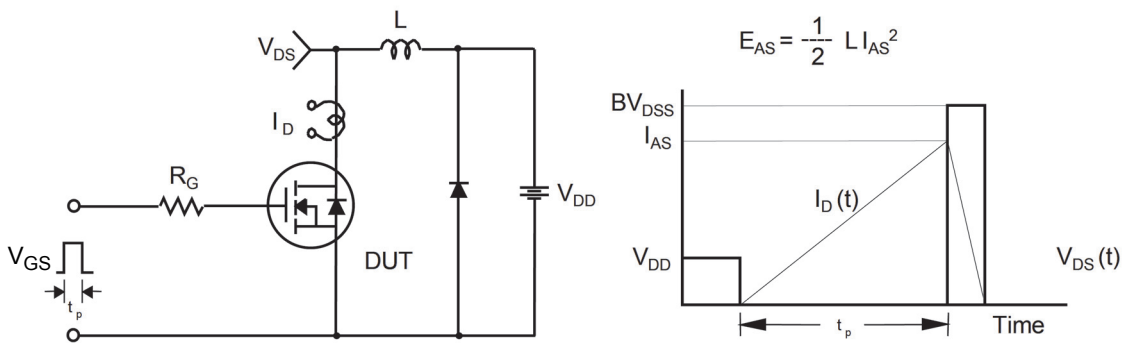


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

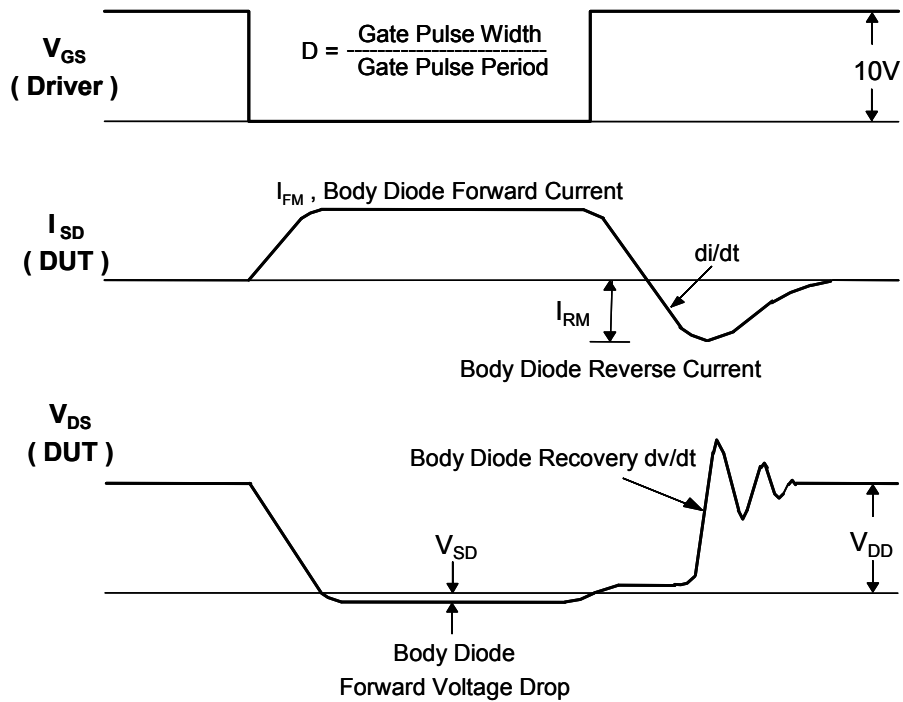
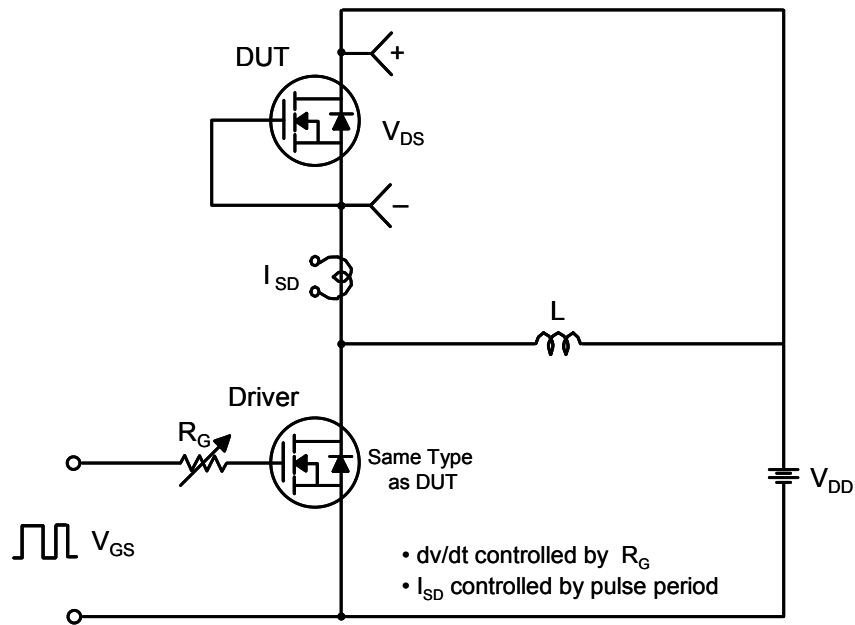
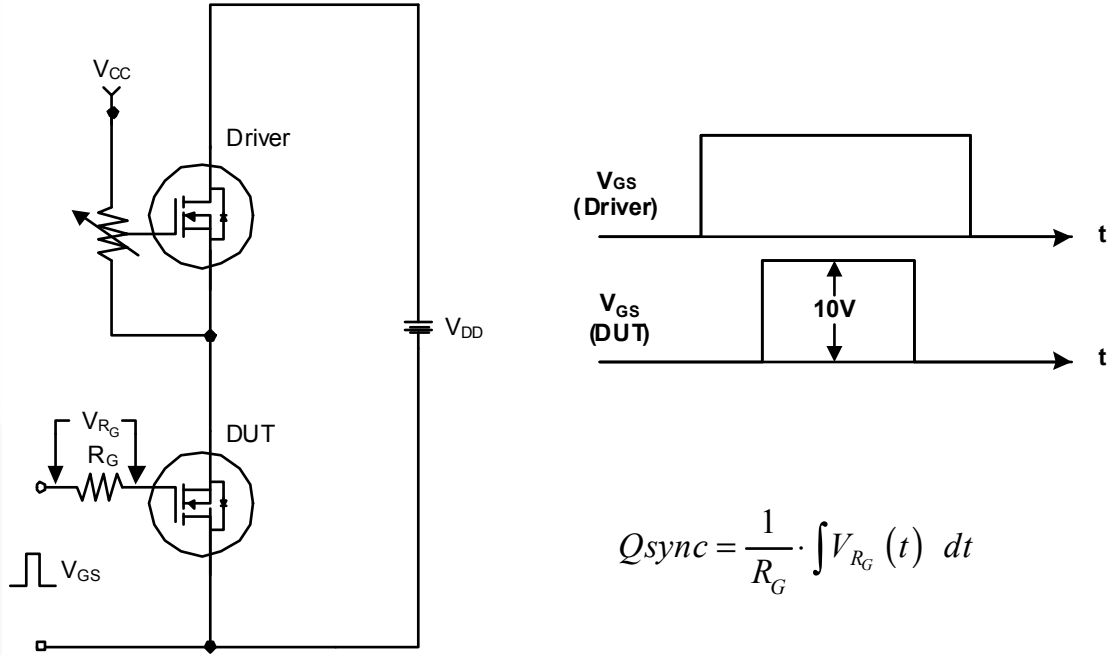
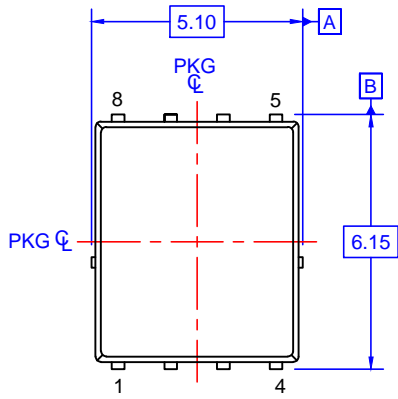




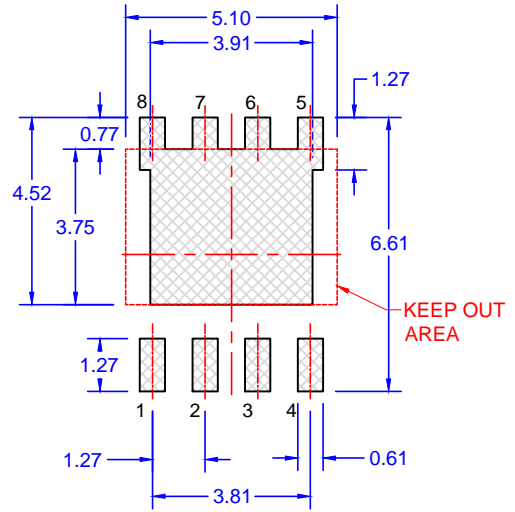
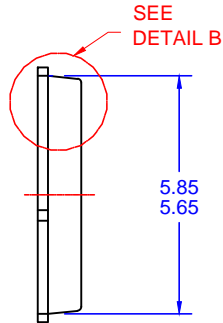
Figure 18. Total Gate Charge  $Q_{sync}$ . Test Circuit & Waveforms



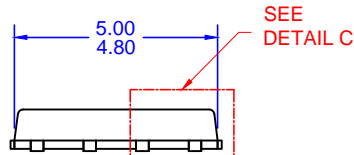
PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A



TOP VIEW

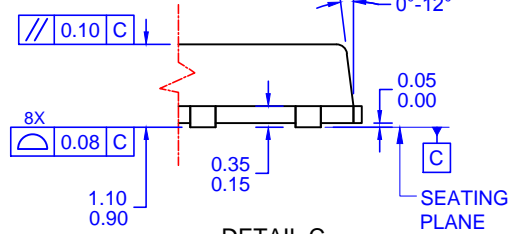


LAND PATTERN RECOMMENDATION

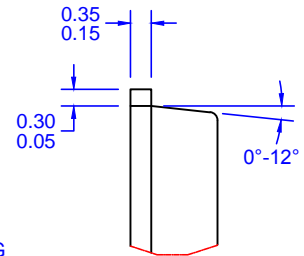


SIDE VIEW

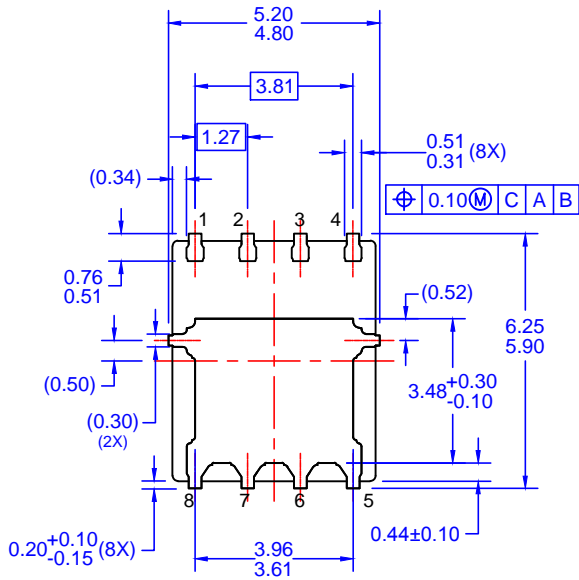
OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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