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June 2014

# FDMC8622

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 100 V, 16 A, 56 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 56 mΩ at  $V_{GS} = 10$  V,  $I_D = 4$  A
- Max  $r_{DS(on)}$  = 90 mΩ at  $V_{GS} = 6$  V,  $I_D = 3$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

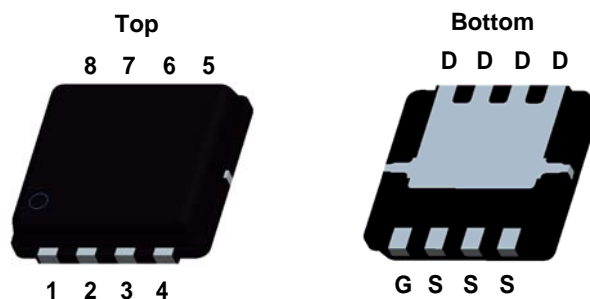


### General Description

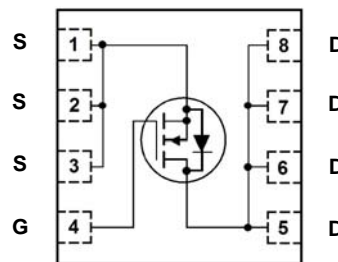
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

### Application

- DC-DC Primary Switch



MLP 3.3X3.3



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous $T_C = 25^\circ\text{C}$	16	A
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	4	
	-Pulsed (Note 4)	30	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	37	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	31	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	4.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8622	FDMC8622	MLP 3.3X3.3	13 "	12 mm	3000 units

# Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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## Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		69		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$ , $V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$ , $V_{DS} = 0\ \text{V}$			$\pm 100$	nA

## On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 4\ \text{A}$		43.7	56	m $\Omega$
		$V_{GS} = 6\ \text{V}$ , $I_D = 3\ \text{A}$		59.9	90	
		$V_{GS} = 10\ \text{V}$ , $I_D = 4\ \text{A}$ , $T_J = 125^\circ\text{C}$		76.4	98	
$g_{FS}$	Forward Transconductance	$V_{DD} = 10\ \text{V}$ , $I_D = 4\ \text{A}$		8.9		S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$		302	402	pF
$C_{oss}$	Output Capacitance			72.5	96	pF
$C_{rss}$	Reverse Transfer Capacitance			4.2	6	pF
$R_g$	Gate Resistance			1.0		$\Omega$

## Switching Characteristics

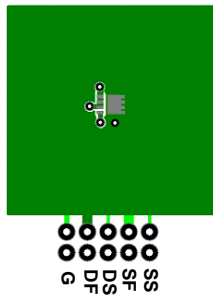
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$ , $I_D = 4\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_{GEN} = 6\ \Omega$		5.9	12	ns
$t_r$	Rise Time			1.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			10.2	18	ns
$t_f$	Fall Time			2.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 50\ \text{V}$ , $I_D = 4\ \text{A}$	5.2	7.3	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$		3.0	4.1	nC
$Q_{gs}$	Total Gate Charge			1.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			1.4		nC

## Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$ , $I_S = 4\ \text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\ \text{V}$ , $I_S = 1.7\ \text{A}$ (Note 2)		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 4\ \text{A}$ , $di/dt = 100\ \text{A}/\mu\text{s}$		36	57	ns
$Q_{rr}$	Reverse Recovery Charge			28	45	nC

### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3. Starting  $T_J = 25^\circ\text{C}$ ; N-ch:  $L = 3.0\ \text{mH}$ ,  $I_{AS} = 5.0\ \text{A}$ ,  $V_{DD} = 100\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .

4. Pulse  $I_d$  refers to Figure.11 Forward Bias Safe Operation Area.

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

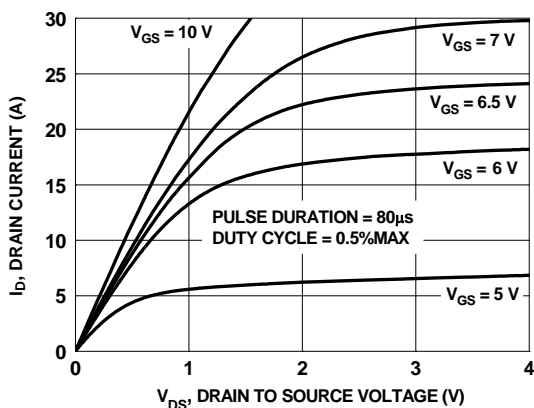


Figure 1. On-Region Characteristics

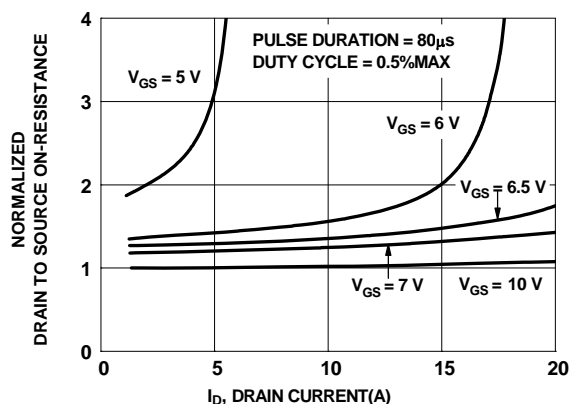


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

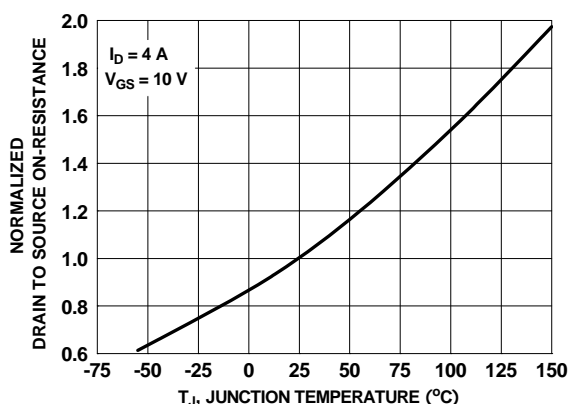


Figure 3. Normalized On-Resistance vs Junction Temperature

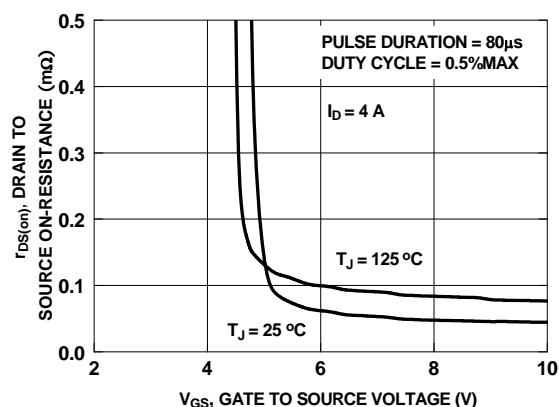


Figure 4. On-Resistance vs Gate to Source Voltage

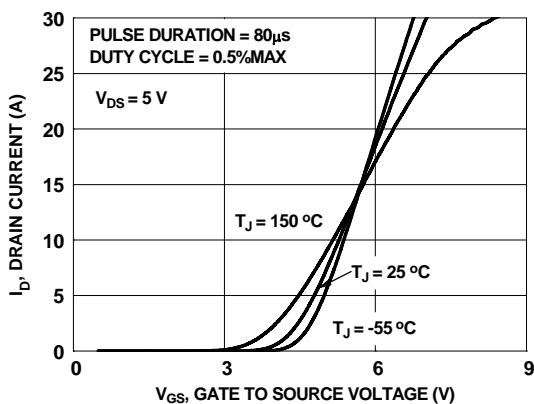


Figure 5. Transfer Characteristics

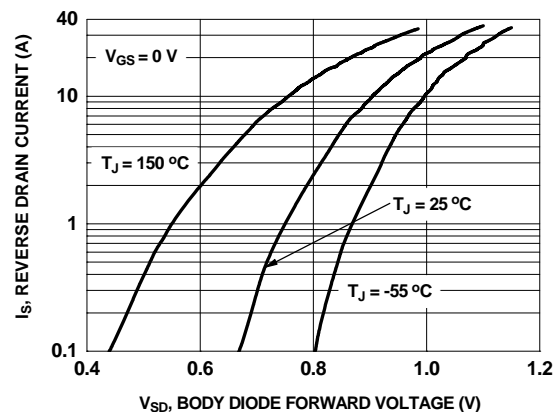


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

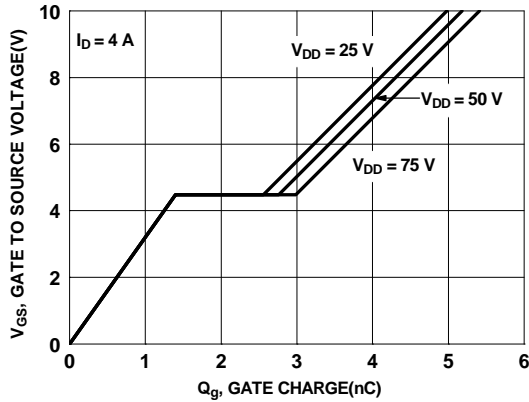


Figure 7. Gate Charge Characteristics

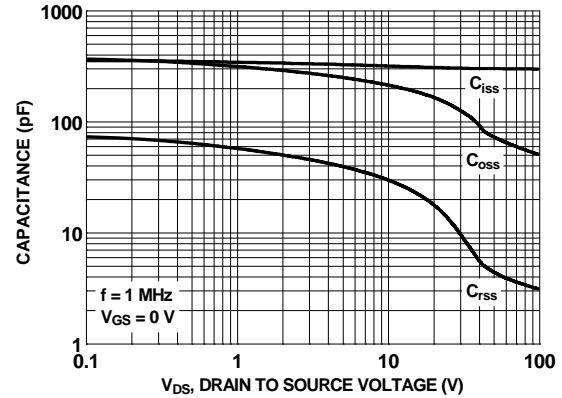


Figure 8. Capacitance vs Drain to Source Voltage

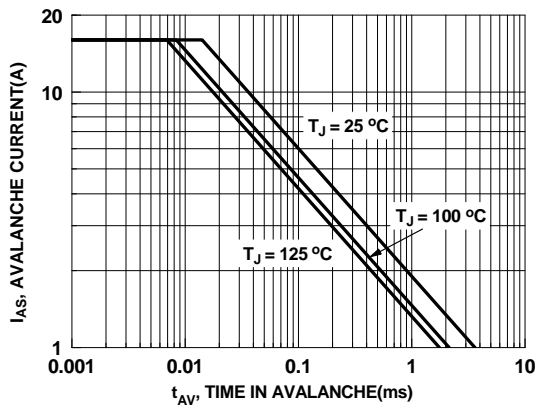


Figure 9. Unclamped Inductive Switching Capability

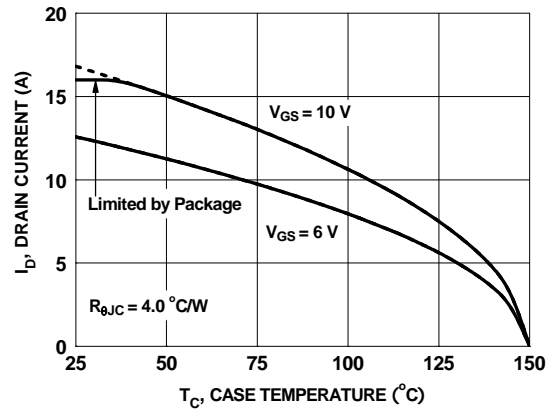


Figure 10. Maximum Continuous Drain Current vs Case Temperature

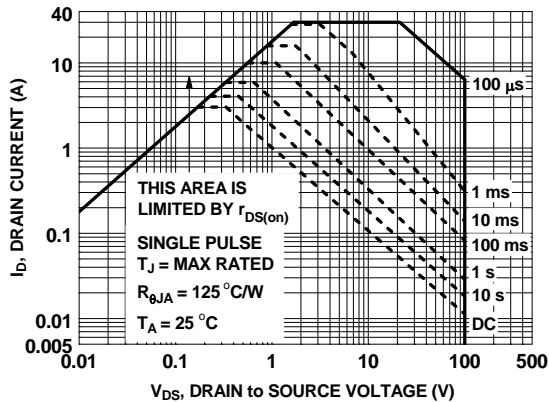


Figure 11. Forward Bias Safe Operating Area

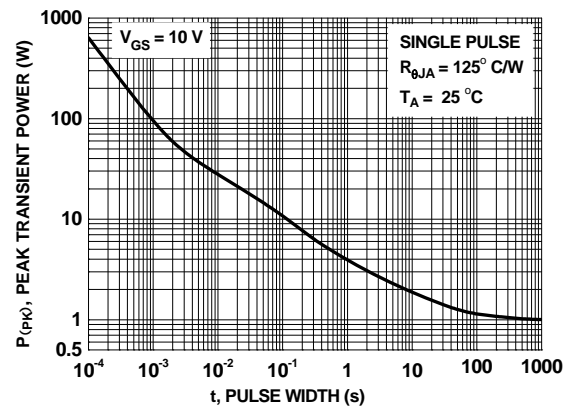


Figure 12. Single Pulse Maximum Power Dissipation

# Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

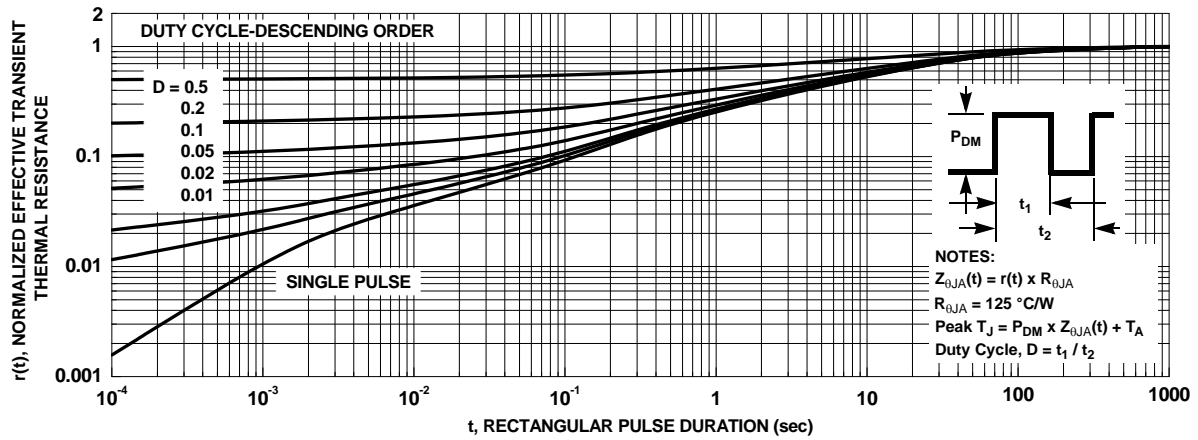
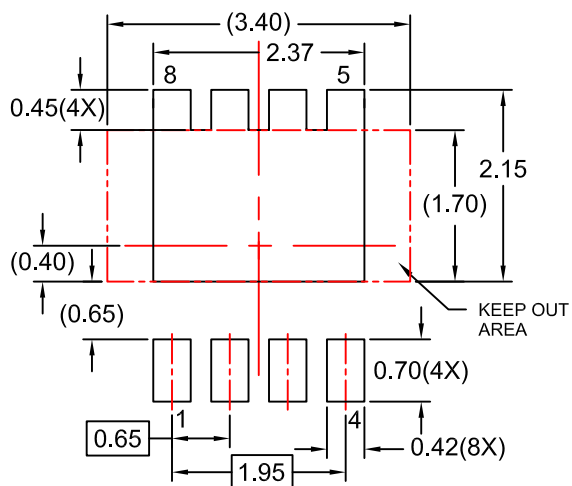
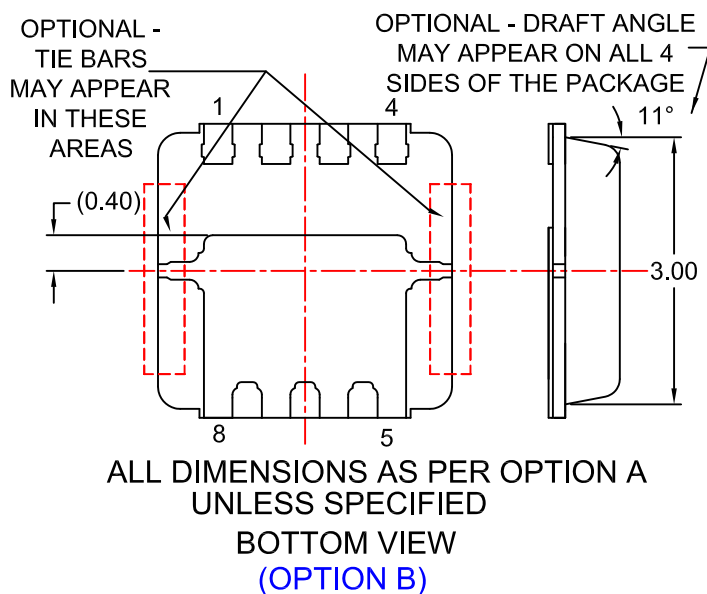
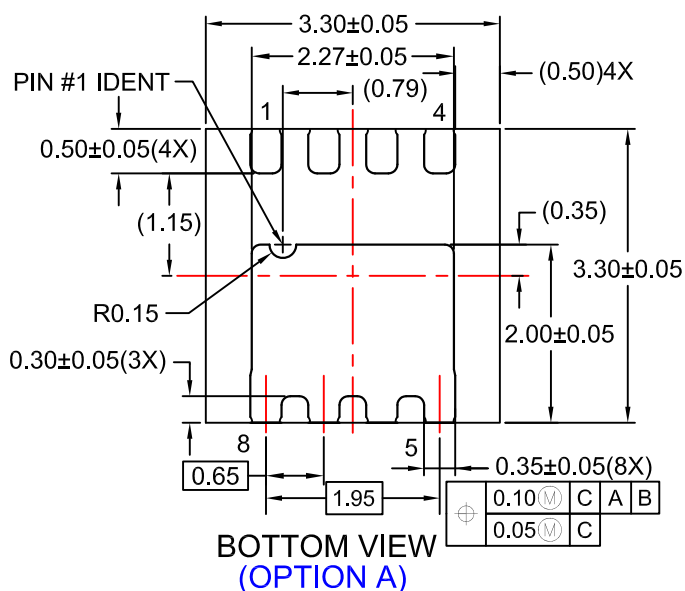
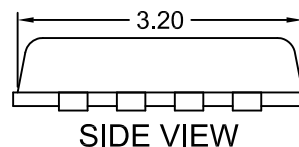
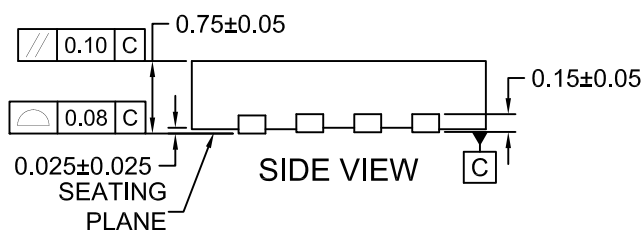
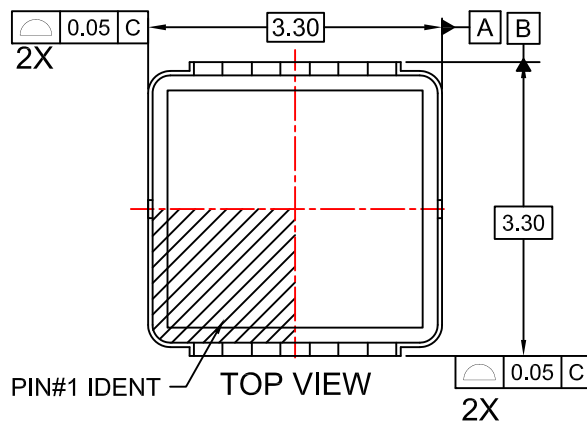
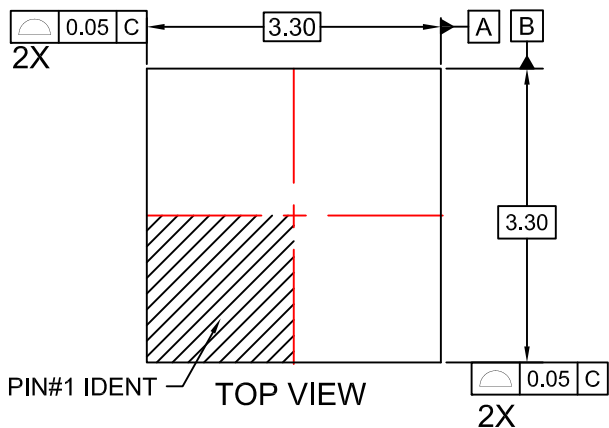
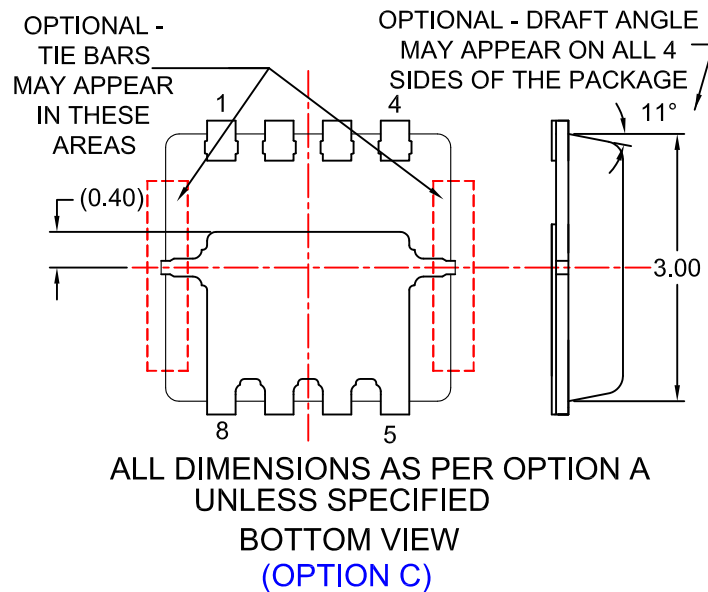
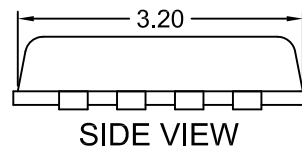
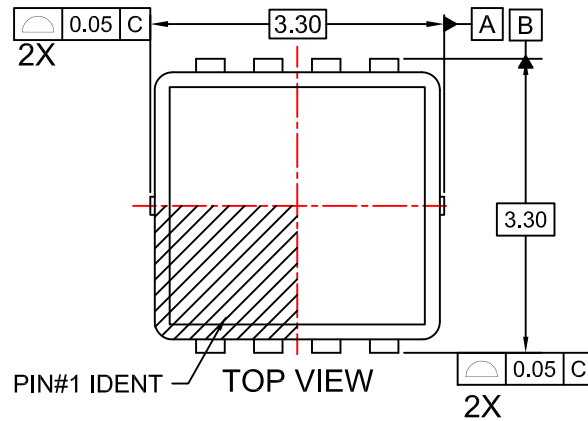


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



RECOMMENDED LAND PATTERN





#### NOTES:

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- G. OPTION A - SAWN MLP, OPTIONS B & C - PUNCH MLP.



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