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September 2013

## FDMC86102

# N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 100 V, 20 A, 24 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)} = 24 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 7 \text{ A}$
- Max  $r_{DS(on)}$  = 38 m $\Omega$  at  $V_{GS}$  = 6 V,  $I_D$  = 5 A
- Low Profile 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

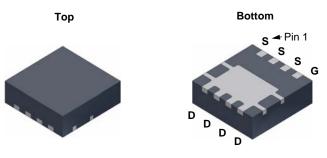


## **General Description**

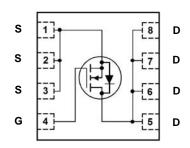
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

## **Application**

■ DC - DC Conversion







## MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parame		Ratings	Units	
$V_{DS}$	Drain to Source Voltage			100	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>C</sub> = 25 °C		20	
$I_D$	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	7	Α
	-Pulsed		(Note 4)	60	
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	72	mJ
D	Power Dissipation	T <sub>C</sub> = 25 °C		41	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.3	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperat	ture Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86102	FDMC86102	Power 33	13"	12 mm	3000 units

## **Electrical Characteristics** $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	ncteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		69		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

#### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-9		mV/°C
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A		19.4	24	
r <sub>DS(on)</sub>	r <sub>DS(on)</sub> Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 5 \text{ A}$		26.8	38	mΩ
	$V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}, T_J = 125 ^{\circ}\text{C}$		32.8	41		
9 <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = 10 V, I <sub>D</sub> = 7 A		19		S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 50 V V 0 V	725	965	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	175	235	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12	15	25	pF
$R_{q}$	Gate Resistance		0.5		Ω

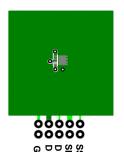
## **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time				8	17	ns
t <sub>r</sub>	Rise Time		$V_{DD} = 50 \text{ V}, I_D = 7 \text{ A},$		4	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$			14	25	ns
t <sub>f</sub>	Fall Time				4	10	ns
0	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}$			13	18	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to 5 V}$	V <sub>DD</sub> = 50 V		8	11	nC
$Q_{gs}$	Total Gate Charge		$I_D = 7 A$		3.7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		_		3.6		nC

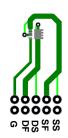
### **Drain-Source Diode Characteristics**

Veb Source to Drain Dioge Forward voltage	Source to Drain Diade Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 7 \text{ A}$	(Note 2)	0.81	1.3	\/
	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$	(Note 2)	0.75	1.2	\ \	
t <sub>rr</sub>	Reverse Recovery Time			44	70	ns
Q <sub>rr</sub>	Reverse Recovery Charge			40	65	nC
NOTES:	·		•			

<sup>1.</sup> R<sub>0JA</sub> is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

<sup>2.</sup> Pulse Test: Pulse Width < 300  $\mu$ s, Duty cycle < 2.0 %. 3. Starting T $_J$  = 25  $^o$ C; N-ch: L = 1 mH, I $_{AS}$  = 12 A, V $_{DD}$  = 90 V, V $_{GS}$  = 10 V. 4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

## Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

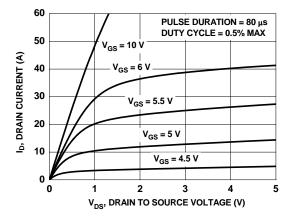


Figure 1. On-Region Characteristics

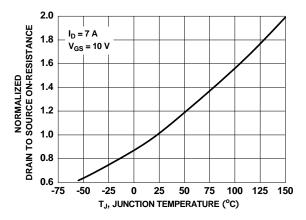


Figure 3. Normalized On-Resistance vs Junction Temperature

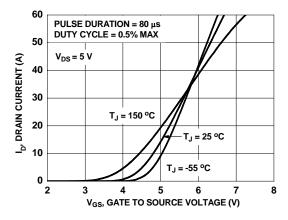


Figure 5. Transfer Characteristics

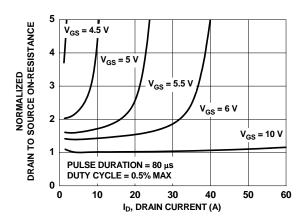


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

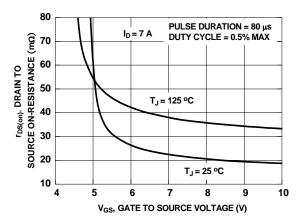


Figure 4. On-Resistance vs Gate to Source Voltage

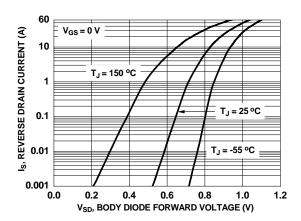


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

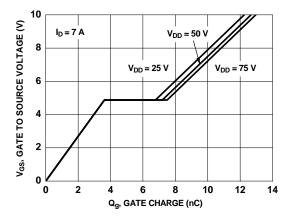


Figure 7. Gate Charge Characteristics

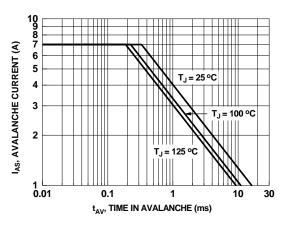


Figure 9. Unclamped Inductive Switching Capability

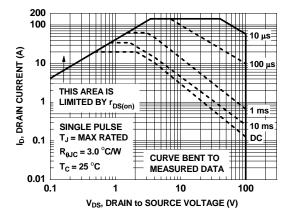


Figure 11. Forward Bias Safe Operating Area

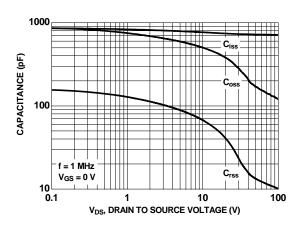


Figure 8. Capacitance vs Drain to Source Voltage

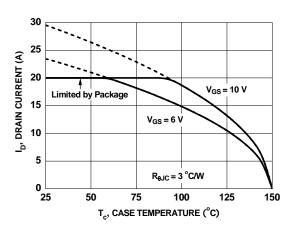


Figure 10. Maximum Continuous Drain Current vs Case Temperature

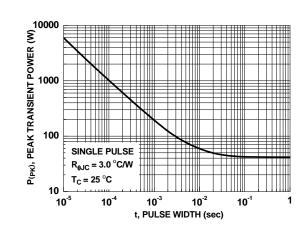


Figure 12. Single Pulse Maximum Power Dissipation

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

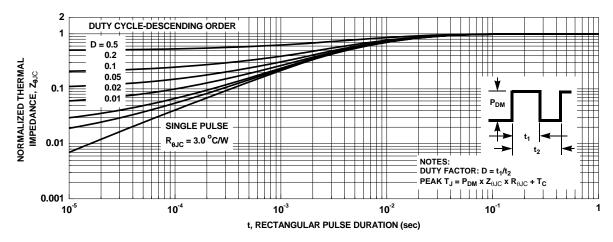
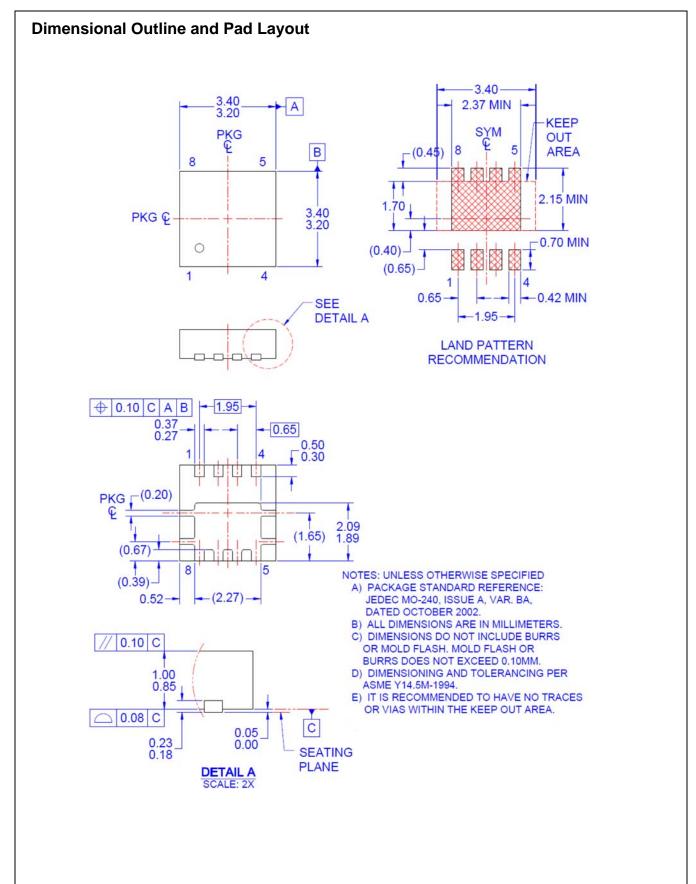


Figure 13. Transient Thermal Response Curve







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