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March 2008

FDMC8462

N-Channel Power Trench[®] MOSFET 40V, 20A, $5.8m\Omega$

Features

- Max $r_{DS(on)} = 5.8m\Omega$ at $V_{GS} = 10V$, $I_D = 13.5A$
- Max $r_{DS(on)} = 8.0 \text{m}\Omega$ at $V_{GS} = 4.5 \text{V}$, $I_D = 11.8 \text{A}$
- Low Profile 1mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

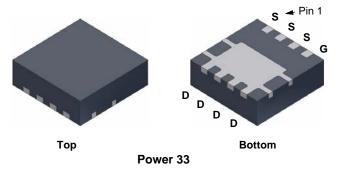


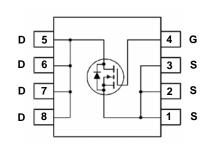
General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

■ DC - DC Conversion





$\textbf{MOSFET Maximum Ratings} \ T_{\text{A}} = 25^{\circ}\text{C unless otherwise noted}$

Symbol	Parameter	Parameter			
V _{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous (Package limited)	T _C = 25°C		20	
	-Continuous (Silicon limited)	T _C = 25°C		64	
ID	-Continuous	T _A = 25°C	(Note 1a)	14	A
	-Pulsed			50	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	216	mJ
Б	Power Dissipation $T_C = 25^{\circ}C$			41	W
P_{D}	Power Dissipation	T _A = 25°C	(Note 1a)	2.0	VV
T _J , T _{STG}	Operating and Storage Junction Temperature R	ange		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1	a) 53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8462	FDMC8462	Power 33	13"	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 250μA, referenced to 25°C		31		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0V, V_{DS} = 32V,$			1	μА
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-6.6		mV/°C
		$V_{GS} = 10V, I_D = 13.5A$		4.7	5.8	
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 11.8A$		6.4	8.0	mΩ
, ,		$V_{GS} = 10V$, $I_D = 13.5A$, $T_J = 125$ °C		7.1	9.3	
9 _{FS}	Forward Transconductance	$V_{DD} = 5V, I_D = 13.5A$		60		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 20V V 0V	2000	2660	pF
C _{oss}	Output Capacitance	$V_{DS} = 20V, V_{GS} = 0V,$ f = 1MHz	545	725	pF
C _{rss}	Reverse Transfer Capacitance	1 – 1111112	80	120	pF
R_{q}	Gate Resistance	f = 1MHz	2.7		Ω

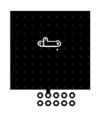
Switching Characteristics

t _{d(on)}	Turn-On Delay Time		12	21	ns
t _r	Rise Time	$V_{DD} = 20V, I_D = 13.5A,$	4	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10V, R_{GEN} = 6\Omega$	27	43	ns
t _f	Fall Time		3	10	ns
Q_g	Total Gate Charge	V _{GS} = 0V to 10V	30	43	nC
Qg	Total Gate Charge	$V_{GS} = 0V \text{ to } 4.5V$ $V_{DD} = 20V,$	15	21	nC
Q_{gs}	Gate to Source Charge	I _D = 13.5A	6		nC
Q_{gd}	Gate to Drain "Miller" Charge		5		nC

Drain-Source Diode Characteristics

	$V_{GS} = 0V, I_S = 13.5A$ (Note	2)	0.8	1.3	V	
V _{SD}	Source to Drain blode Forward voltage	$V_{GS} = 0V$, $I_S = 1.7A$ (Note	2)	0.7	1.2	V
t _{rr}	Reverse Recovery Time	-I _F = 13.5A, di/dt = 100A/μs		35	57	ns
Q _{rr}	Reverse Recovery Charge	- I _F = 13.5A, α/αι = 100A/μS		20	32	nC

^{1.} R_{0,1} is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,1} is guaranteed by design while R_{0,2} is determined by the user's board design.



a. 53°C/W when mounted on a 1 in² pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < $300\mu s$, Duty cycle < 2.0%.
- 3. Starting $T_J = 25^{\circ}C$; N-ch: L = 3 mH, $I_{AS} = 12A$, $V_{DD} = 40V$, $V_{GS} = 10V$

Typical Characteristics $T_J = 25$ °C unless otherwise noted

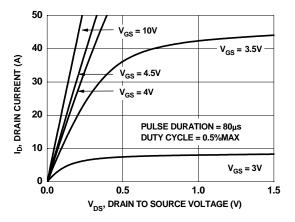


Figure 1. On-Region Characteristics

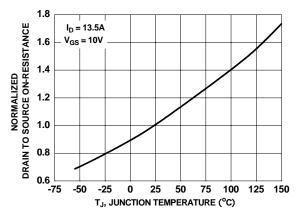


Figure 3. Normalized On-Resistance vs Junction Temperature

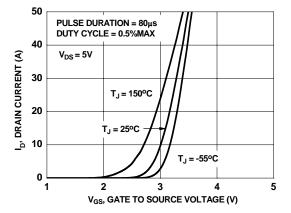


Figure 5. Transfer Characteristics

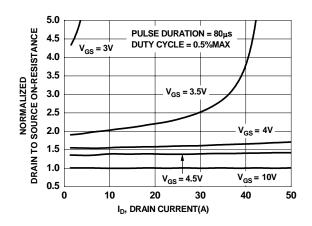


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

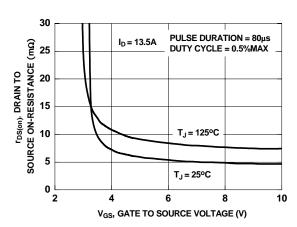


Figure 4. On-Resistance vs Gate to Source Voltage

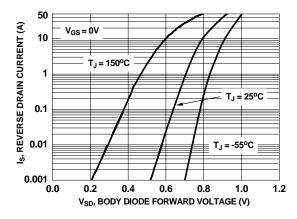


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

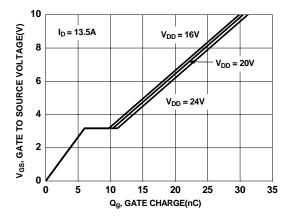


Figure 7. Gate Charge Characteristics

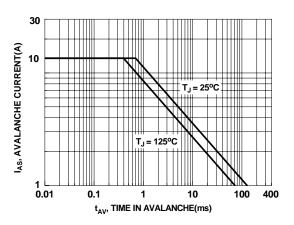


Figure 9. Unclamped Inductive Switching Capability

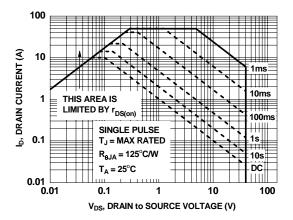


Figure 11. Forward Bias Safe Operating Area

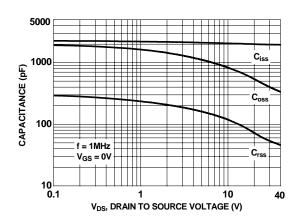


Figure 8. Capacitance vs Drain to Source Voltage

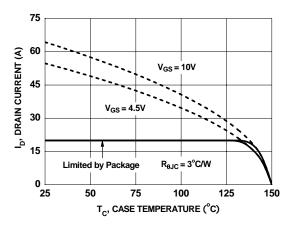


Figure 10. Maximum Continuous Drain Current vs Case Temperature

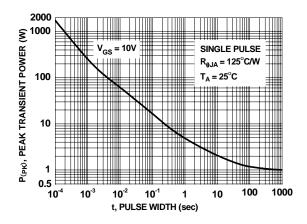


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

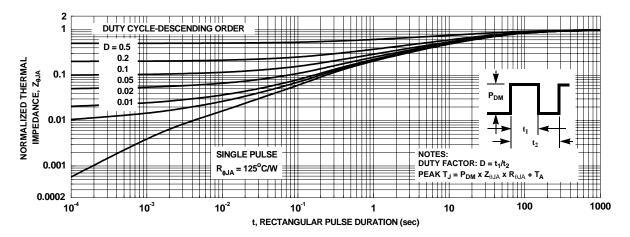


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout $-3.30\pm0.10-$ 2.37 MIN SYM PKG Ė -(0.45) 8 5 2.15 MIN (0.40)PKG Q-PKGQ 3.30 ± 0.10 (0.65) \bigcirc 0.70 MIN 4 1 0.65 -0.42 MIN SEE DETAIL A 1.95 LAND PATTERN RECOMMENDATION 1.95 0.65 0.32±0.05-⊕ 0.10 C A B -0.40 ± 0.10 (0.20)PKGÇ 2.00 ± 0.10 (0.39)8 5 (2.27) — NOTES: UNLESS OTHERWISE SPECIFIED (0.52)-PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002. 0.10 C ALL DIMENSIONS ARE IN MILLIMETERS. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR 1.10 BURRS DOES NOT EXCEED 0.10MM. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. DRAWING FILE NAME: PQFN08BREV1 \triangle 0.08 C 0.05 С 0.20 ± 0.025 **SEATING** PLANE DETAIL A PQFN08BREV1





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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I34

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