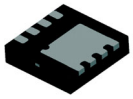
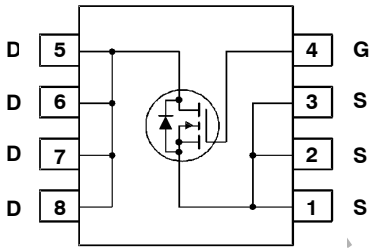
MOSFET – Power, N-Channel, UltraFET

55 V, 15 A, 90 mΩ

FDMC15N06



WDFN8 3.3X3.3, 0.65P
CASE 511DQ



Description

These N−Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on−resistance per silicon area, resulting in outstanding performance.

This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low voltage bus switches, and power management in portable and battery−operated products.

Features

- $R_{DS(on)}$ = 75 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 15 A
- 100% Avalanche Tested
- These Device is Pb−Free and RoHS Compliant

MARKING DIAGRAM

Z = Assembly Plant Code
XY = Date Code (Year & Week)
KK = Lot Traceability Code
15N06 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMC15N06	WDFN8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	55	V
V_{GSS}	Gate to Source Voltage	±20	V
I_D	Drain Current –Continuous (T_C= 25°C) –Continuous (T_C = 100°C) –Continuous (T_A = 25°C) (Note 1)	 15 9 2.4	A
I_{DM}	Drain Current –Pulsed (Note 2)	60	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	36	mJ
I_{AR}	Avalanche Energy	15	A
E_{AR}	Repetitive Avalanche Energy	3.5	mJ
P_D	Power Dissipation (T_C= 25°C) (T_A = 25°C)	 35 2.3	W
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max (Note 1)	53	

ELECTRICAL CHARACTERISTICS Tc = 25 °C unless otherwise noted.

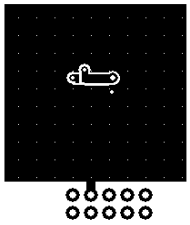
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_C = 25 °C	55	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	70	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V V_{DS} = 45 V, T_C = 150 °C	– –	– –	1 250	μA
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 15 A	–	0.075	0.090	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 15 A	–	5	–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	265	350	pF
C_{oss}	Output Capacitance		–	97	130	pF
C_{rss}	Reverse Transfer Capacitance		–	28	42	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 30 V, I_D = 15 A, V_{GS} = 10 V (Note 4)	–	8.8	11.5	nC
Q_{gs}	Gate to Source Gate Charge		–	1.7	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	3.6	–	nC

ELECTRICAL CHARACTERISTICS Tc = 25 °C unless otherwise noted.(continued)

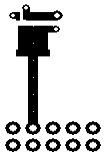
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Switching Characteristics						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 30 V, I_D = 15 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	–	9.5	29	ns
t_r	Turn−On Rise Time		–	36.5	83	ns
$t_{d(off)}$	Turn−Off Delay Time		–	22.5	55	ns
t_f	Turn−Off Fall Time		–	22	54	ns
Drain−Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	15	A
			–	–	60	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	1.25	V
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 15 A				
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 15 A, dI_F/dt = 100 A/μs (Note 5)	–	30	–	ns
Q_{rr}	Reverse Recovery Charge		–	35	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR−4 material $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

2. Repetitive rating: pulse−width limited by maximum junction temperature.
3. L = 1 mH, I_{AS} = 8.5 A, R_G = 25 Ω, starting TJ = 25°C.
4. Essentially independent of operating temperature typical characteristics.
5. I_{SD} ≤ 15 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 40 V, starting T_J = 25°C.

TYPICAL CHARACTERISTICS

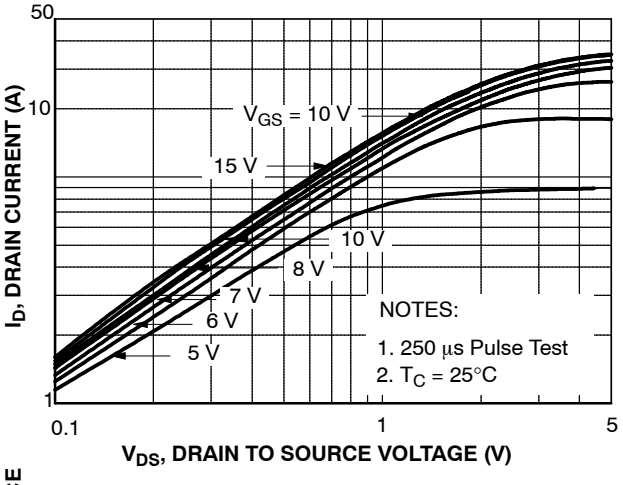


Figure 1. On−Region Characteristics

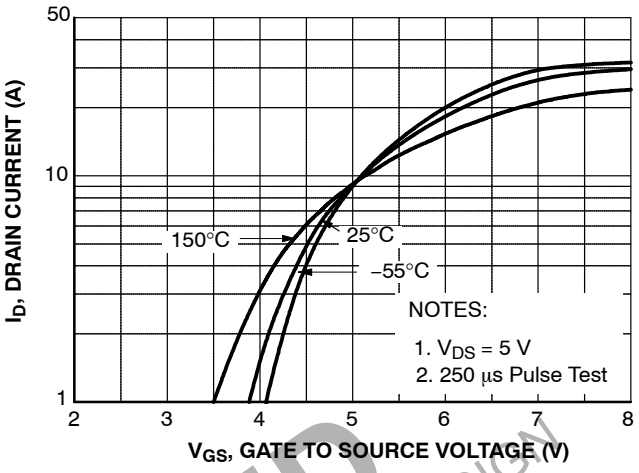


Figure 2. Transfer Characteristics

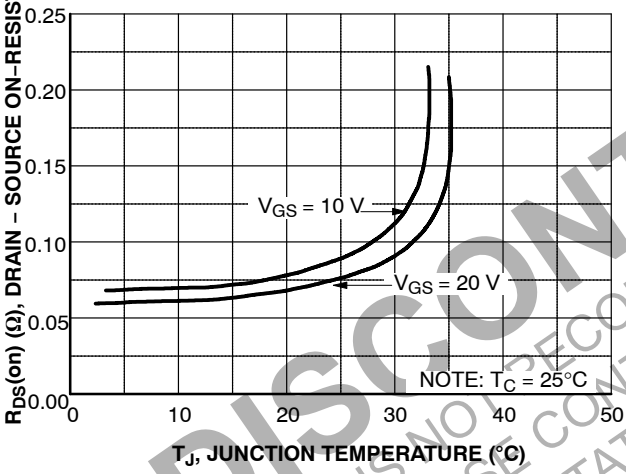


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

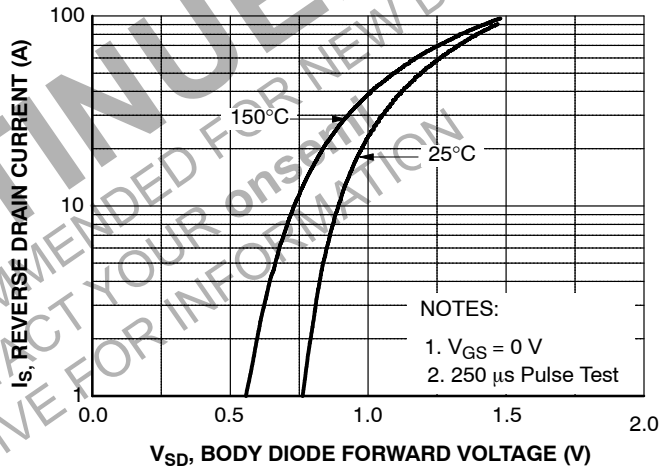


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

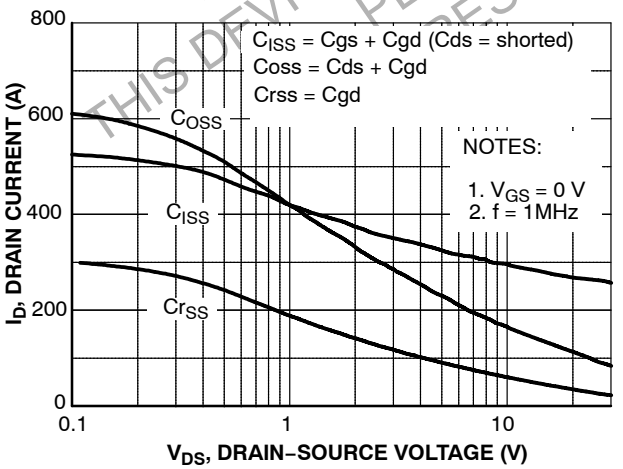


Figure 5. Capacitance Characteristics

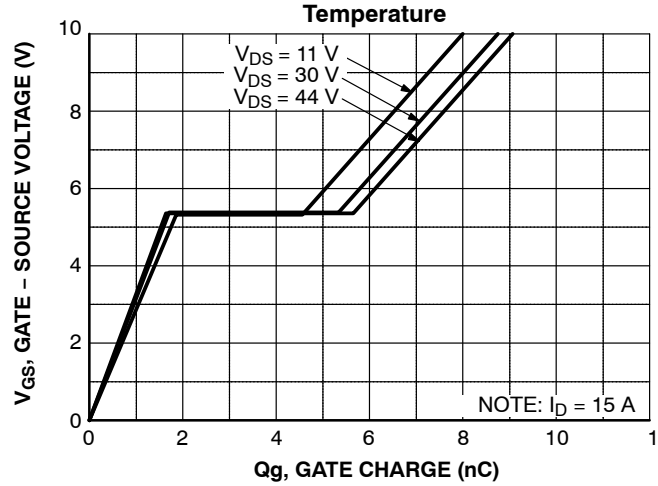


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

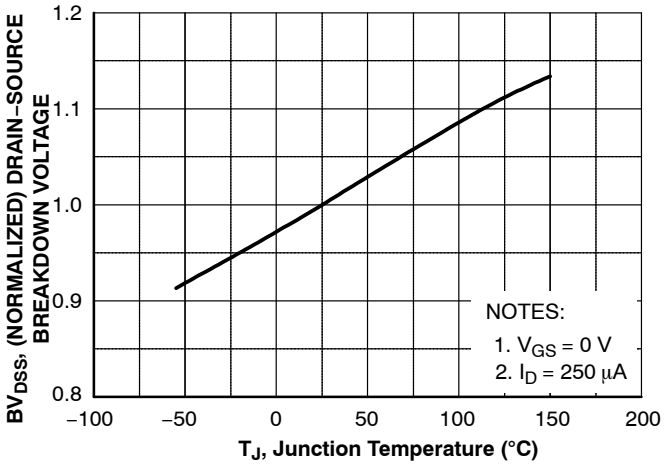


Figure 7. Breakdown Voltage Variation vs. Temperature

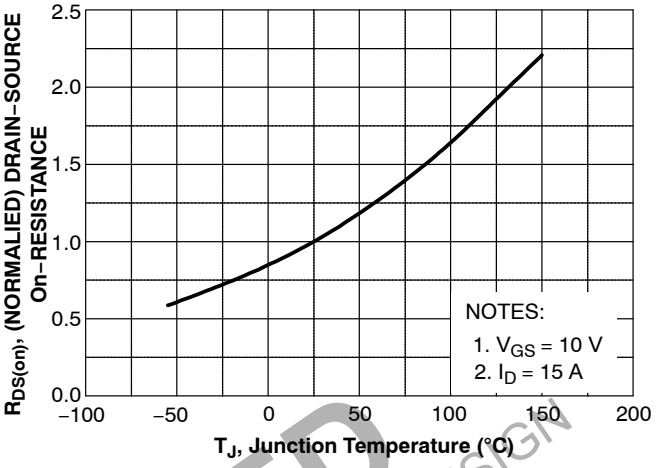


Figure 8. On–Resistance Variation vs. Temperature

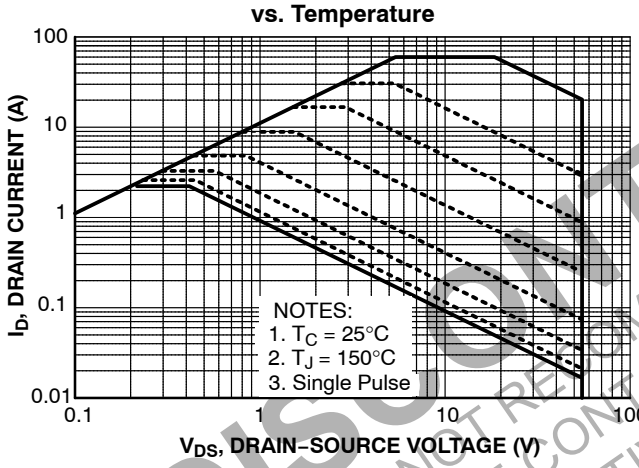


Figure 9. Unclamped Inductive Switching Capability

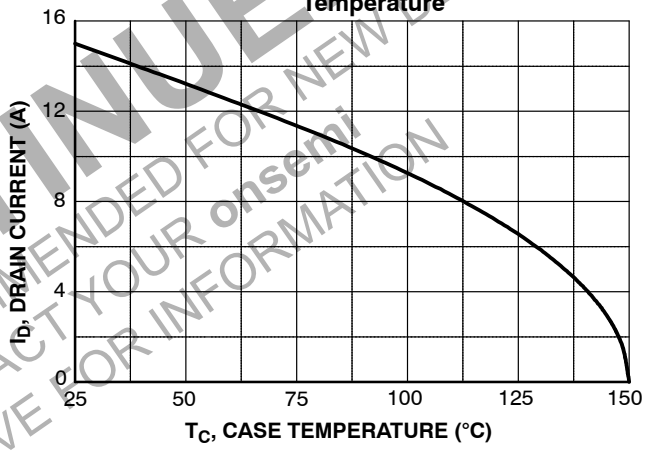


Figure 10. Maximum Drain Current vs. Case Temperature

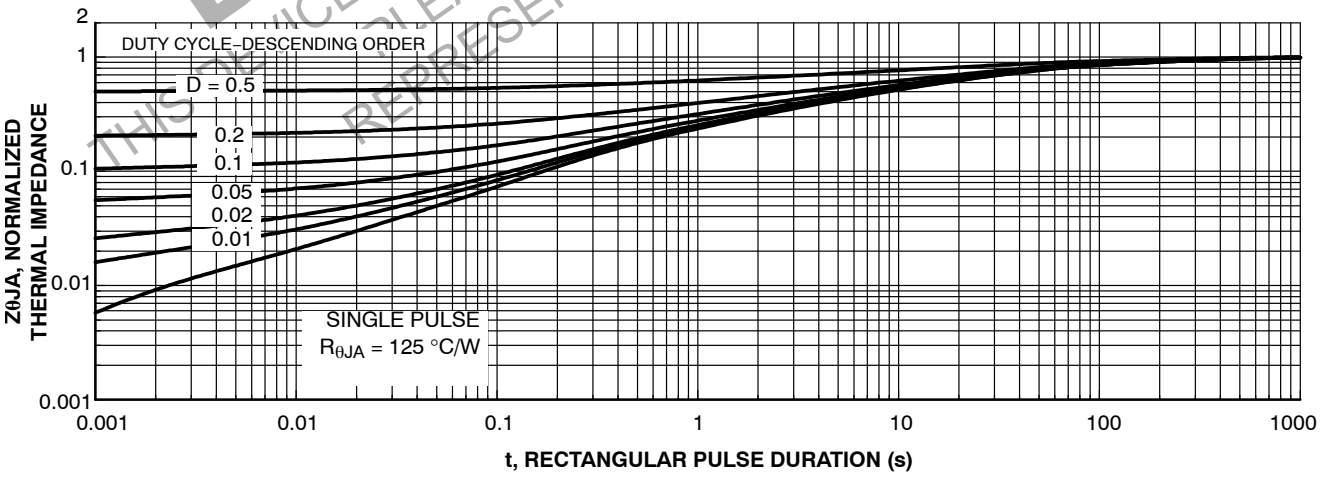


Figure 11. Thermal Response Curve

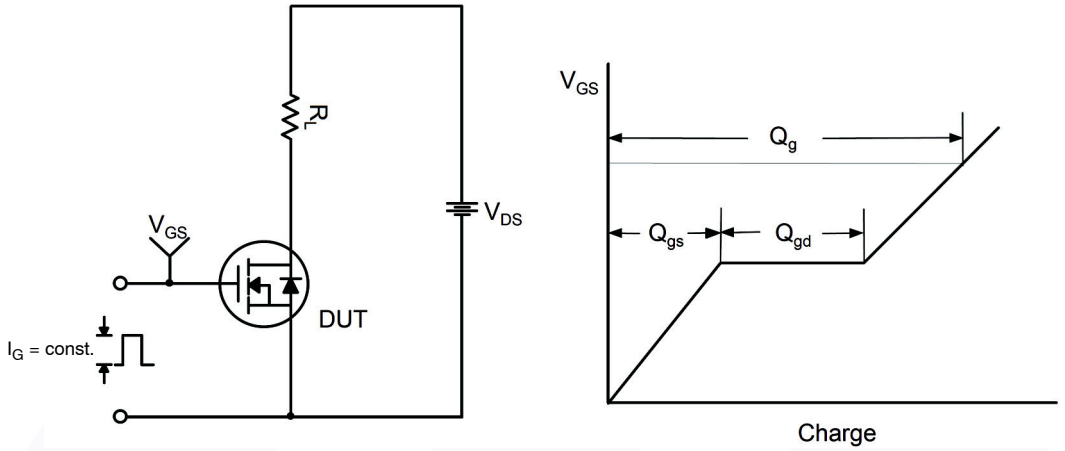


Figure 12. Gate Charge Test Circuit & Waveform

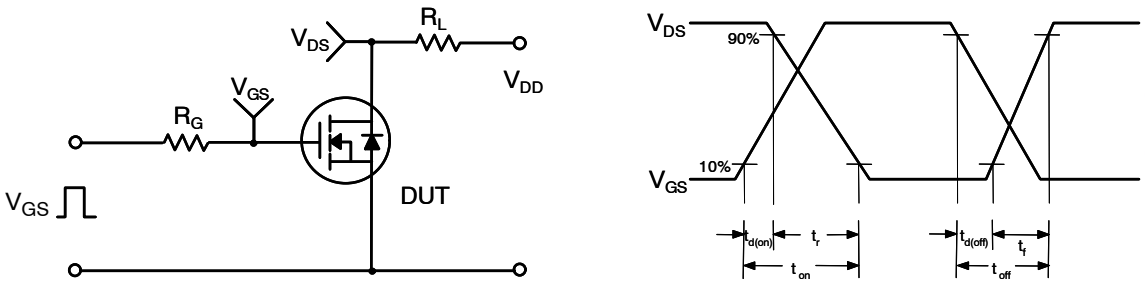


Figure 13. Resistive Switching Test Circuit & Waveforms

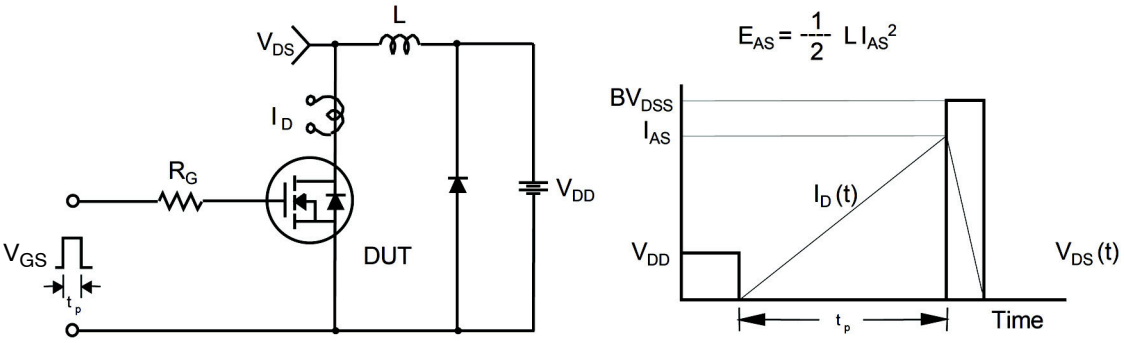


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

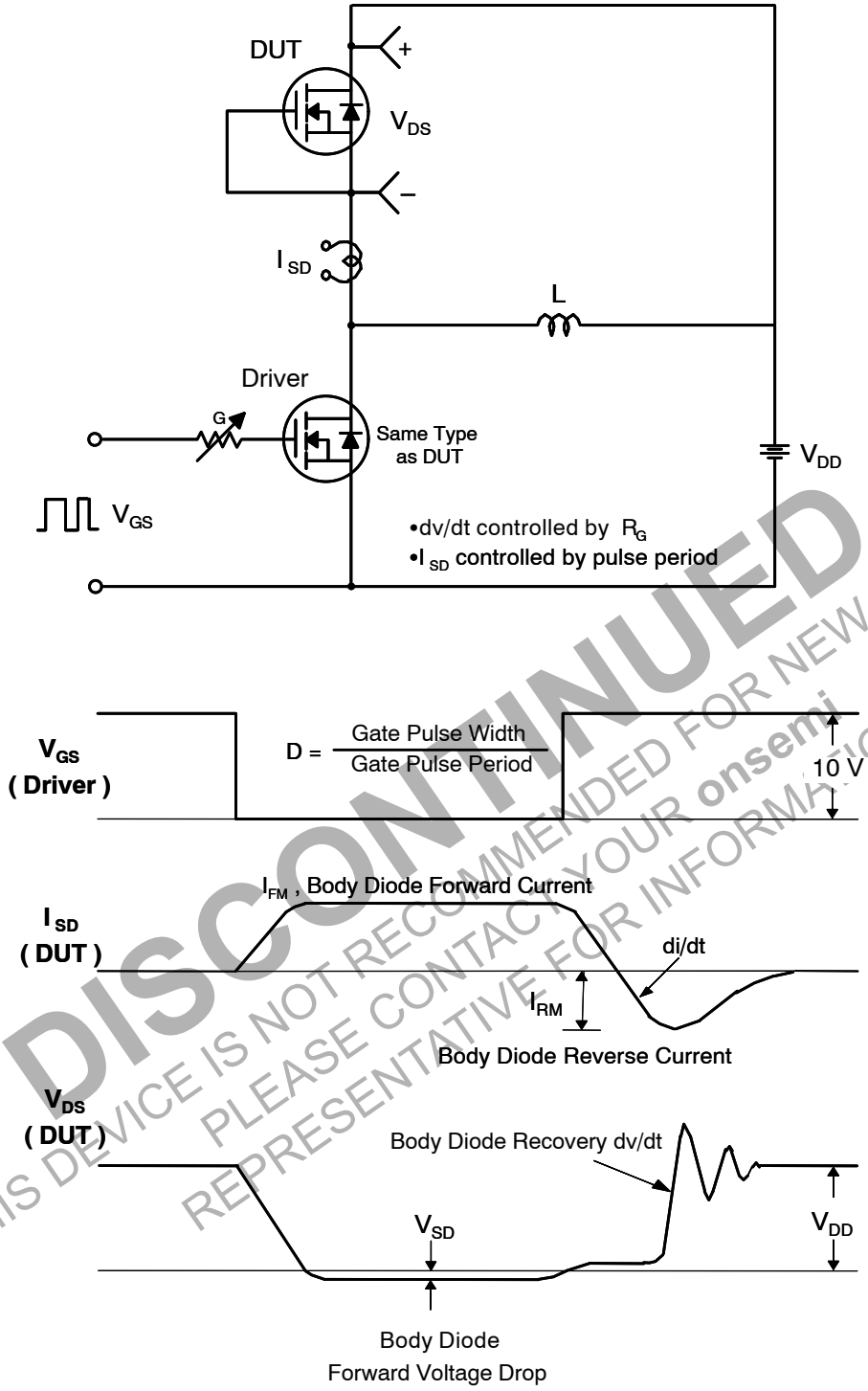


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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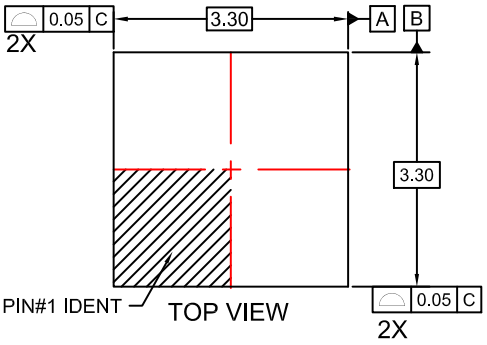

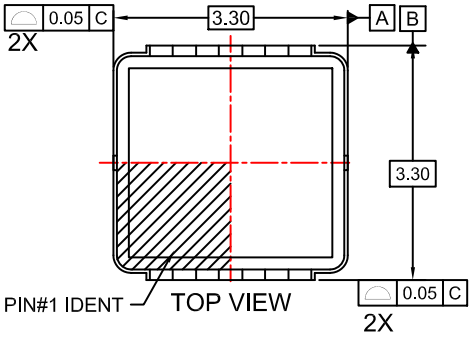

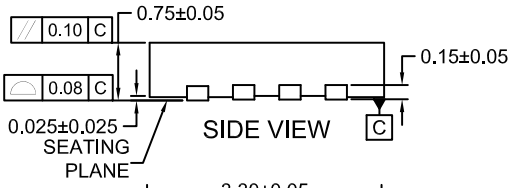

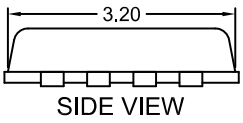

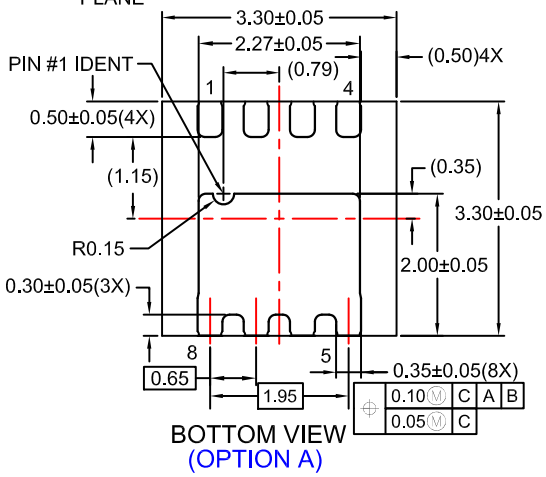

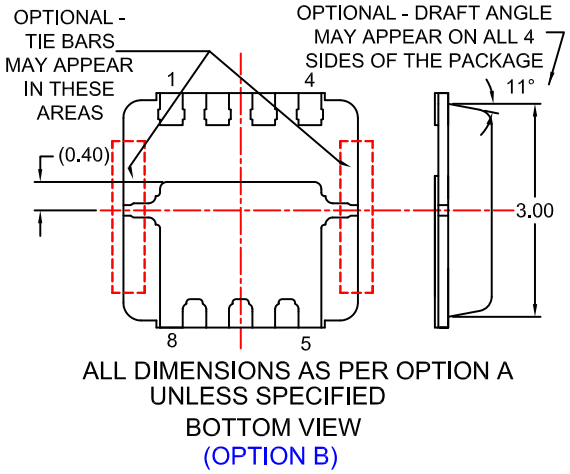

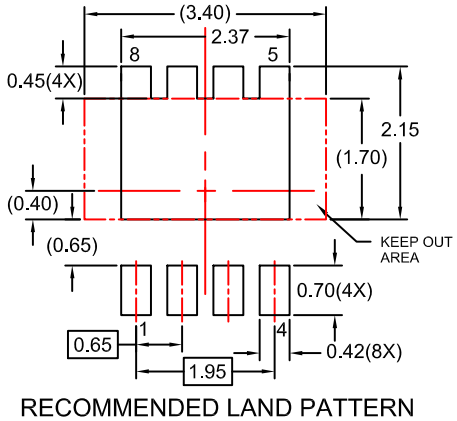

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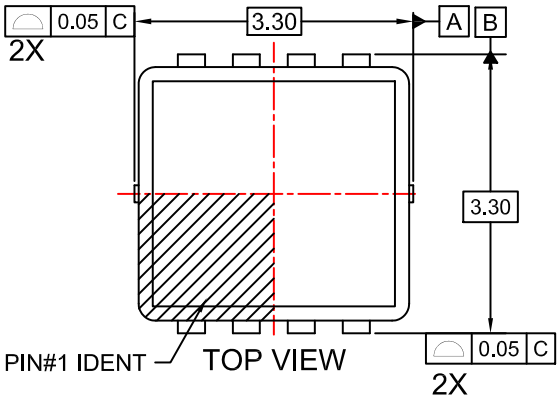
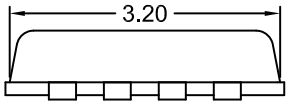
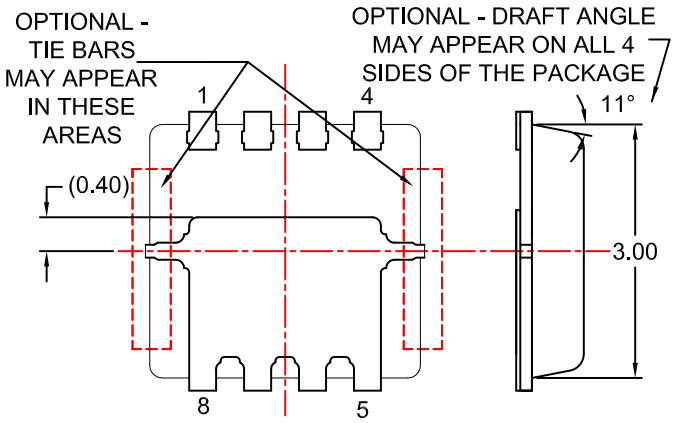




SIDE VIEW



ALL DIMENSIONS AS PER OPTION A UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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