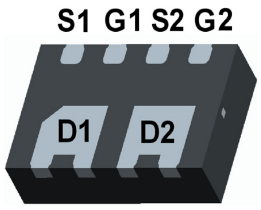
MOSFET – Dual, N-Channel, POWERTRENCH®

30 V, 4.8 A, 40 mΩ

FDMB3800N

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
30 V	40 mΩ @ 4.8 V	4.8 A
	51 mΩ @ 4.3 V	



WDFN8 3x1.9, 0.65P
(MicroFET 3x1.9)
CASE 511CW

General Description

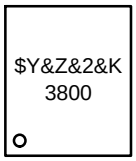
These N−Channel Logic Level MOSFETs are produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in−line power loss and fast switching are required.

Features

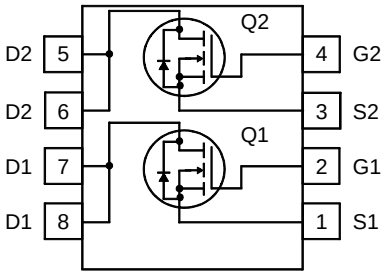
- Max $r_{DS(on)}$ = 40 mΩ at V_{GS} = 10 V, I_D = 4.8 A
- Max $r_{DS(on)}$ = 51 mΩ at V_{GS} = 4.5 V, I_D = 4.3 A
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MARKING DIAGRAM



$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
3800 = Specific Device Code

PIN ASSIGNMENT



MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current − Continuous T_A = 25°C (Note 1a) − Pulsed	 4.8 9	A
P_D	Power Dissipation T_A = 25°C (Note 1a) T_A = 25°C (Note 1b)	 1.6 0.75	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	165	

ORDERING INFORMATION

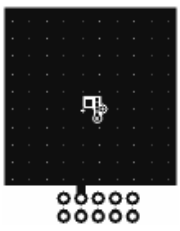
See detailed ordering and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

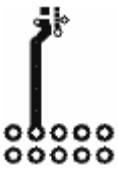
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	24	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C	–	–	10	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−4	–	mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4.8 A	–	32	40	mΩ
		V_{GS} = 4.5 V, I_D = 4.3 A	–	41	51	
		V_{GS} = 10 V, I_D = 4.8 A, T_J = 125°C	–	43	61	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 4.8 A	–	14	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} =15 V, V_{GS} = 0 V, f = 1 MHz	–	350	465	pF
C_{oss}	Output Capacitance		–	90	120	pF
C_{rss}	Reverse Transfer Capacitance		–	40	60	pF
R_g	Gate Resistance	f = 1 MHz	–	3	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	8	16	ns
t_r	Rise Time		–	5	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	21	34	ns
t_f	Fall Time		–	2	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 5 V	V_{GS} = 0 V to 5 V, V_{DD} = 15 V, I_D = 7.5 A	–	4	5.6	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 15 V, I_D = 7.5 A	–	1.0	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	1.5	–	nC
DRAIN−SOURCE CHARACTERISTICS						
I_S	Maximum Continuous Drain − Source Diode Forward Current		–	–	1.25	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 4.8 A, di/dt = 100 A/μs	–	17	–	ns
Q_{rr}	Reverse Recovery Charge		–	7	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 80°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 165°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

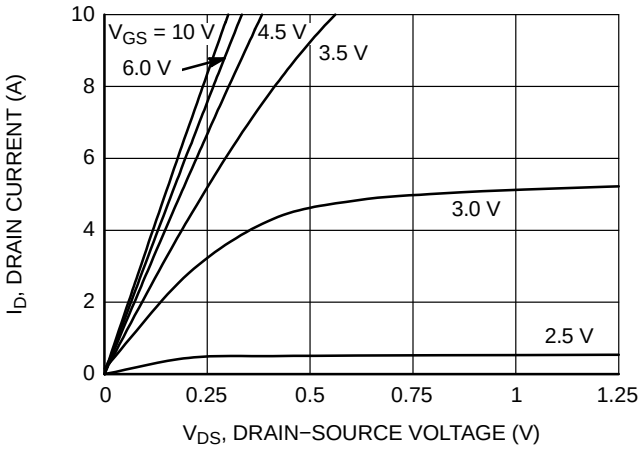


Figure 1. On Region Characteristics

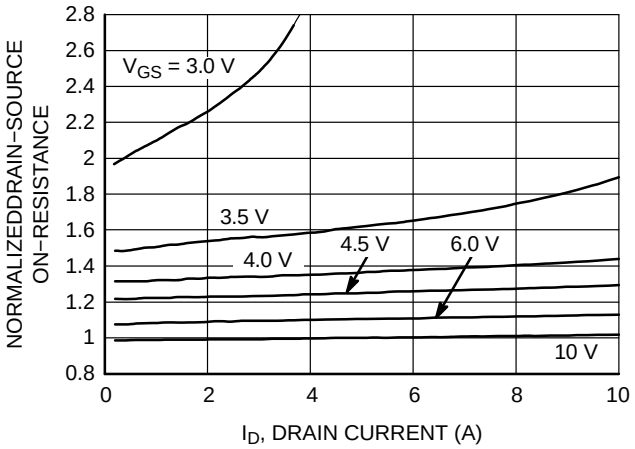


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

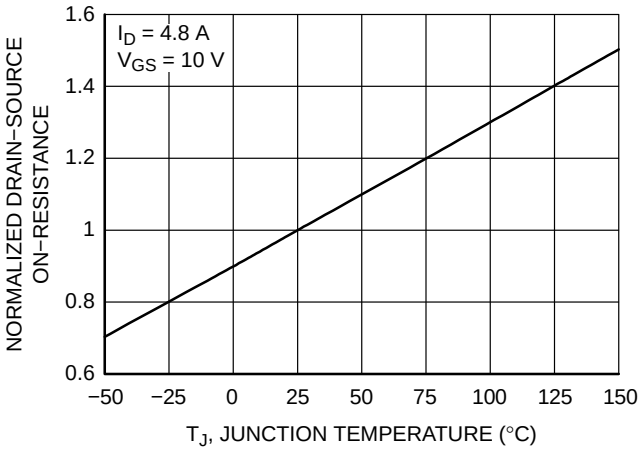


Figure 3. Normalized On−Resistance vs. Junction Temperature

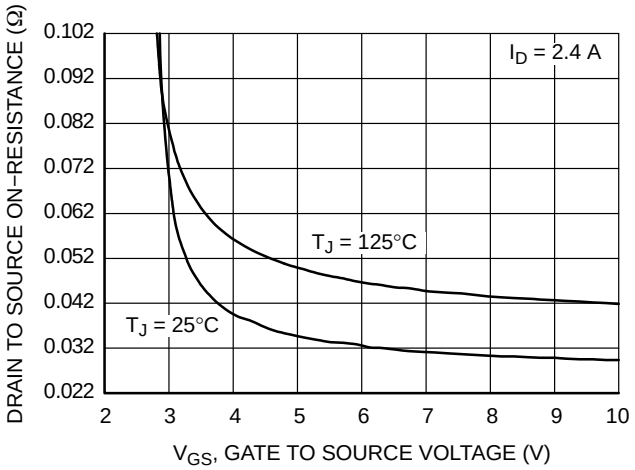


Figure 4. On−Resistance vs. Gate to Source Voltage

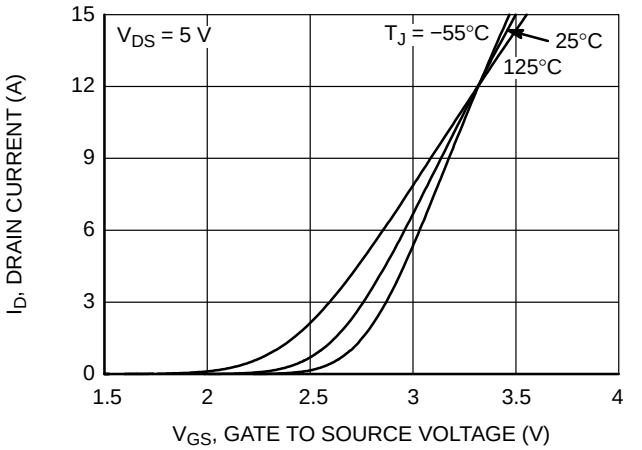


Figure 5. Transfer Characteristics

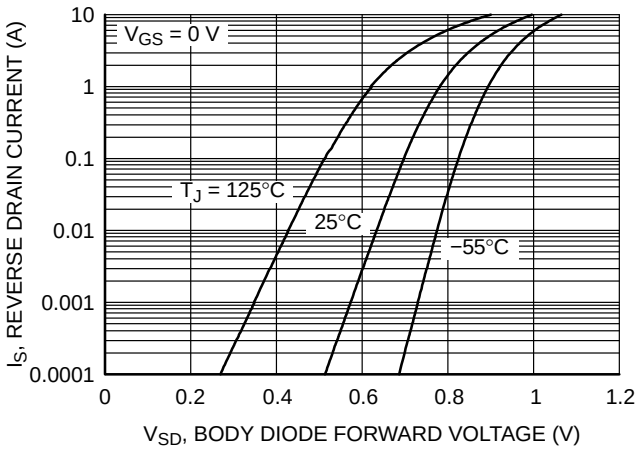


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

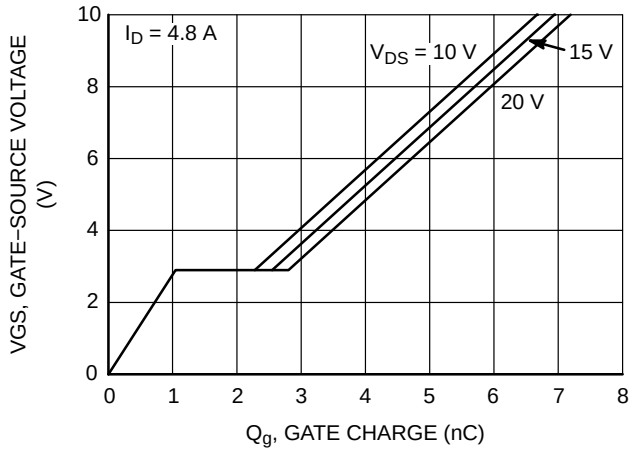


Figure 7. Gate Charge Characteristics

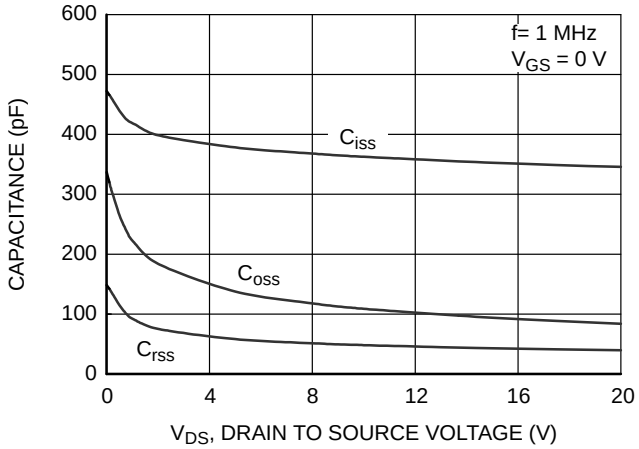


Figure 8. Capacitance vs. Drain to Source Voltage

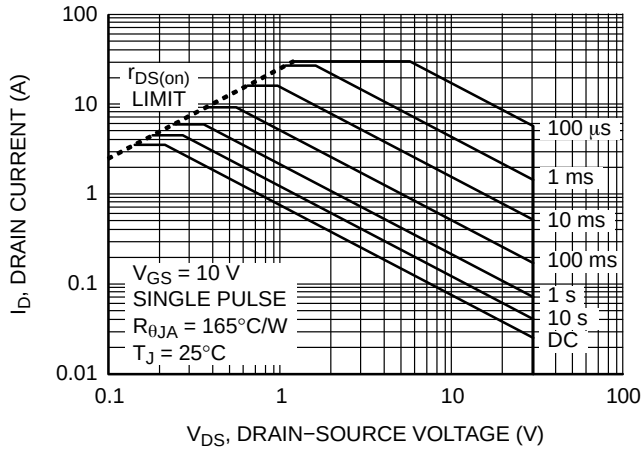


Figure 9. Forward Bias Safe Operating Area

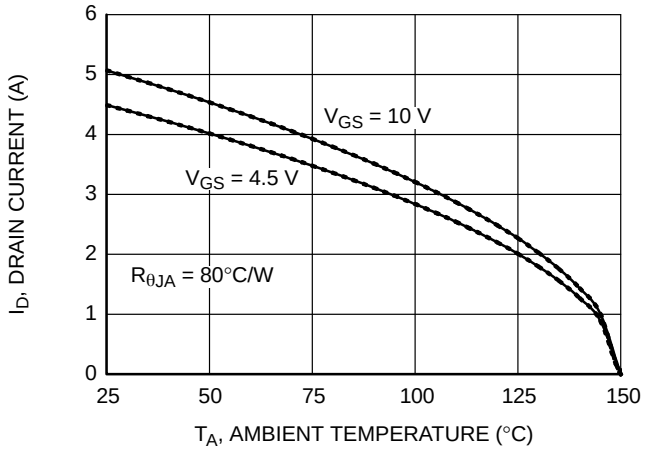


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

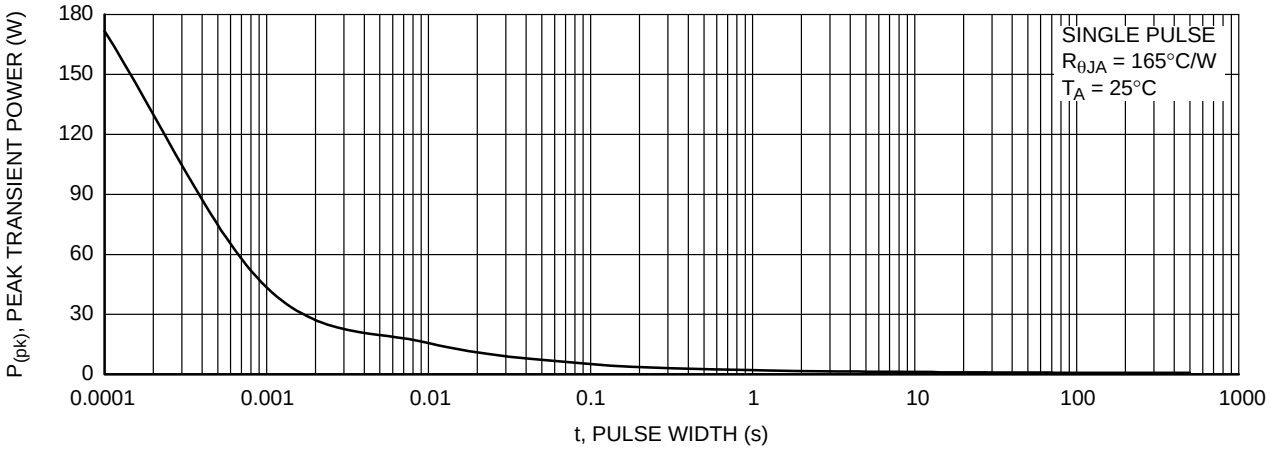


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

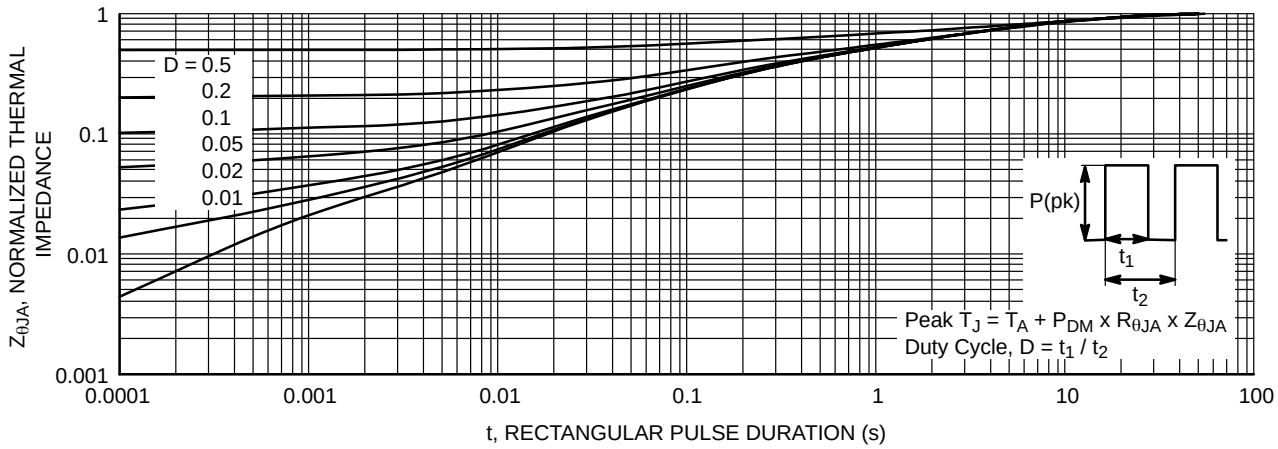


Figure 12. Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMB3800N	3800	WDFN8 3x1.9, 0.65P (MicroFET 3x1.9) (Pb−Free, Halide Free)	7”	8 mm	3000 / Tape & Reel

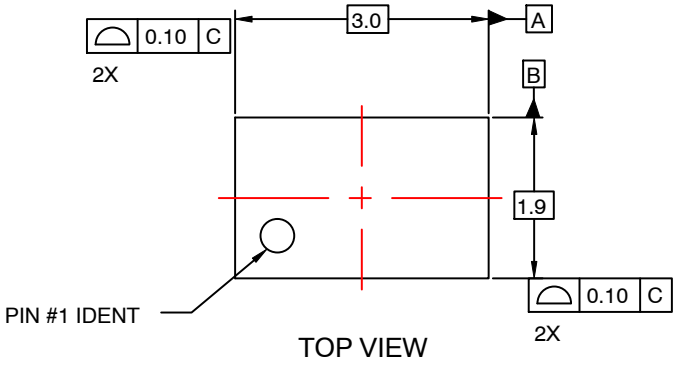
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

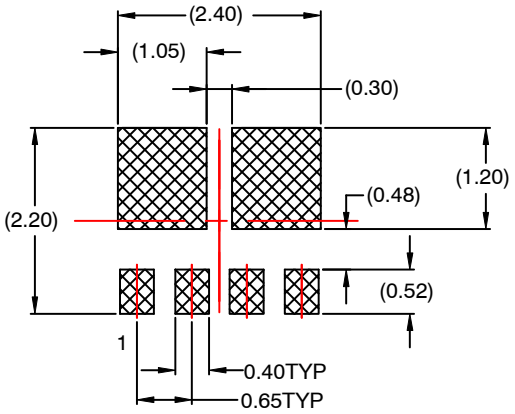
ON Semiconductor®

WDFN8 3x1.9, 0.65P
CASE 511CW
ISSUE O

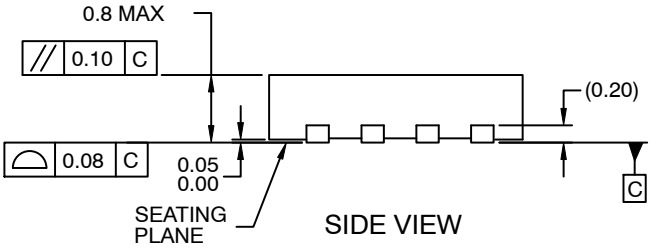
DATE 31 JUL 2016



TOP VIEW



RECOMMENDED LAND PATTERN



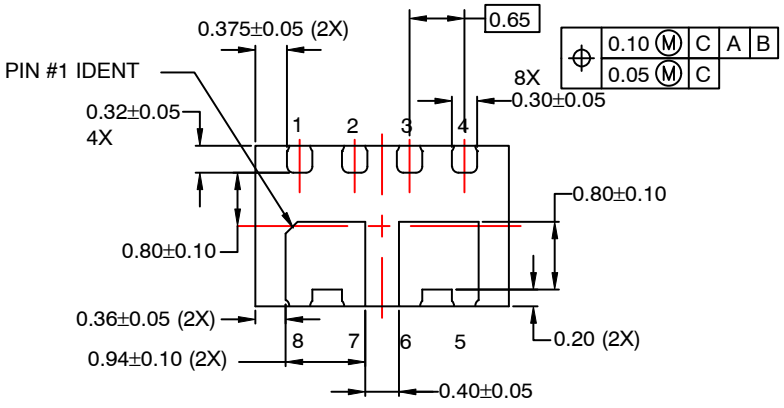
SIDE VIEW

NOTES:

A. DOES NOT FULLY CONFORM TO JEDED REGISTRATION MO−229.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.



BOTTOM VIEW

DOCUMENT NUMBER:	**98AON13611G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**WDFN8 3X1.9, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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