# Digital FET, Dual N & P Channel

# FDG6320C

**ON Semiconductor®**

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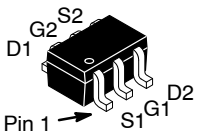



**SC−88/SC70−6/SOT−363**
**CASE 419B−02**

### General Description

These dual N & P−Channel logic level enhancement mode field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology, this very high density process is especially tailored to minimize on−state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETS. Since bias resistors are not required, this dual digital FET can replace several different digital transistors, with different bias resistor values.

### Features

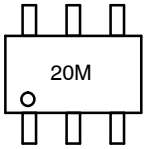
- N−Ch 0.22 A, 0.25 V
  - $R_{DS(ON)}$ = 4.0 Ω @ $V_{GS}$ = 4.5 V
  - $R_{DS(ON)}$ = 5.0 Ω @ $V_{GS}$ = 2.7 V
- P−Ch −0.14 A, −25 V
  - $R_{DS(ON)}$ = 10 Ω @ $V_{GS}$ = −4.5 V
  - $R_{DS(ON)}$ = 13 Ω @ $V_{GS}$ = −2.7 V
- Very Small Package Outline SC70−6
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits ($V_{GS(th)}$ < 1.5 V)
- Gate−Source Zener for ESD Ruggedness (>6 kV Human Body Model)
- These Devices are Pb−Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | | N−Channel | P−Channel | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | | 25 | −25 | V |
| $V_{GSS}$ | Gate−Source Voltage | | 8 | −8 | V |
| $I_D$ | Drain Current | Continuous | 0.22 | −0.14 | A |
| | | Pulsed | 0.65 | −0.4 | |
| $P_D$ | Maximum Power Dissipation (Note 1) | | 0.3 | | W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | −55 to 150 | | °C |
| ESD | Electrostatic Discharge Rating MIL−STD−883D Human Body Model (100 pF / 1500 Ω) | | 6 | | kV |

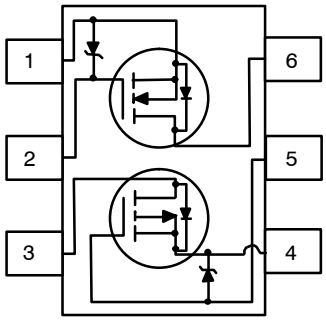
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### MARKING DIAGRAM




20 = Specific Device Code
M = Assembly Operation Month

### PIN CONNECTIONS




### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient (Note 1) | 415 | °C/W |

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W on minimum pad mounting on FR−4 board in still air.

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Type | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| $BV_{DSS}$ | Drain−Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | N−Ch | 25 | – | – | V |
| | | $V_{GS}$ = 0 V, $I_D$ = −250 μA | P−Ch | −25 | – | – | |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | N−Ch | – | 25 | – | mV/°C |
| | | $I_D$ = −250 μA, Referenced to 25°C | P−Ch | – | −19 | – | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | N−Ch | – | – | 1 | μA |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | | – | – | 10 | |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = −20 V, $V_{GS}$ = 0 V | P−Ch | – | – | −1 | μA |
| | | $V_{DS}$ = −20 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | | – | – | −10 | |
| $I_{GSS}$ | Gate−Body Leakage Current | $V_{GS}$ = 8 V, $V_{DS}$ = 0 V | N−Ch | – | – | 100 | nA |
| | | $V_{GS}$ = −8 V, $V_{DS}$ = 0 V | P−Ch | – | – | −100 | |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | N−Ch | 0.65 | 0.85 | 1.5 | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = −250 μA | P−Ch | −0.65 | −0.82 | −1.5 | |
| $\Delta V_{GS(th)}$ / $\Delta T_J$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | N−Ch | – | −2.1 | – | mV/°C |
| | | $I_D$ = −250 μA, Referenced to 25°C | P−Ch | – | 2.1 | – | |
| $R_{DS(ON)}$ | Static Drain−Source On−Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 0.22 A | N−Ch | – | 2.6 | 4 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 0.22 A, $T_J$ = 125°C | | – | 5.3 | 7 | |
| | | $V_{GS}$ = 2.7 V, $I_D$ = 0.19 A | | – | 3.7 | 5 | |
| | | $V_{GS}$ = −4.5 V, $I_D$ = −0.14 A | P−Ch | – | 7.3 | 10 | |
| | | $V_{GS}$ = −4.5 V, $I_D$ = −0.14 A, $T_J$ = 125°C | | – | 11 | 17 | |
| | | $V_{GS}$ = −2.7 V, $I_D$ = −0.05 A | | – | 10.4 | 13 | |
| $I_{D(ON)}$ | On−State Drain Current | $V_{GS}$ = 4.5 V, $V_{DS}$ = 5 V | N−Ch | 0.22 | – | – | A |
| | | $V_{GS}$ = −4.5 V, $V_{DS}$ = −5 V | P−Ch | −0.14 | – | – | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 0.22 A | N−Ch | – | 0.2 | – | S |
| | | $V_{DS}$ = −5 V, $I_D$ = −0.14 A | P−Ch | – | 0.12 | – | |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $C_{iss}$ | Input Capacitance | N−Channel $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz<br>P−Channel $V_{DS}$ = −10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | N−Ch | – | 9.5 | – | pF |
| | | | P−Ch | – | 12 | – | |
| $C_{oss}$ | Output Capacitance | | N−Ch | – | 6 | – | |
| | | | P−Ch | – | 7 | – | |
| $C_{rss}$ | Reverse Transfer Capacitance | | N−Ch | – | 1.3 | – | |
| | | | P−Ch | – | 1.5 | – | |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (continued)

| Symbol | Parameter | Conditions | Type | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | | |
| $t_{D(on)}$ | Turn-On Delay Time | N−Channel<br>$V_{DD}$ = 5 V, $I_D$ = 0.5 A,<br>$V_{GS}$ = 4.5 V, $R_{GEN}$ = 50 Ω<br><br>P−Channel<br>$V_{DD}$ = −5 V, $I_D$ = −0.5 A,<br>$V_{GS}$ = −4.5 V, $R_{GEN}$ = 50 Ω | N−Ch | − | 5 | 12 | ns |
| | | | P−Ch | − | 5 | 12 | |
| $t_r$ | Turn-On Rise Time | | N−Ch | − | 4.5 | 10 | ns |
| | | | P−Ch | − | 8 | 16 | |
| $t_{D(off)}$ | Turn-Off Delay Time | | N−Ch | − | 4 | 8 | ns |
| | | | P−Ch | − | 9 | 18 | |
| $t_f$ | Turn-Off Fall Time | | N−Ch | − | 3.2 | 7 | ns |
| | | | P−Ch | − | 5 | 12 | |
| $Q_g$ | Total Gate Charge | N−Channel<br>$V_{DS}$ = 5 V, $I_D$ = 0.22 A,<br>$V_{GS}$ = 4.5 V<br><br>P−Channel<br>$V_{DS}$ = −5 V, $I_D$ = −0.14 A,<br>$V_{GS}$ = −4.5 V | N−Ch | − | 0.29 | 0.4 | nC |
| | | | P−Ch | − | 0.22 | 0.31 | |
| $Q_{gs}$ | Gate−Source Charge | | N−Ch | − | 0.12 | − | nC |
| | | | P−Ch | − | 0.12 | − | |
| $Q_{gd}$ | Gate−Drain Charge | | N−Ch | − | 0.03 | − | nC |
| | | | P−Ch | − | 0.05 | − | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | | |
| $I_S$ | Maximum Continuous Source Current | | N−Ch | − | − | 0.25 | A |
| | | | P−Ch | − | − | −0.25 | |
| $V_{SD}$ | Drain−Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 0.5 A (Note 2) | N−Ch | − | 0.8 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = −0.5 A (Note 2) | P−Ch | − | −0.8 | −1.2 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

## TYPICAL PERFORMANCE CHARACTERISTICS: N−CHANNEL

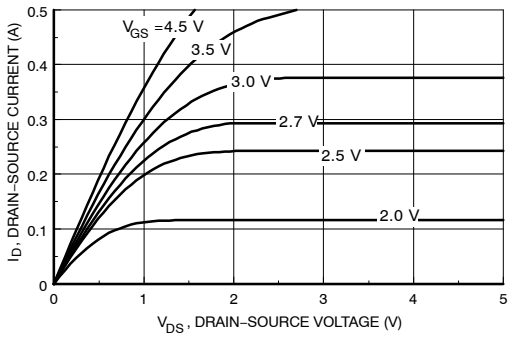



**Figure 1. On−Region Characteristics**

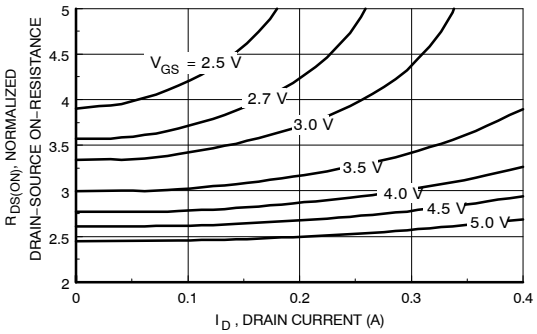



**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

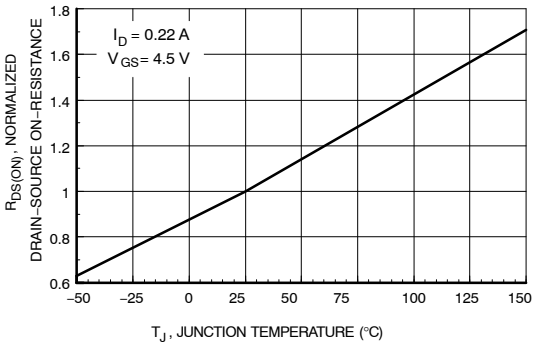



**Figure 3. On−Resistance Variation with Temperature**

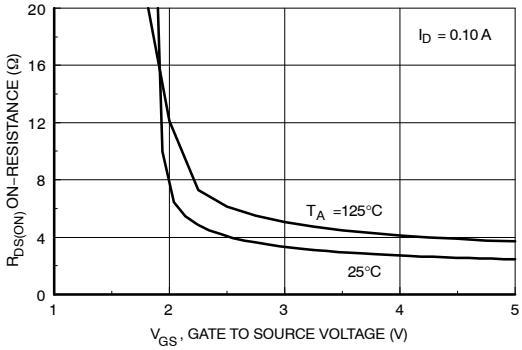



**Figure 4. On−Resistance Variation with Gate−to−Source Voltage**

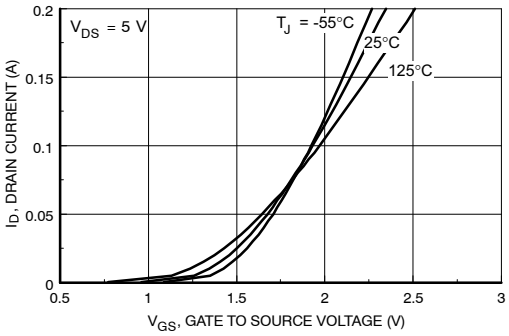



**Figure 5. Transfer Characteristics**

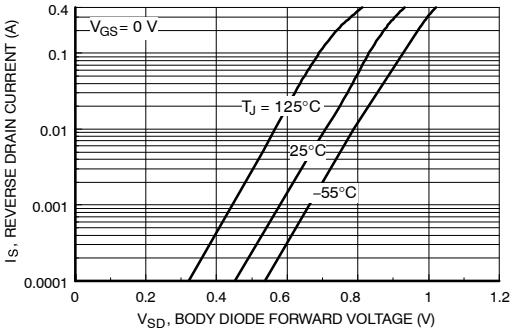



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## TYPICAL PERFORMANCE CHARACTERISTICS: N−CHANNEL (continued)

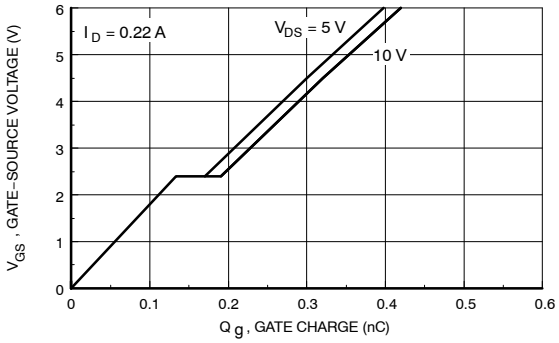



**Figure 7. Gate Charge Characteristics**

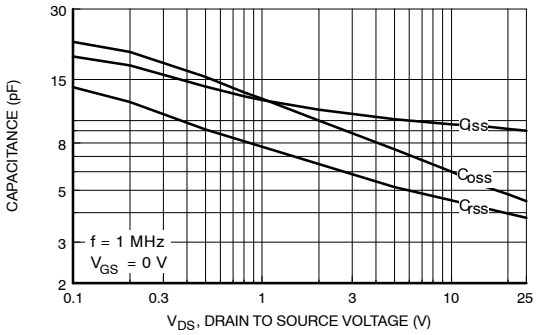



**Figure 8. Capacitance Characteristics**

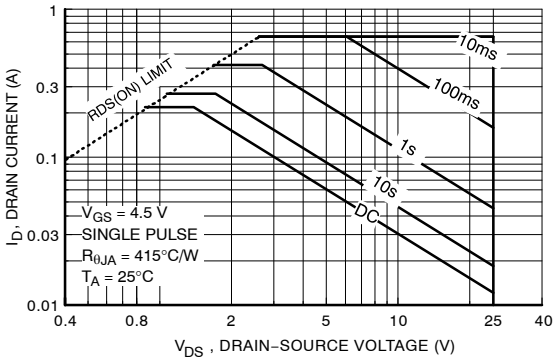



**Figure 9. Maximum Safe Operating Area**

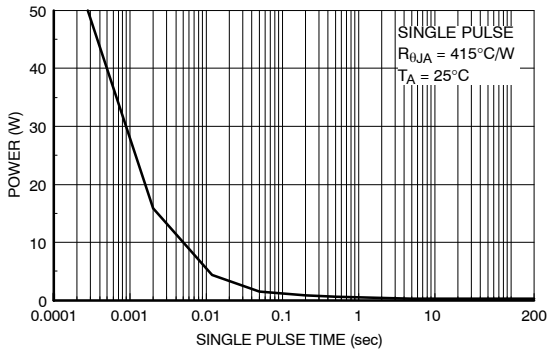



**Figure 10. Single Pulse Maximum Power Dissipation**

## TYPICAL PERFORMANCE CHARACTERISTICS: P−CHANNEL

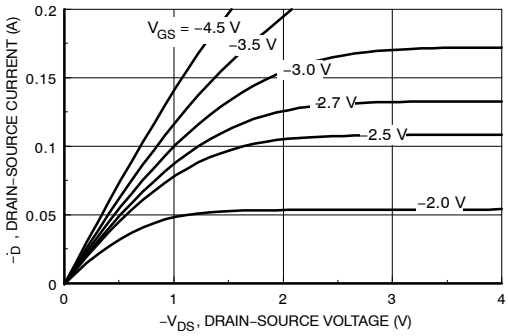



**Figure 11. On−Region Characteristics**

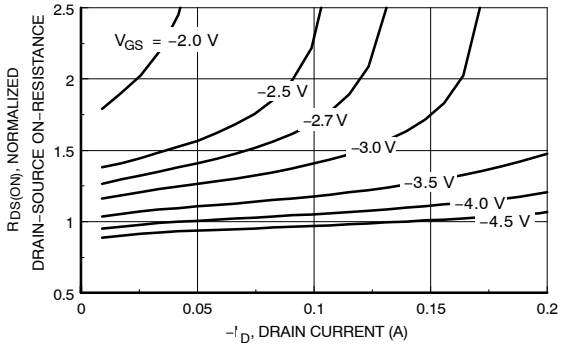



**Figure 12. On−Resistance Variation with Drain Current and Gate Voltage**

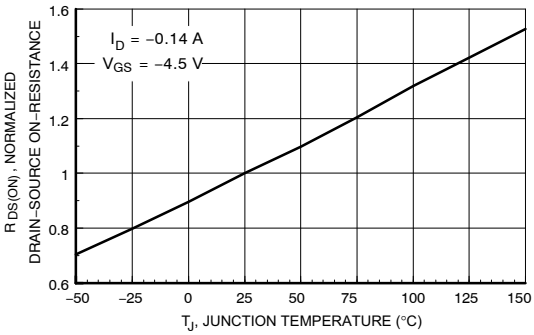



**Figure 13. On−Resistance Variation with Temperature**

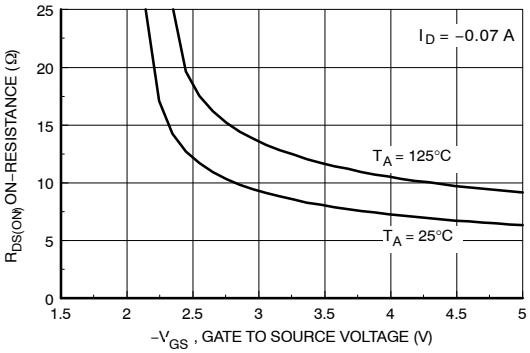



**Figure 14. On−Resistance Variation with Gate−to−Source Voltage**

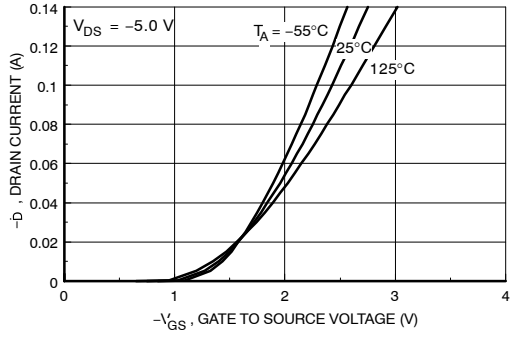



**Figure 15. Transfer Characteristics**

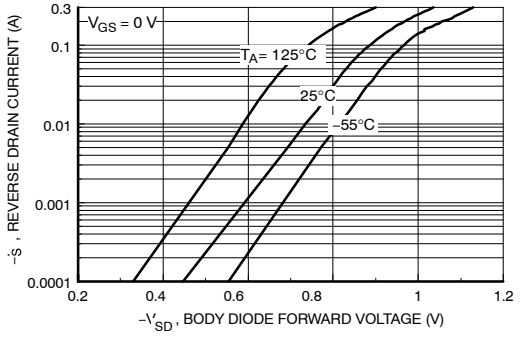



**Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature**

## TYPICAL PERFORMANCE CHARACTERISTICS: P−CHANNEL (continued)

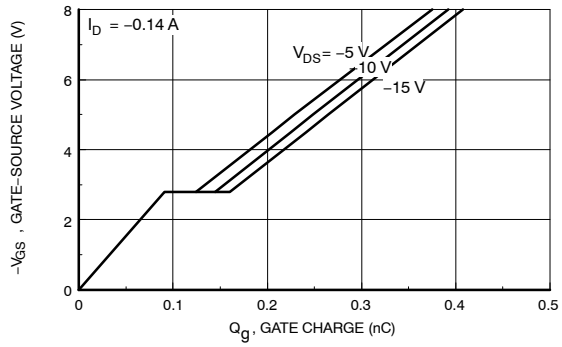



**Figure 17. Gate Charge Characteristics**

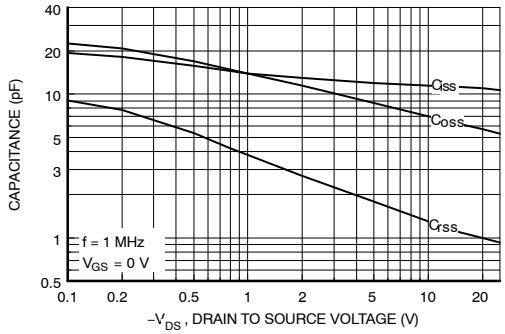



**Figure 18. Capacitance Characteristics**

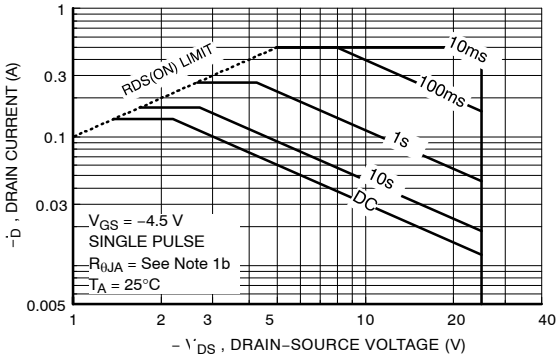



**Figure 19. Maximum Safe Operating Area**

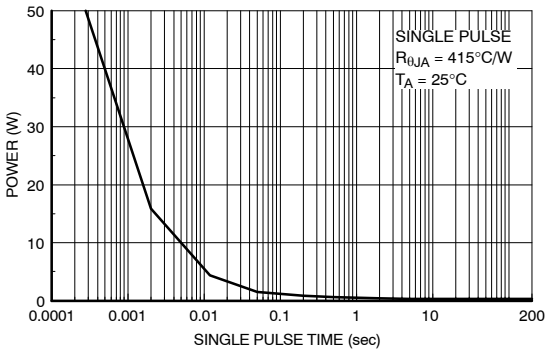
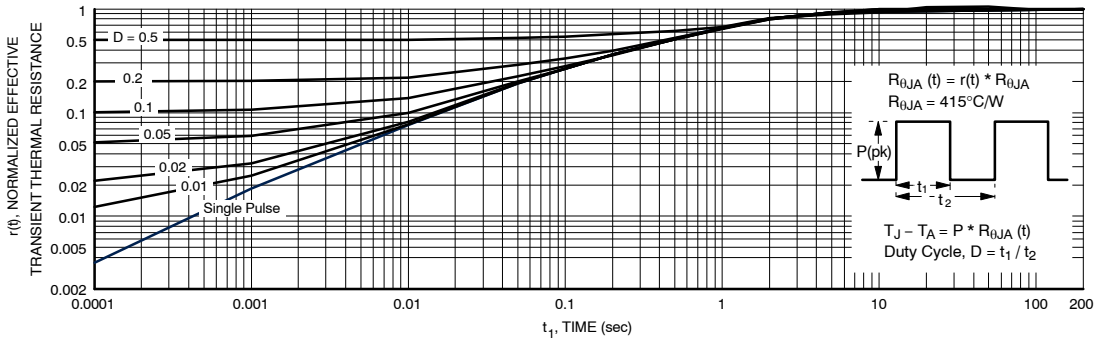



**Figure 20. Single Pulse Maximum Power Dissipation**

## TYPICAL PERFORMANCE CHARACTERISTICS: N & P−CHANNEL




Thermal characterization performed using the conditions described in Note 1.
Transient thermal response will change depending on the circuit board design.

**Figure 21. Transient Thermal Response Curve**

## ORDERING INFORMATION

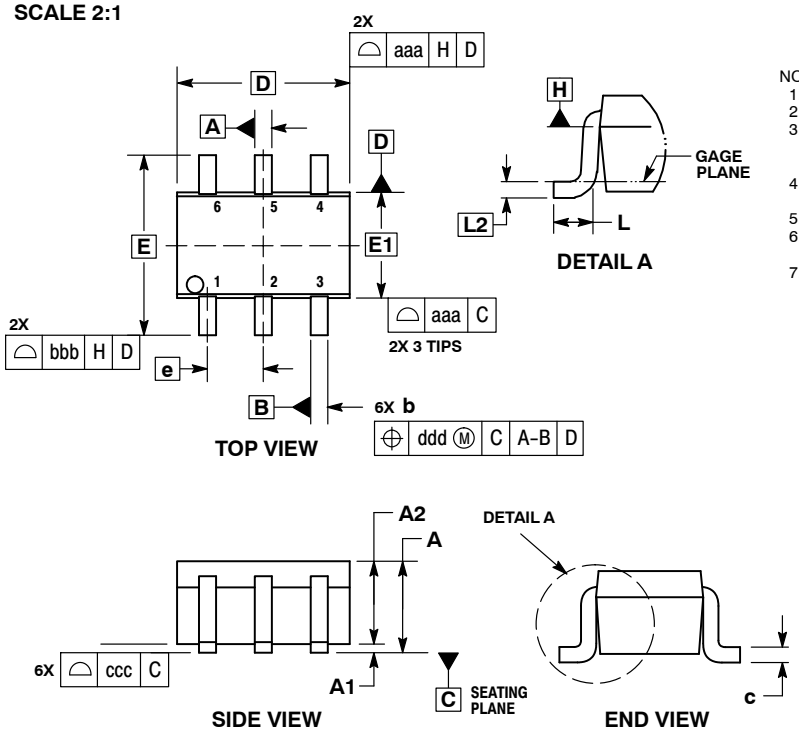
| Device Order Number | Device Marking | Package Type | Shipping† |
|---|---|---|---|
| FDG6320C | 20 | SC−88/SC70−6/SOT−363 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**SC−88/SC70−6/SOT−363**
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

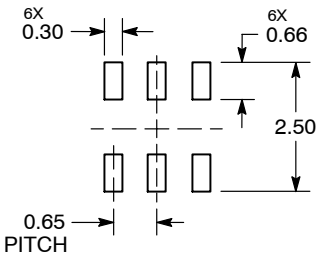
1
**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| **DIM** | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** |
| **A** | −−− | −−− | 1.10 | −−− | −−− | 0.043 |
| **A1** | 0.00 | −−− | 0.10 | 0.000 | −−− | 0.004 |
| **A2** | 0.70 | 0.90 | 1.00 | 0.027 | 0.035 | 0.039 |
| **b** | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| **C** | 0.08 | 0.15 | 0.22 | 0.003 | 0.006 | 0.009 |
| **D** | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| **E** | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |
| **E1** | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| **e** | 0.65 BSC | | | 0.026 BSC | | |
| **L** | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| **L2** | 0.15 BSC | | | 0.006 BSC | | |
| **aaa** | 0.15 | | | 0.006 | | |
| **bbb** | 0.30 | | | 0.012 | | |
| **ccc** | 0.10 | | | 0.004 | | |
| **ddd** | 0.10 | | | 0.004 | | |

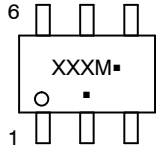
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "▪", may or may not be present. Some products may not follow the Generic Marking.


**STYLES ON PAGE 2**

**SC−88/SC70−6/SOT−363**
CASE 419B−02
ISSUE Y

DATE 11 DEC 2012

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
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