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April 2015

# FDD5353

## N-Channel Power Trench<sup>®</sup> MOSFET

60V, 50A, 12.3mΩ

### Features

- Max  $r_{DS(on)}$  = 12.3mΩ at  $V_{GS} = 10V$ ,  $I_D = 10.7A$
- Max  $r_{DS(on)}$  = 15.4mΩ at  $V_{GS} = 4.5V$ ,  $I_D = 9.5A$
- 100% UIL Tested
- RoHS Compliant

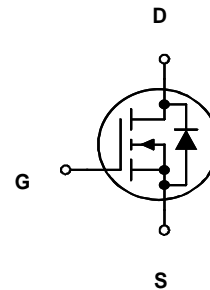
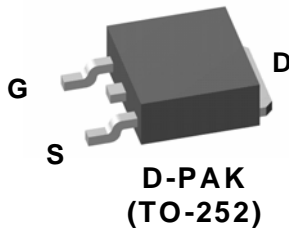


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- Inverter
- Synchronous rectifier
- Primary switch



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Rating	Units
$V_{DS}$	Drain to Source Voltage		60	V
$V_{GS}$	Gate to Source Voltage		$\pm 20$	V
$I_D$	Drain Current -Continuous	$T_C = 25^\circ\text{C}$	50	A
	-Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	11.5	
	-Pulsed		100	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	253	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	69	W
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	3.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Rating	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD5353	FDD5353	D-PAK (TO-252)	13"	16mm	2500 units

FDD5353 N-Channel Power Trench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		77		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{V}, V_{DS} = 48\text{V}$ ,			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-8		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 10.7\text{A}$		10.1	12.3	m $\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 9.5\text{A}$		12.1	15.4	
		$V_{GS} = 10\text{V}, I_D = 10.7\text{A}, T_J = 125^\circ\text{C}$		16.7	20.3	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{V}, I_D = 10.7\text{A}$		41		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		2420	3215	pF
$C_{oss}$	Output Capacitance			215	285	pF
$C_{riss}$	Reverse Transfer Capacitance			120	180	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$		1.7	

### Switching Characteristics

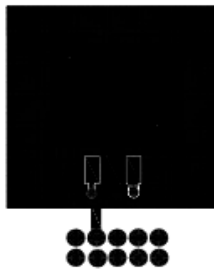
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}, I_D = 10.7\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$		11	20	ns
$t_r$	Rise Time			6	11	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
$t_f$	Fall Time			4	10	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V to } 10\text{V}$		46	65
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{V to } 4.5\text{V}$	$V_{DD} = 30\text{V},$ $I_D = 10.7\text{A}$	23	32	nC
$Q_{gs}$	Gate to Source Charge			7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			9		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 10.7\text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{V}, I_S = 2.6\text{A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 10.7\text{A}, di/dt = 100\text{A}/\mu\text{s}$		28	45	ns
$Q_{rr}$	Reverse Recovery Charge			21	34	nC

Notes:

- 1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  
 $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $40^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper

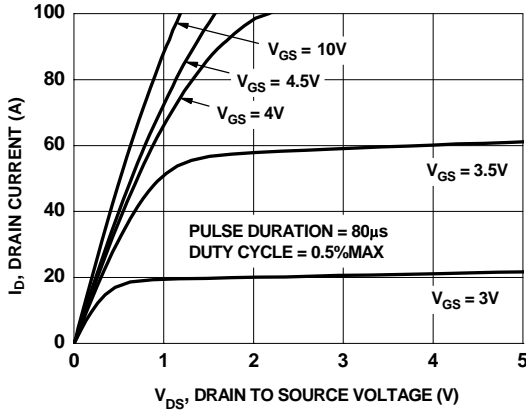


b)  $96^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

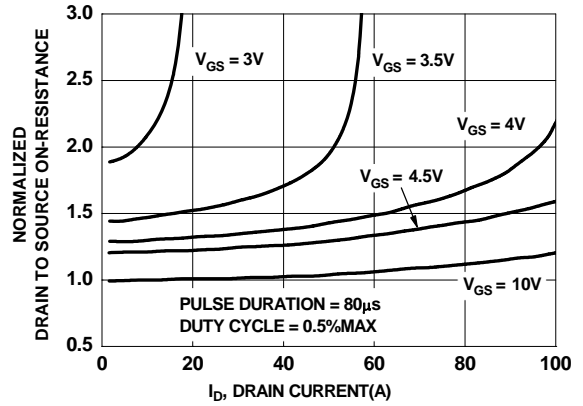
2: Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

3:  $E_{AS}$  of 253mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = 13\text{A}$ ,  $V_{DD} = 60\text{V}$ ,  $V_{GS} = 10\text{V}$ . 100% test at  $L = 0.1\text{mH}$ ,  $I_{AS} = 41\text{A}$ .

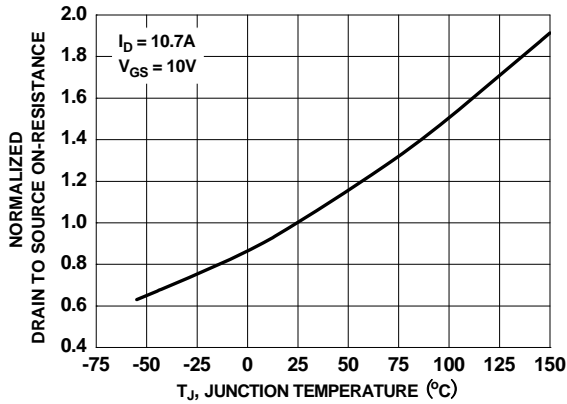
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



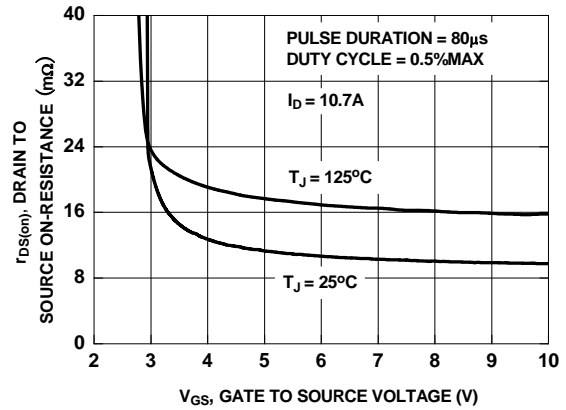
**Figure 1. On-Region Characteristics**



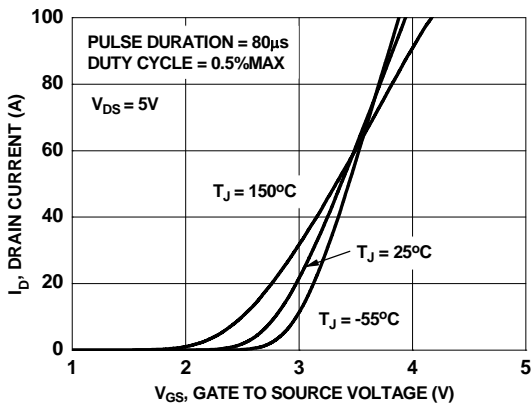
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



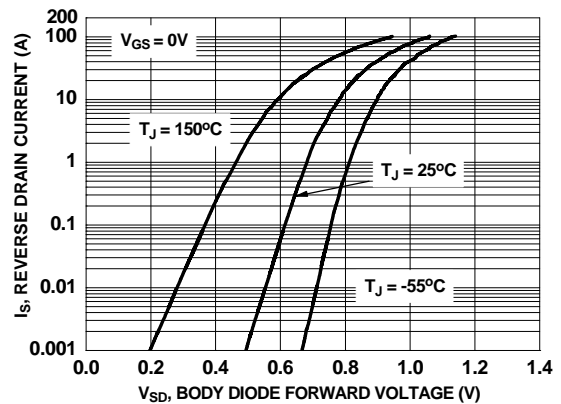
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

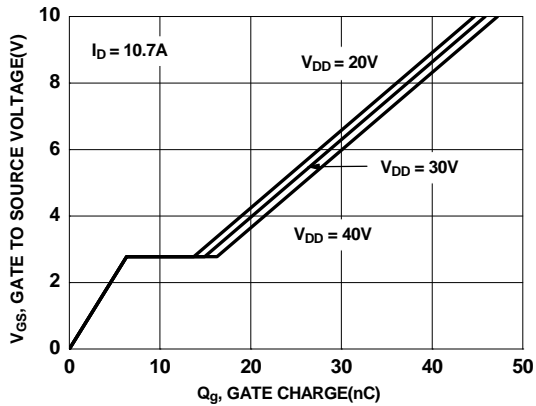


**Figure 5. Transfer Characteristics**

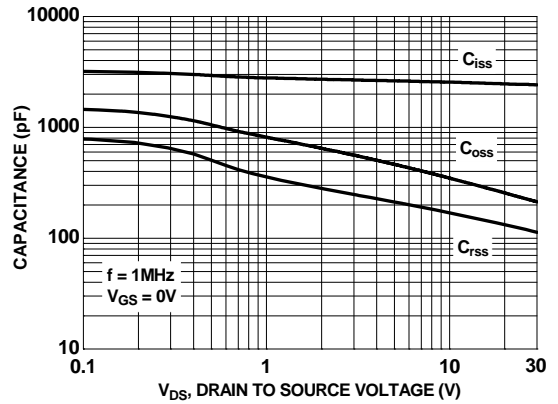


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

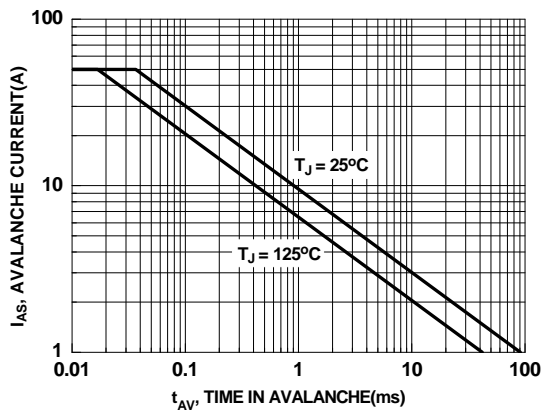
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



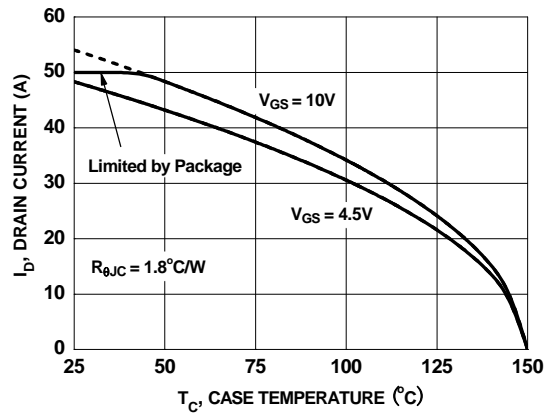
**Figure 7. Gate Charge Characteristics**



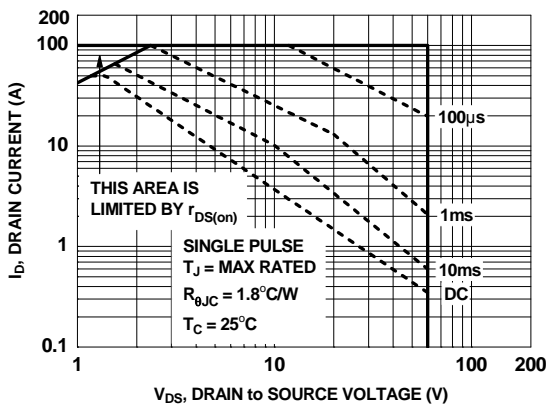
**Figure 8. Capacitance vs Drain to Source Voltage**



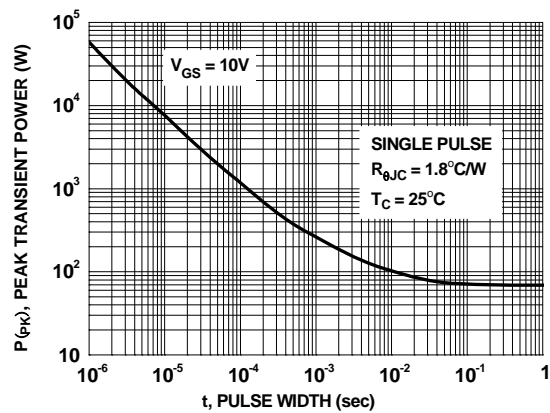
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

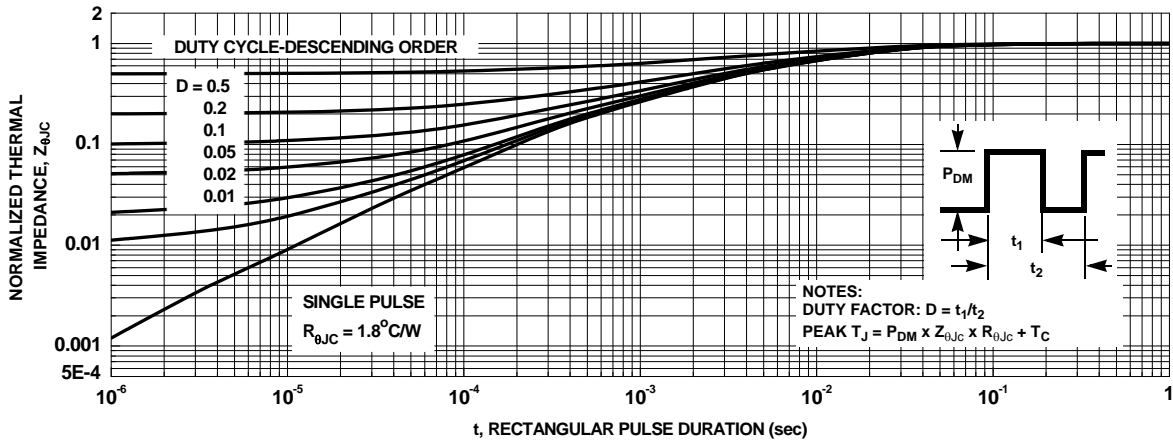


**Figure 11. Forward Bias Safe Operating Area**

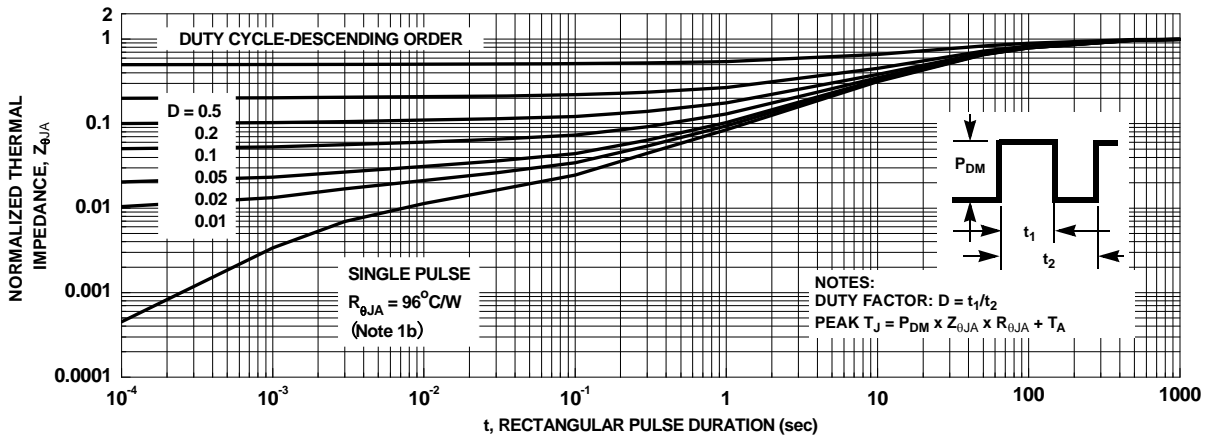


**Figure 12. Single Pulse Maximum Power Dissipation**

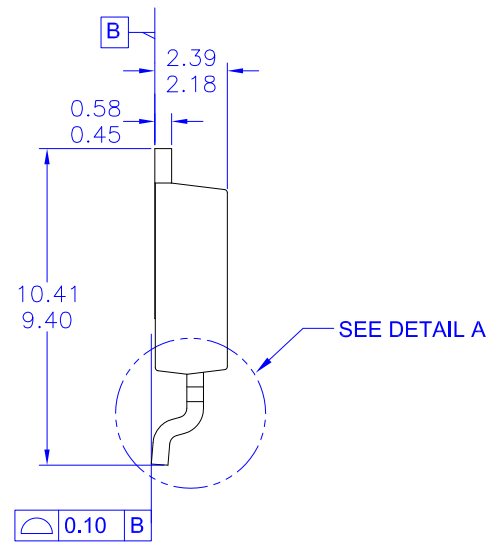
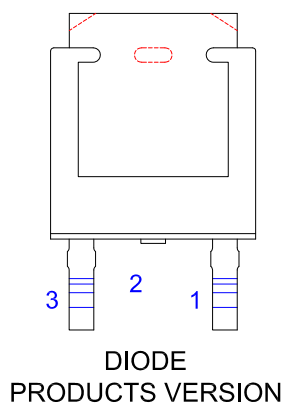
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**

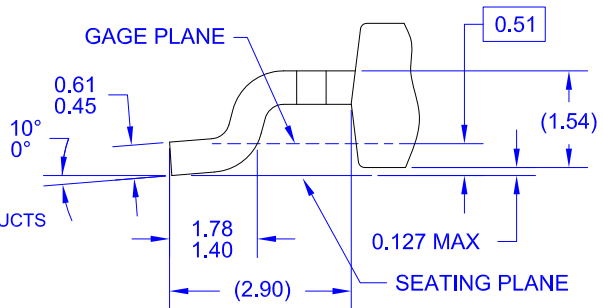


**Figure 14. Transient Thermal Response Curve**



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A  
(ROTATED -90°)  
SCALE: 12X



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