

# Integrated Load Switch

## FDC6324L

### Description

These Integrated Load Switches are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage high side load switch application where low conduction loss and ease of driving are needed.

### Features

- $V_{\text{DROP}} = 0.2 \text{ V} @ V_{\text{IN}} = 12 \text{ V}, I_{\text{L}} = 1 \text{ A}, V_{\text{ON/OFF}} = 1.5 \text{ to } 8 \text{ V}$
- $V_{\text{DROP}} = 0.3 \text{ V} @ V_{\text{IN}} = 5 \text{ V}, I_{\text{L}} = 1 \text{ A}, V_{\text{ON/OFF}} = 1.5 \text{ to } 8 \text{ V}$
- High Density Cell Design for Extremely Low On-Resistance
- $V_{\text{ON/OFF}}$  Zener Protection for ESD Ruggedness > 6 kV Human Body Model
- SUPERSOT<sup>™</sup>-6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- This is a Pb-Free and Halide Free Device

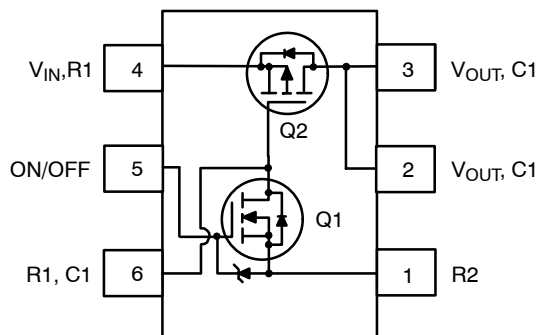


Figure 1.

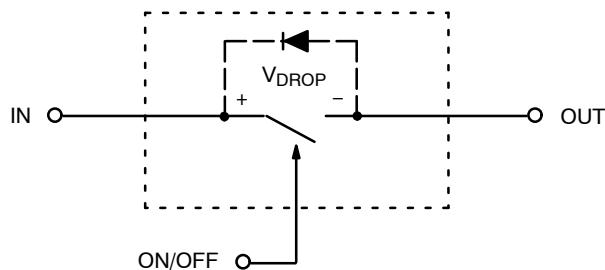
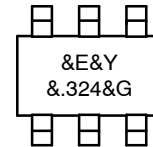


Figure 2. Equivalent Circuit



TSOT-23-6  
CASE 419BL

### MARKING DIAGRAM



&E	= Designates Space
&Y	= Binary Calendar Year Coding Scheme
&.	= Pin One Dot
324	= Specific Device Code
&G	= Date Code

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
FDC6324L	TSOT-23-6 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# FDC6324L

## ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Unit
$V_{IN}$	Input Voltage Range	3–20	V
$V_{ON/OFF}$	On/Off Voltage Range	1.5–8	V
$I_L$	Load Current @ $V_{DROP} = 0.5\text{ V}$ – Continuous (Note 1)	1.5	A
	Load Current @ $V_{DROP} = 0.5\text{ V}$ – Pulsed (Note 1, Note 3)	2.5	
$P_D$	Maximum Power Dissipation (Note 2a)	0.7	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	–55 to 150	$^\circ\text{C}$
ESD	Electrostatic Discharge Rating MIL–STD–883D Human Body Model (100 pF/1500 $\Omega$ )	6	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 2a)	180	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case (Note 2)	60	$^\circ\text{C/W}$

## ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$I_{FL}$	Forward Leakage Current	$V_{IN} = 20\text{ V}, V_{ON/OFF} = 0\text{ V}$	–	–	1	$\mu\text{A}$
$I_{RL}$	Reverse Leakage Current	$V_{IN} = -20\text{ V}, V_{ON/OFF} = 0\text{ V}$	–	–	–1	$\mu\text{A}$

### ON CHARACTERISTICS (Note 3)

$V_{IN}$	Input Voltage		3	–	20	V
$V_{ON/OFF}$	On/Off Voltage		1.5	–	8	V
$V_{DROP}$	Conduction Voltage Drop @ 1 A	$V_{IN} = 10\text{ V}, V_{ON/OFF} = 3.3\text{ V}$	–	0.135	0.2	V
		$V_{IN} = 5\text{ V}, V_{ON/OFF} = 3.3\text{ V}$	–	0.215	0.3	
$I_L$	Load Current	$V_{DROP} = 0.2\text{ V}, V_{IN} = 10\text{ V}, V_{ON/OFF} = 3.3\text{ V}$	1	–	–	A
		$V_{DROP} = 0.3\text{ V}, V_{IN} = 5\text{ V}, V_{ON/OFF} = 3.3\text{ V}$	1	–	–	

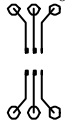
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- $V_{IN} = 20\text{ V}, V_{ON/OFF} = 8\text{ V}, V_{DROP} = 0.5\text{ V}, T_A = 25^\circ\text{C}$
- $R_{\theta JA}$  is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)}@T_J$$

Typical  $R_{\theta CA}$  for single device operation using the board layouts shown below on FR–4 PCB in a still air environment:



a) 180 $^\circ\text{C/W}$  when mounted on a 2oz minimum copper pad.

- Pulse Test: Pulse Width  $\leq 300\text{ }\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

TYPICAL ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

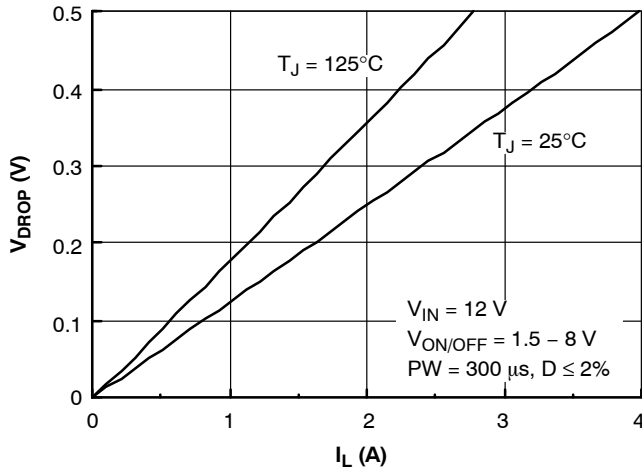


Figure 3.  $V_{\text{DROP}}$  Versus  $I_L$  at  $V_{\text{IN}} = 12\text{ V}$

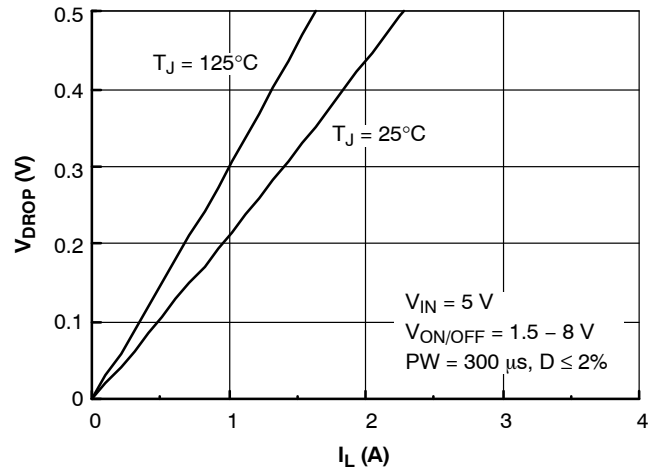


Figure 4.  $V_{\text{DROP}}$  Versus  $I_L$  at  $V_{\text{IN}} = 5.0\text{ V}$

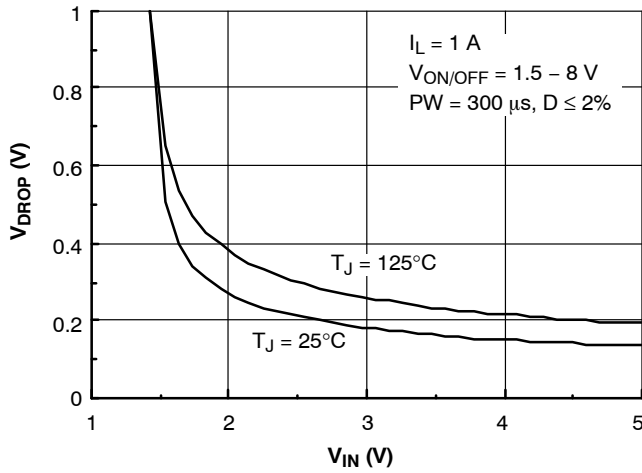


Figure 5.  $V_{\text{DROP}}$  Versus  $V_{\text{IN}}$  at  $I_L = 1\text{ A}$

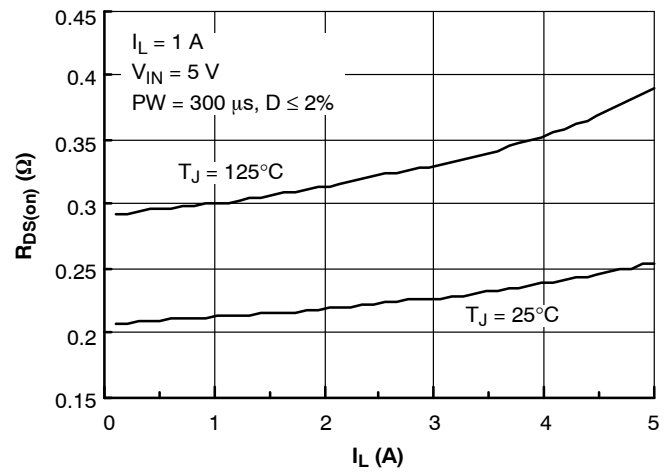


Figure 6.  $R_{\text{DS(on)}}$  Versus  $I_L$  at  $V_{\text{IN}} = 5.0\text{ V}$

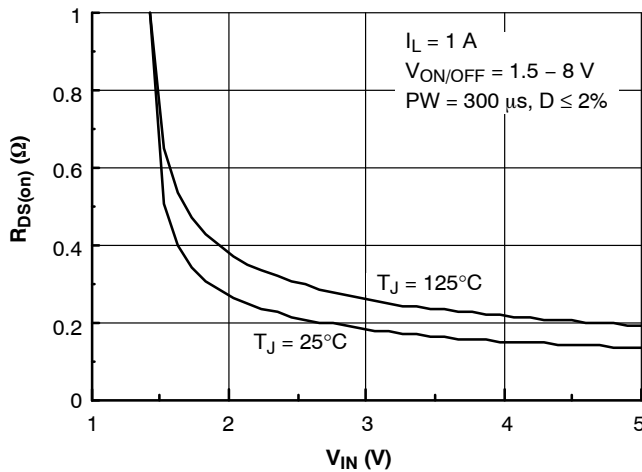


Figure 7. On Resistance Variation with Input Voltage

TYPICAL ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

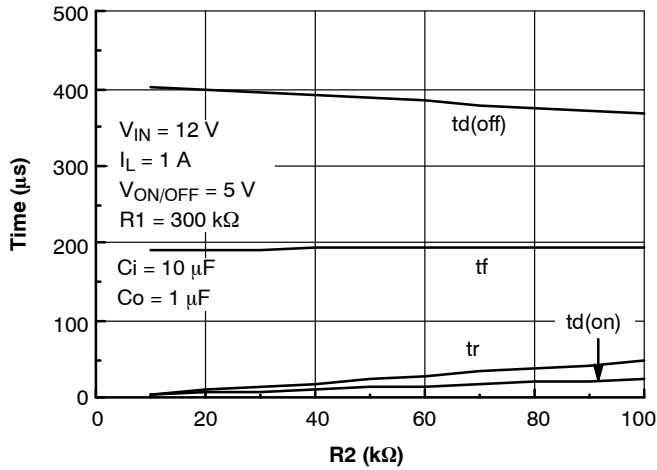


Figure 8. Switching Variation with  $R_2$  at  $V_{IN} = 12\text{ V}$  and  $R_1 = 300\text{ k}\Omega$

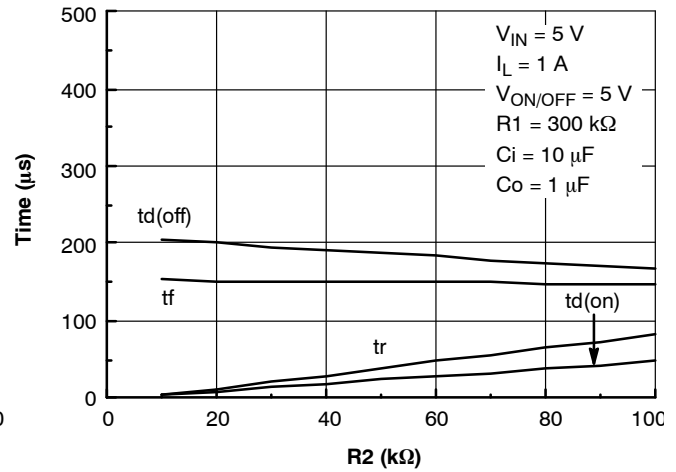


Figure 9. Switching Variation with  $R_2$  at  $V_{IN} = 5\text{ V}$  and  $R_1 = 300\text{ k}\Omega$

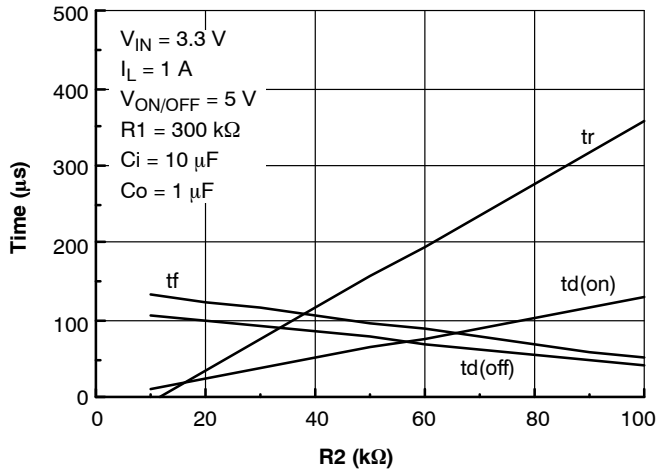


Figure 10. Switching Variation with  $R_2$  at  $V_{IN} = 3.3\text{ V}$  and  $R_1 = 300\text{ k}\Omega$

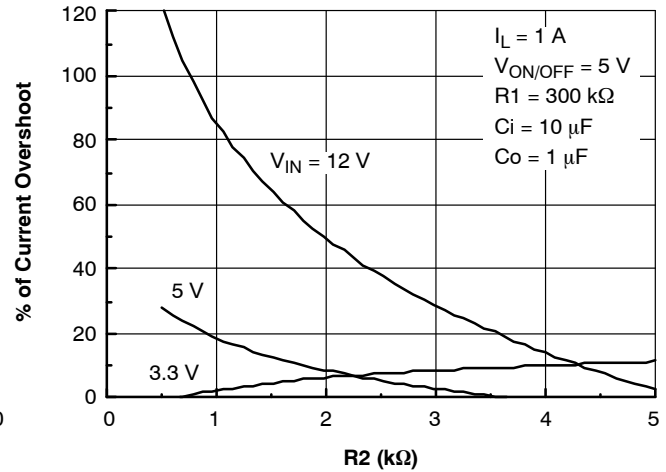


Figure 11. % of Current Overshoot Variation with  $V_{IN}$  and  $R_2$

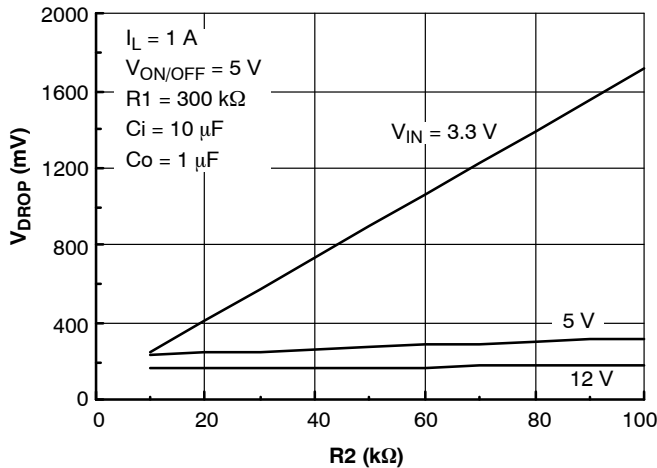


Figure 12.  $V_{DROP}$  Variation with  $V_{IN}$  and  $R_2$

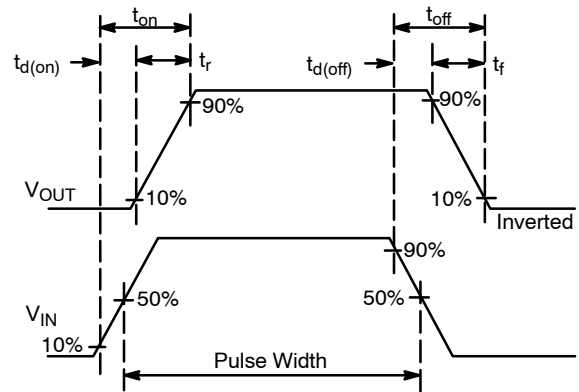


Figure 13. Switching Waveforms

# FDC6324L

## TYPICAL ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

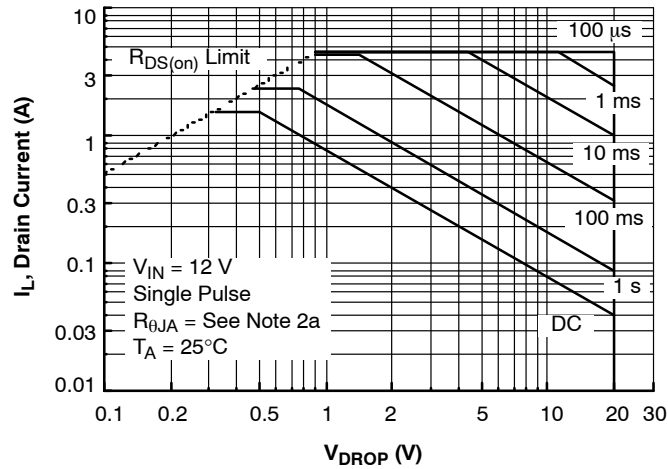


Figure 14. Safe Operating Area

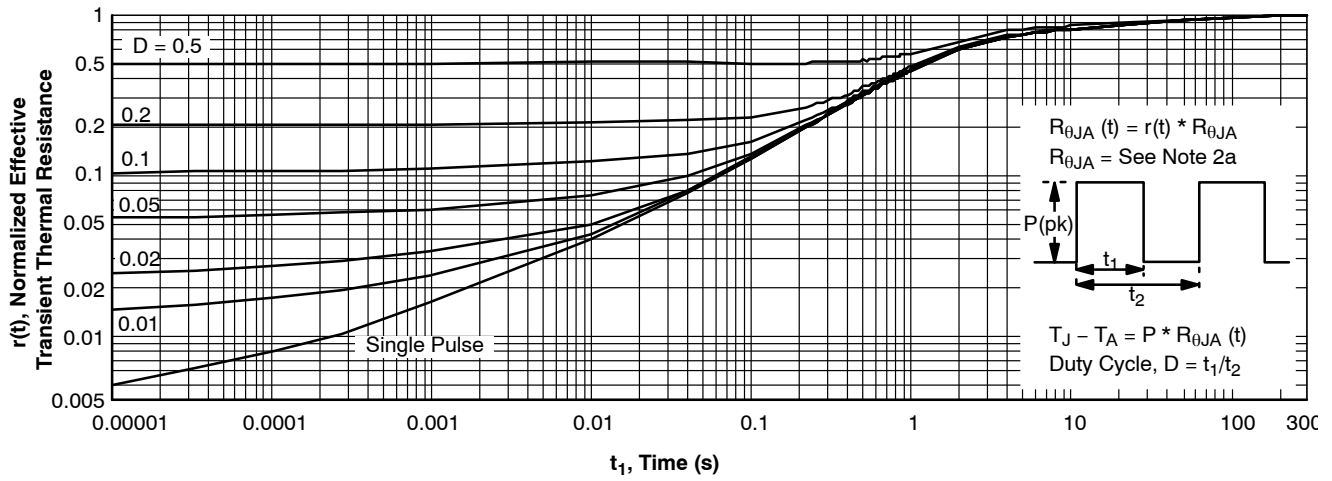


Figure 15. Transient Thermal Response Curve

NOTE: Thermal characterization performed on the conditions described in Note 2a. Transient thermal response will change depends on the circuit board.

## LOAD SWITCH APPLICATION

## General Description

This device is particularly suited for computer peripheral switching applications where 20 V input and 1 A output current capability are needed. This load switch integrates a small N-Channel Power MOSFET (Q1) which drives a large P-Channel Power MOSFET (Q2) in one tiny SUPERSOT-6 package.

A load switch is usually configured for high side switching so that the load can be isolated from the active power source. A P-Channel Power MOSFET, because it does not require its drive voltage above the input voltage, is usually more cost effective than using an N-Channel device in this particular application. A large P-Channel Power MOSFET minimizes voltage drop. By using a small N-Channel device the driving stage is simplified.

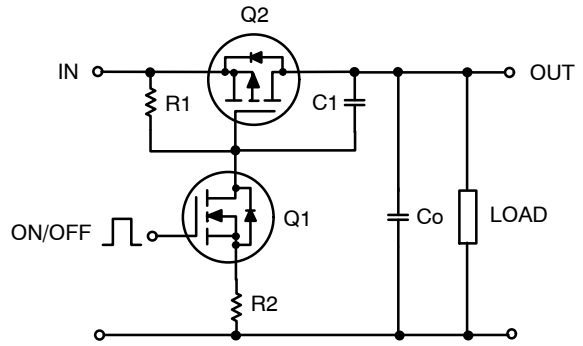


Figure 16. Application Circuit

## Component Values

- R1: Typical 10k–1 MΩ
- R2: Typical 0–100 kΩ (optional)
- C1: Typical 1000 pF (optional)

## Design Notes

- R1 is needed to turn off Q2.
- R2 can be used to soft start the switch in case the output capacitance Co is small.
- R2 should be at least 10 times smaller than R1 to guarantee Q1 turns on.
- By using R1 and R2 a certain amount of current is lost from the input. This bias current loss is given by the equation:  

$$I_{BIAS\_LOSS} = \frac{V_{IN}}{R1 + R2}$$
 when the switch is ON.  $I_{BIAS\_LOSS}$  can be minimized by selecting a large value for R1.
- R2 and  $C_{RSS}$  of Q2 make ramp for slow turn on. If excessive overshoot current occurs due to fast turn on, additional capacitance C1 can be added externally to slow down the turn on.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

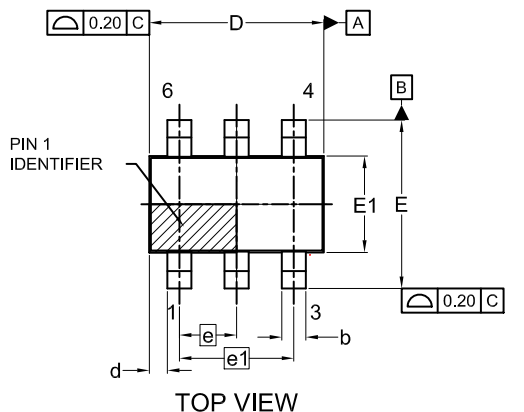
ON Semiconductor®



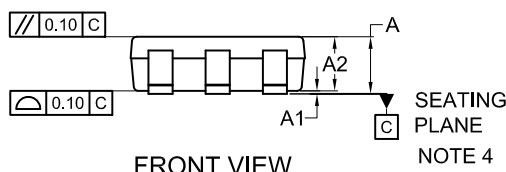
SCALE 2:1

### TSOT23 6-Lead CASE 419BL ISSUE A

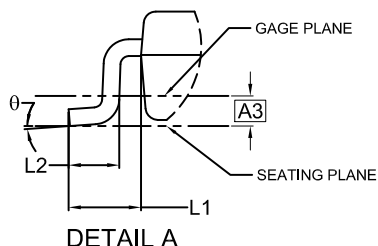
DATE 31 AUG 2020



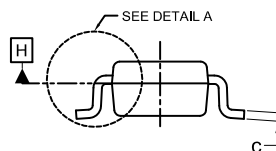
TOP VIEW



FRONT VIEW

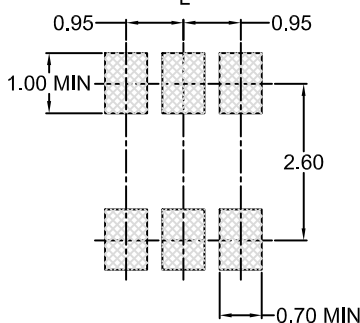


DETAIL A



SIDE VIEW

SYMM  
⌀



### LAND PATTERN RECOMMENDATION

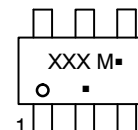
\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	---	10°

### GENERIC MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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