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FCPF11N60F

N-Channel SuperFET® FRFET® MOSFET

600 V, 11 A, 380 mΩ

Features

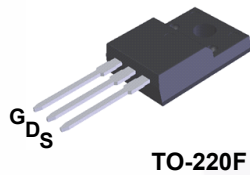
- 600 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 320\text{ m}\Omega$
- Fast Recovery Type ($t_{rr} = 120\text{ ns}$)
- Ultra Low Gate Charge (Typ. $Q_g = 40\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 95\text{ pF}$)
- 100% Avalanche Tested
- RoHS compliant

Applications

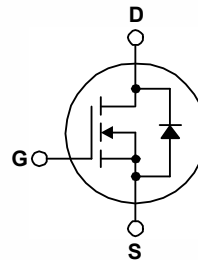
- LCD/LED/PDP TV
- Lighting
- Solar Inverter
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



TO-220F



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCPF11N60F	Unit
V_{DSS}	Drain to Source Voltage	600	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	11*
		- Continuous ($T_C = 100^\circ\text{C}$)	7*
I_{DM}	Drain Current	33*	A
		(Note 1)	
V_{GSS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy	340	mJ
		(Note 2)	
I_{AR}	Avalanche Current	11	A
		(Note 1)	
E_{AR}	Repetitive Avalanche Energy	12.5	mJ
		(Note 1)	
dv/dt	Peak Diode Recovery dv/dt	4.5	V/ns
		(Note 3)	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	36
		- Derate Above 25°C	0.29
			W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCPF11N60F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCPF11N60F	FCPF11N60F	TO-220F	-	-	50

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.6	-	$V/^\circ\text{C}$
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 11\text{ A}$	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}$	-	0.32	0.38	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 5.5\text{ A}$	-	6	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	1148	1490	pF
C_{oss}	Output Capacitance		-	671	870	pF
C_{rss}	Reverse Transfer Capacitance		-	63	82	pF
C_{oss}	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	35	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	95	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 480\text{ V}, I_D = 11\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	40	52	nC
Q_{gs}	Gate to Source Gate Charge		-	7.2	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	21	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 11\text{ A}, R_G = 25\ \Omega$ (Note 4)	-	34	80	ns
t_r	Turn-On Rise Time		-	98	205	ns
$t_{d(off)}$	Turn-Off Delay Time		-	119	250	ns
t_f	Turn-Off Fall Time		-	56	120	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	11	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	33	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$	-	120	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{ A}/\mu\text{s}$	-	0.8	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{AS} = 5.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 11\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

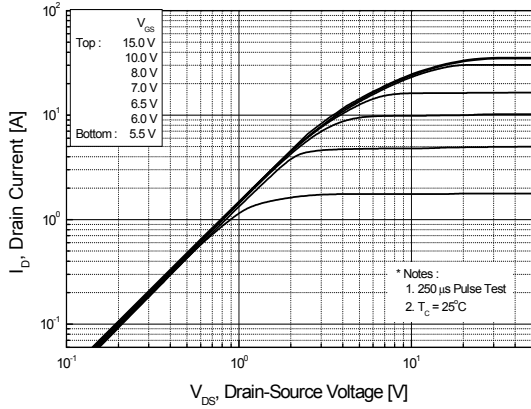


Figure 2. Transfer Characteristics

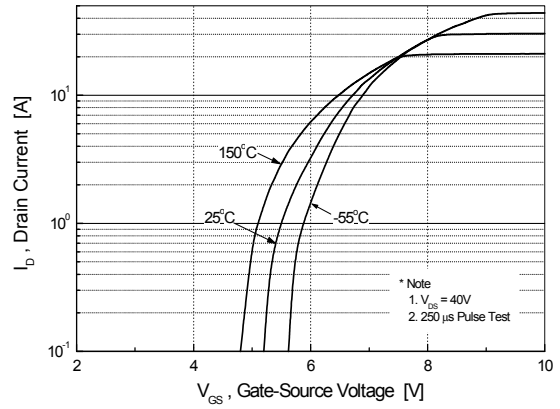


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

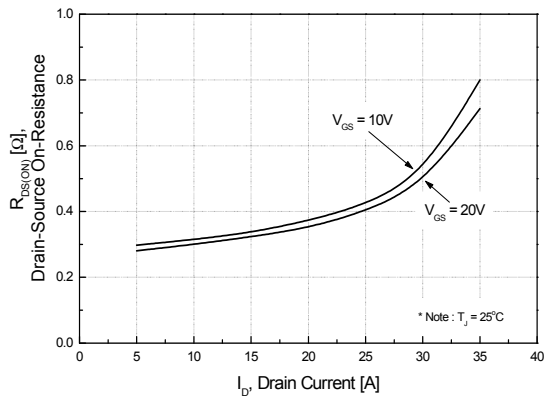


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

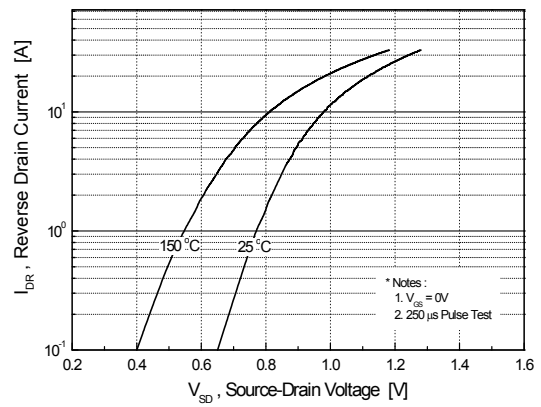


Figure 5. Capacitance Characteristics

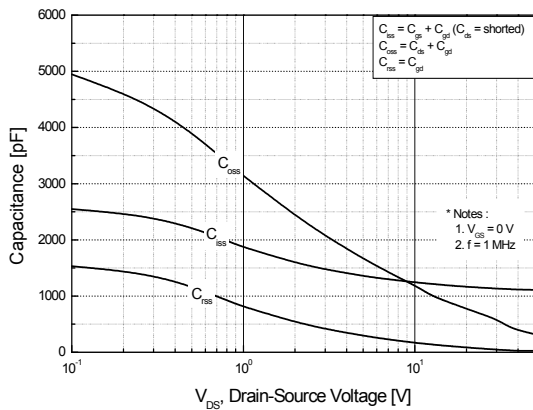
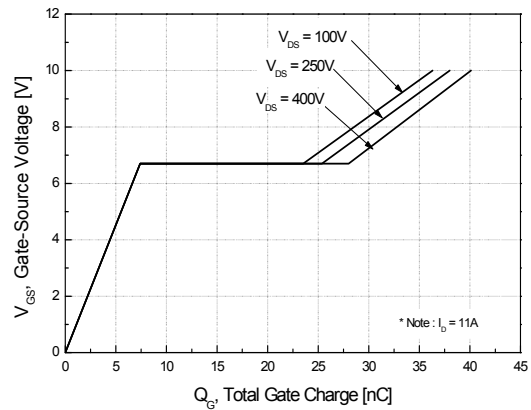


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

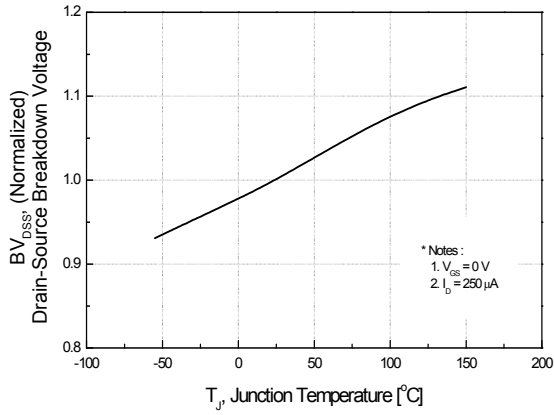


Figure 8. On-Resistance Variation vs. Temperature

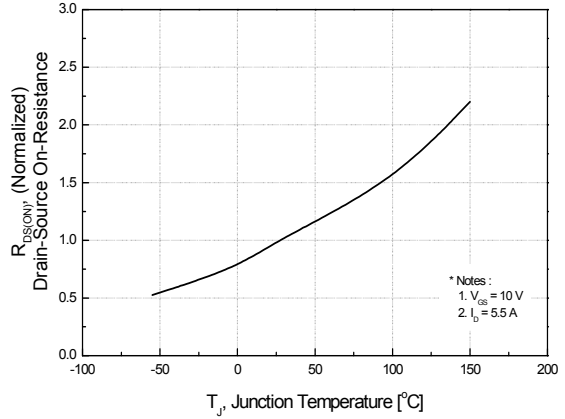


Figure 9. Safe Operating Area

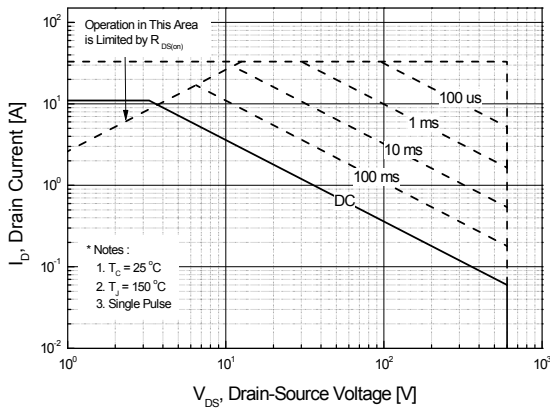


Figure 10. Maximum Drain Current vs. Case Temperature

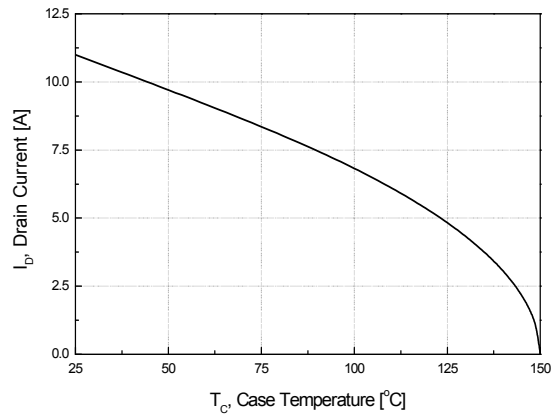
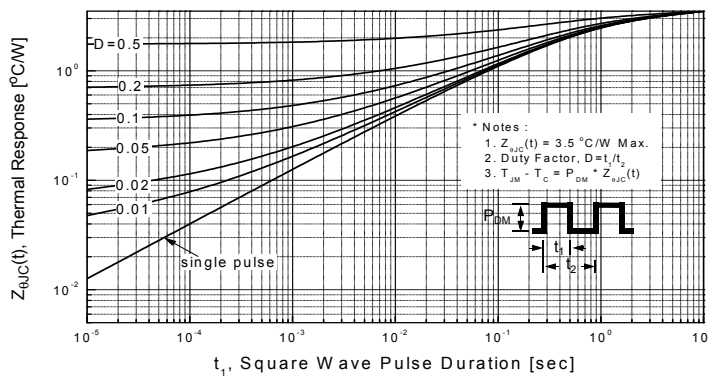


Figure 11. Transient Thermal Response Curve



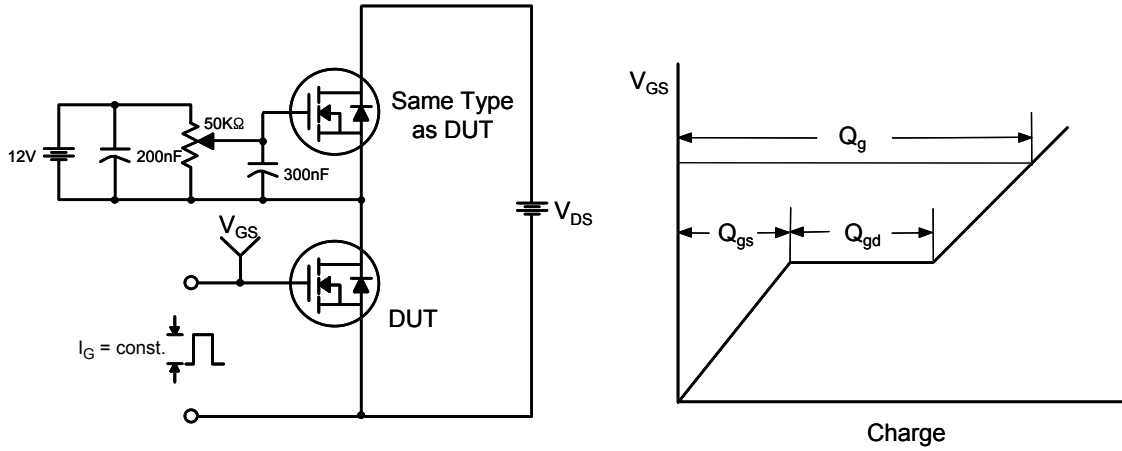


Figure 12. Gate Charge Test Circuit & Waveform

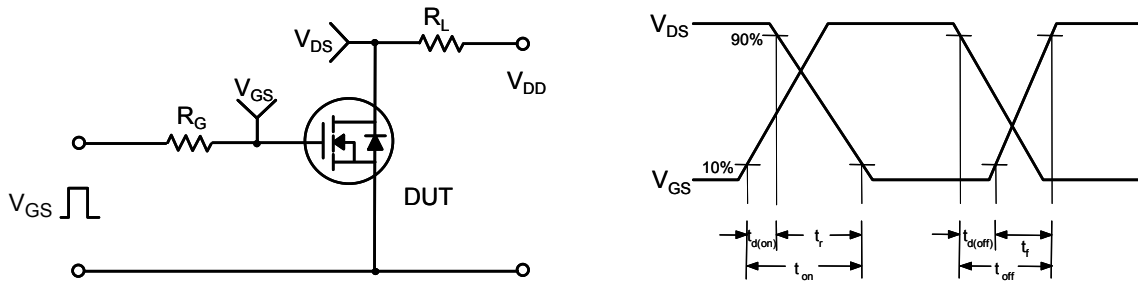


Figure 13. Resistive Switching Test Circuit & Waveforms

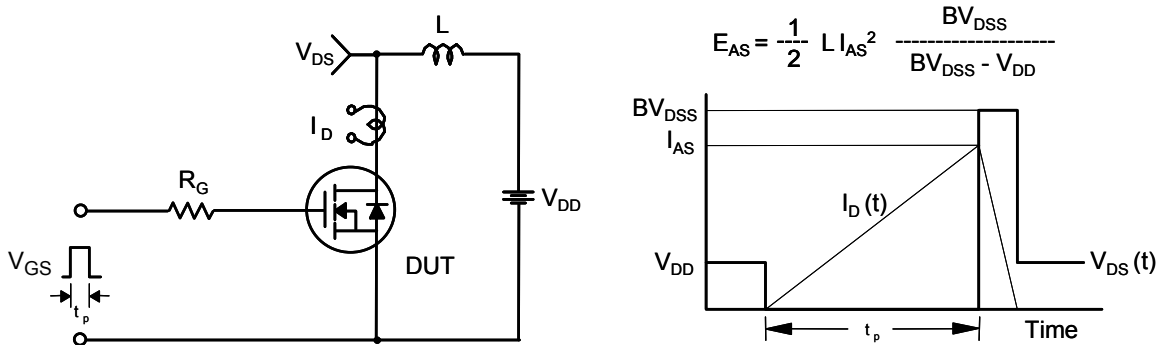


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

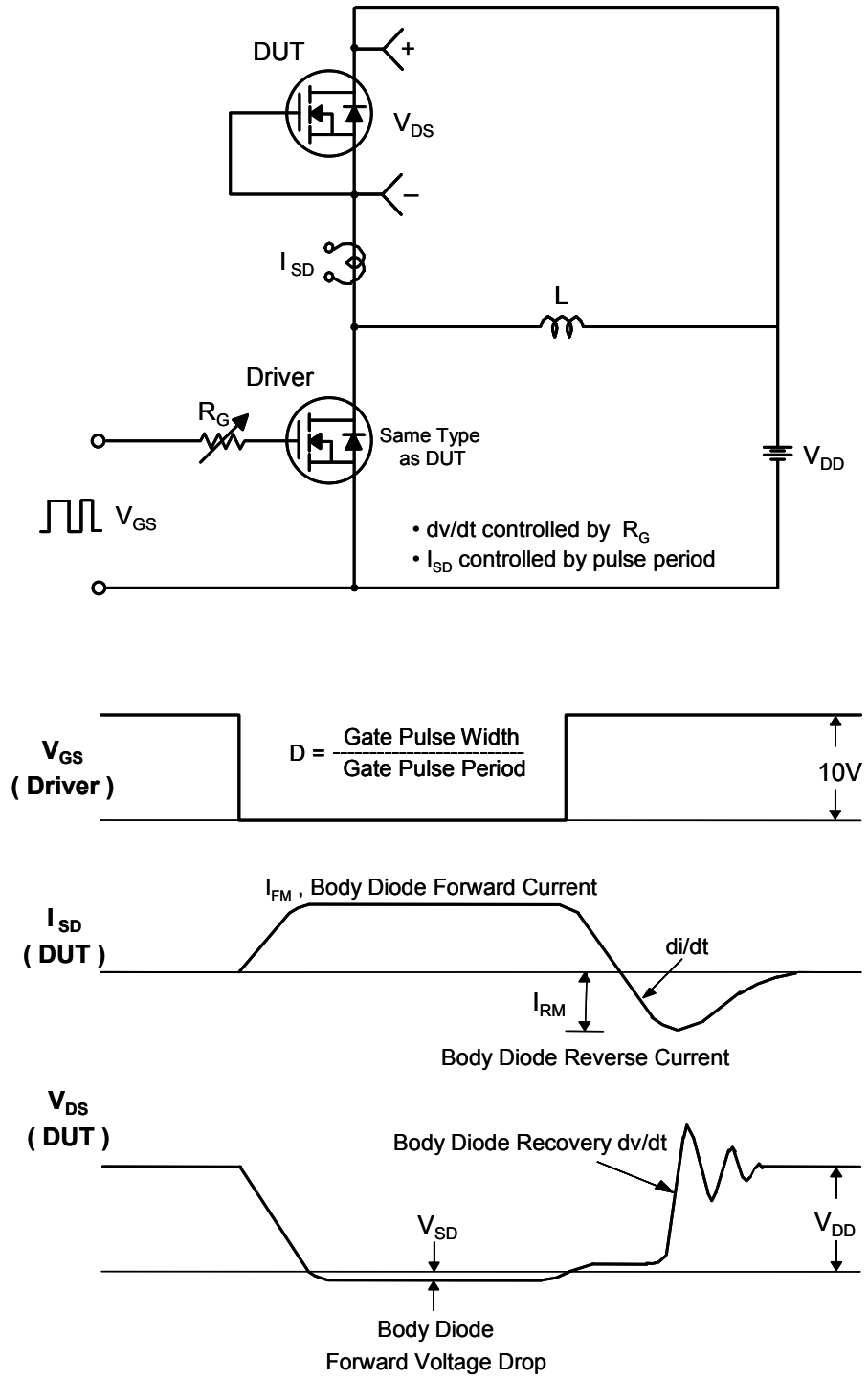
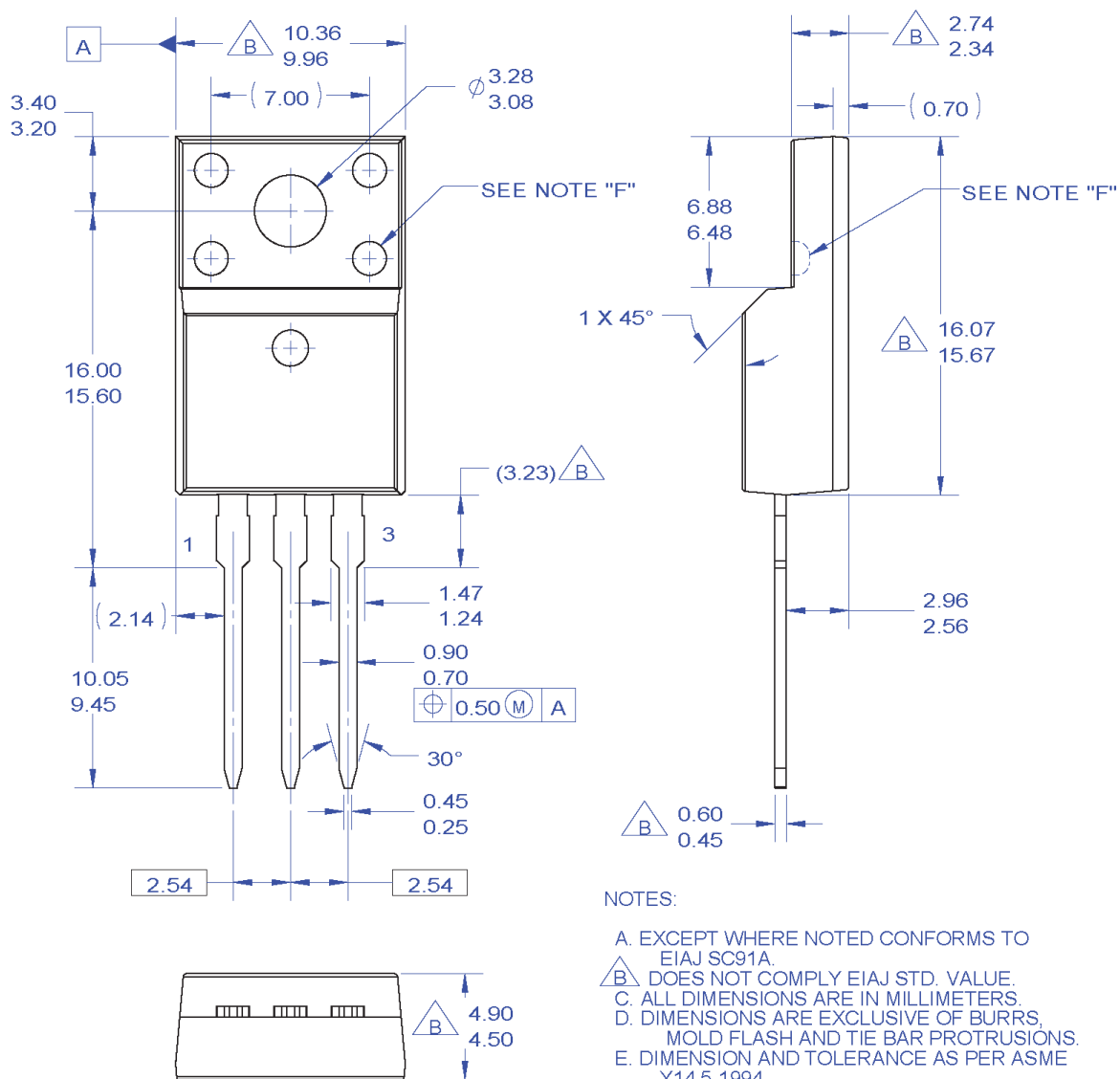


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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