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December 2014

# FCP110N65F

## N-Channel SuperFET® II FRFET® MOSFET 650 V, 35 A, 110 mΩ

### Features

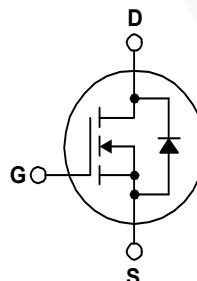
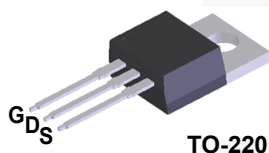
- 700 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 96\text{ m}\Omega$  (Typ.)
- Ultra Low Gate Charge (Typ.  $Q_g = 98\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 464\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- LCD / LED / PDP TV
- Telecom / Server Power Supplies
- Solar Inverter
- AC - DC Power Supply

### Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCP110N65F	Unit
$V_{DSS}$	Drain to Source Voltage	650	V
$V_{GSS}$	Gate to Source Voltage	- DC	V
		- AC (f > 1 Hz)	
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$I_{AR}$	Avalanche Current	(Note 1)	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt	(Note 3)	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	W
		- Derate Above $25^\circ\text{C}$	$W/^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCP110N65F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP110N65F	FCP110N65F	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	650	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	700	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.72	-	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	-	110	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 3.5\text{ mA}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 17.5\text{ A}$	-	96	110	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 17.5\text{ A}$	-	30	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	3680	4895	pF
$C_{oss}$	Output Capacitance		-	110	145	pF
$C_{rss}$	Reverse Transfer Capacitance		-	0.65	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	65	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	464	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 17.5\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	98	145	nC
$Q_{gs}$	Gate to Source Gate Charge		-	20	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	43	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.7	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 17.5\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\text{ }\Omega$ (Note 4)	-	31	72	ns
$t_r$	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	89	188	ns
$t_f$	Turn-Off Fall Time	(Note 4)	-	5.7	21	ns

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	35	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	105	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 17.5 A	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 17.5 A, dI <sub>F</sub> /dt = 100 A/μs	-	133	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	0.67	-	μC

#### Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2.  $I_{AS} = 8\text{ A}$ ,  $R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 17.5\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 380\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

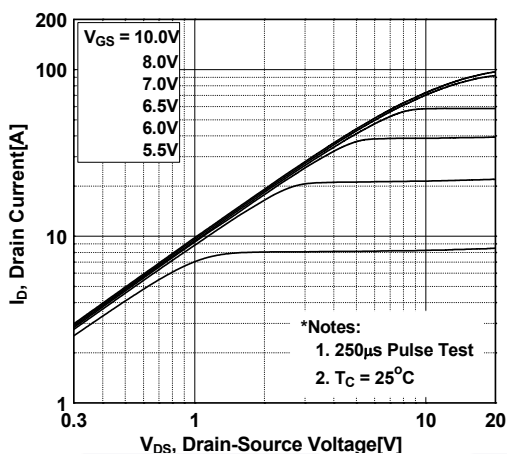


Figure 2. Transfer Characteristics

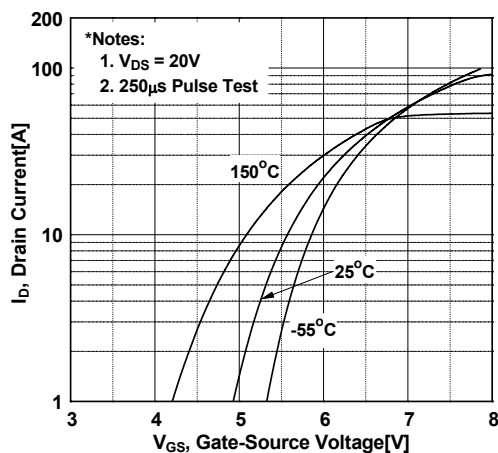


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

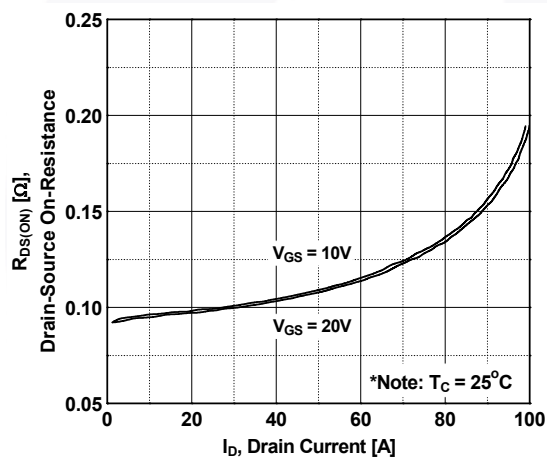


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

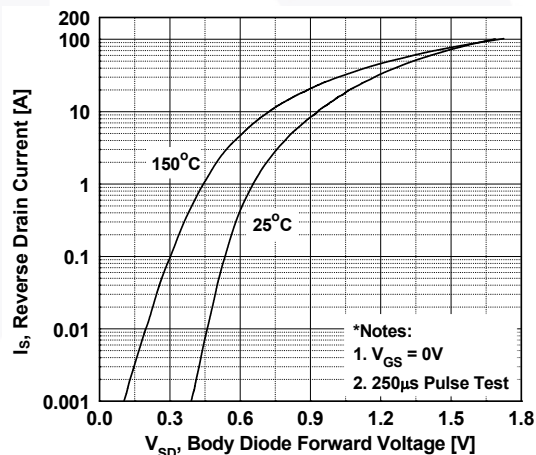


Figure 5. Capacitance Characteristics

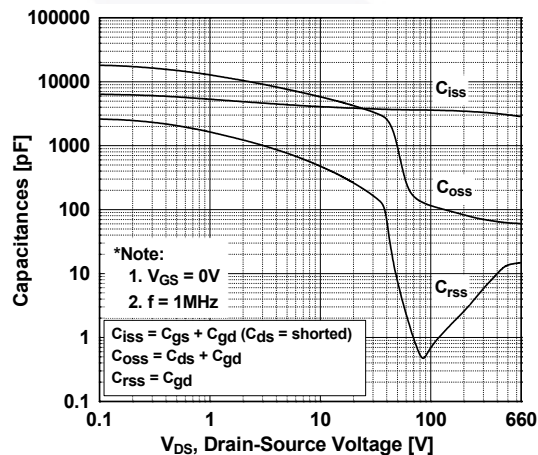
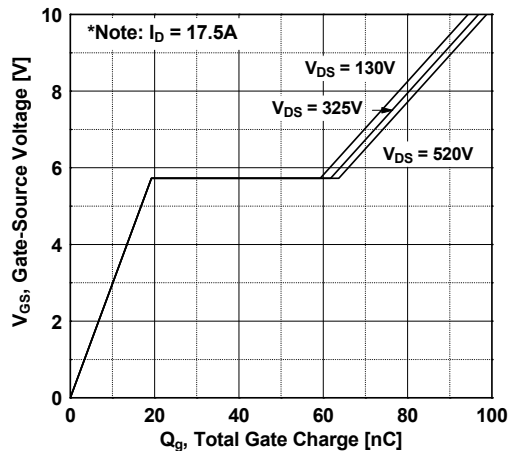


Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

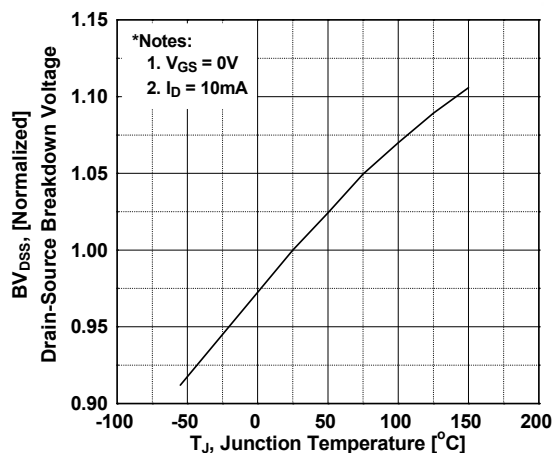


Figure 8. On-Resistance Variation vs. Temperature

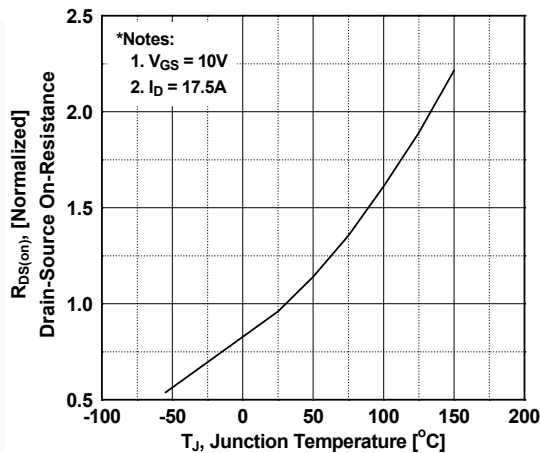


Figure 9. Maximum Safe Operating Area

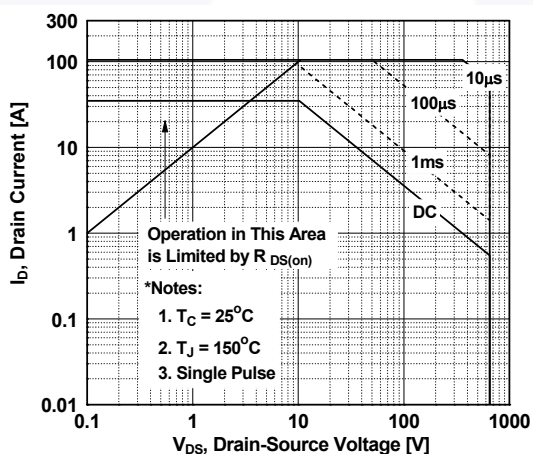


Figure 10. Maximum Drain Current vs. Case Temperature

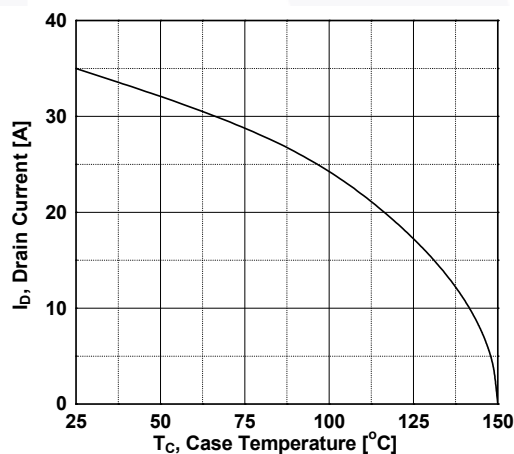
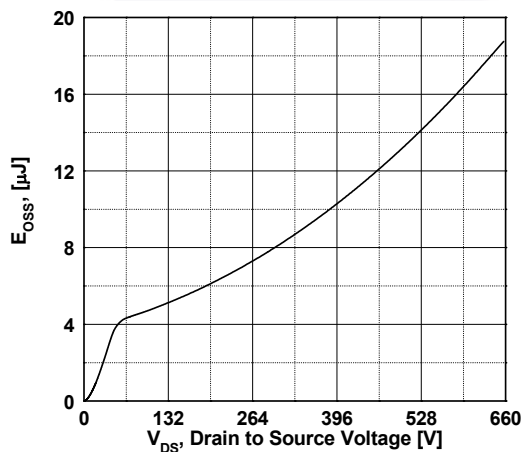
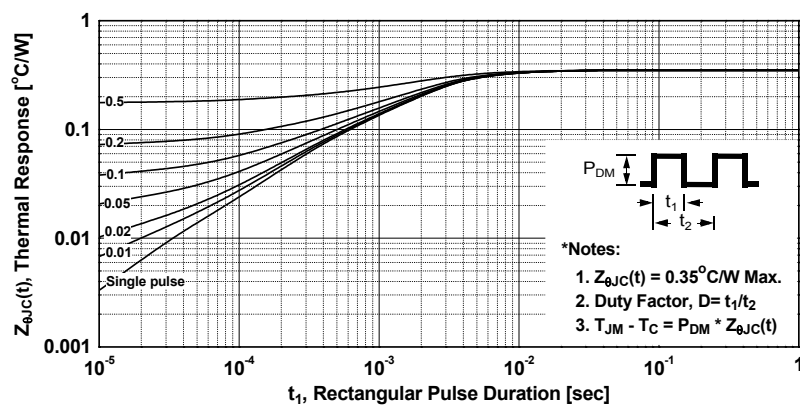


Figure 11. Eoss vs. Drain to Source Voltage



# Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



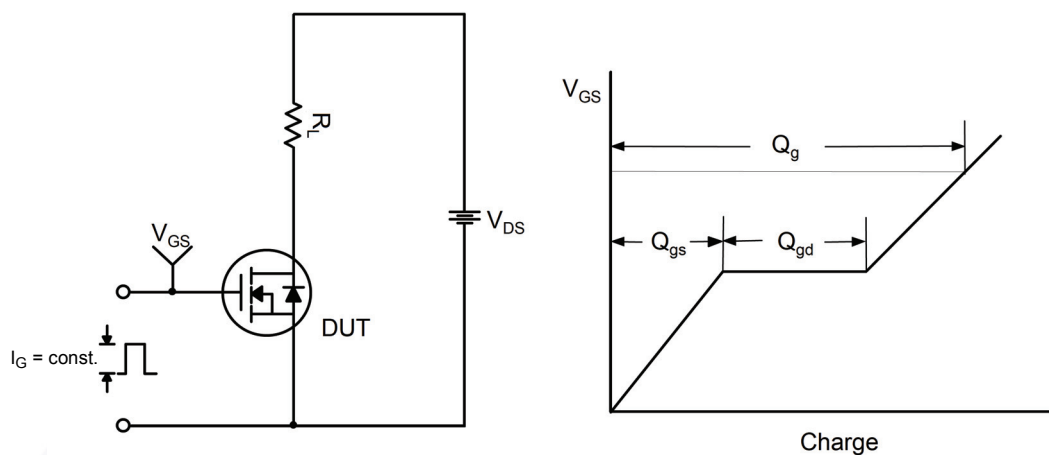


Figure 13. Gate Charge Test Circuit & Waveform

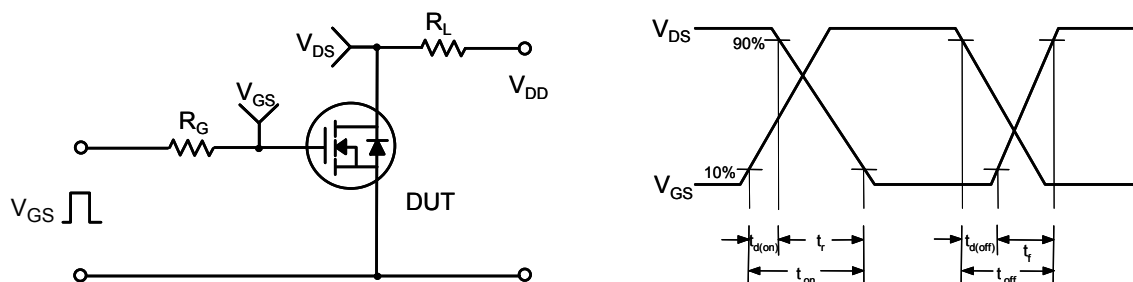


Figure 14. Resistive Switching Test Circuit & Waveforms



Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

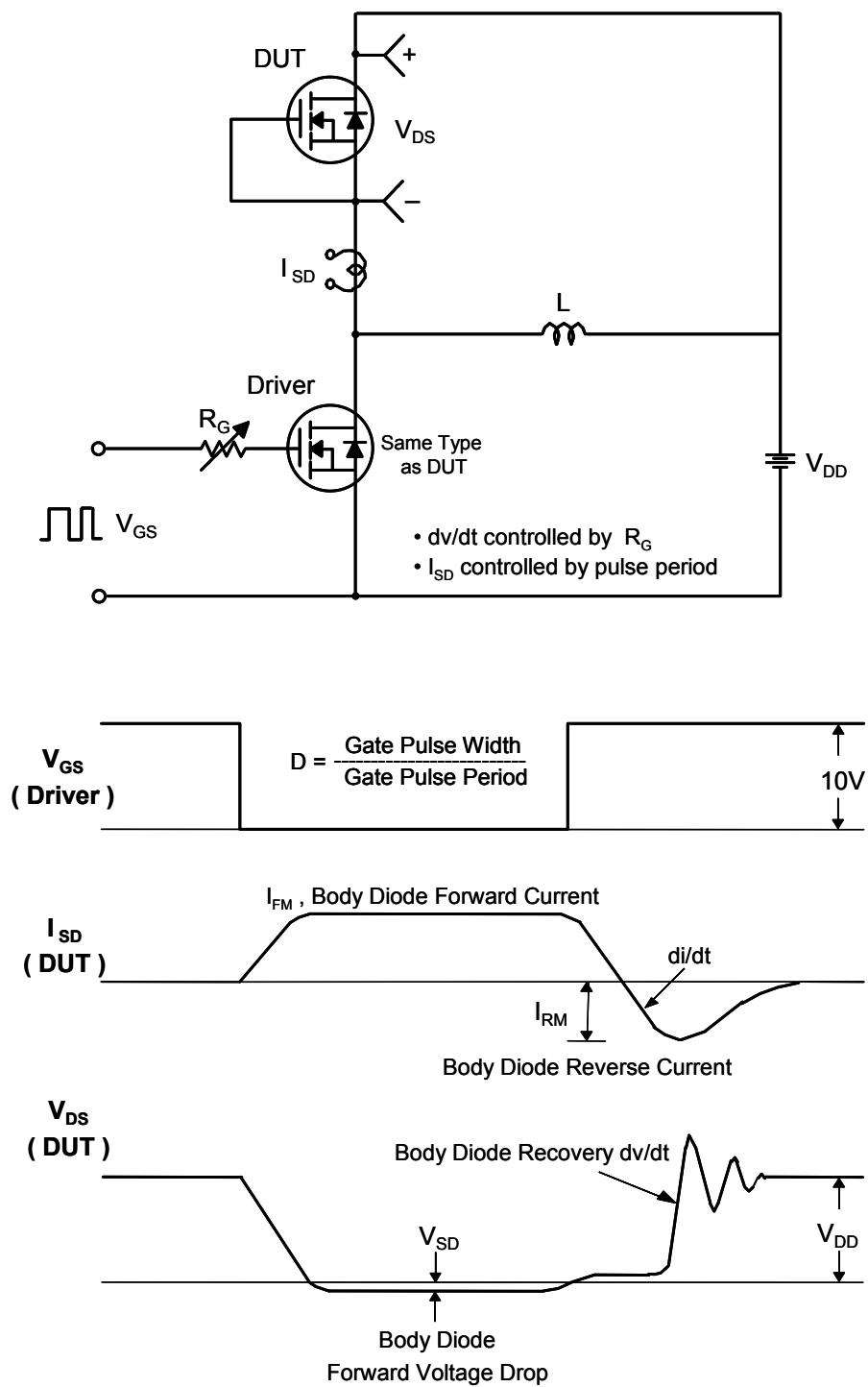


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms





# NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- E) DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:  
SINGLE GAUGE = 0.51 - 0.61  
DUAL GAUGE = 1.10 - 1.45
- G) DRAWING FILE NAME: TO220B03REV9
- H) PRESENCE IS SUPPLIER DEPENDENT
- I) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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