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# FAN8841

## Dual Half-Bridge Piezoelectric Driver with Step-up DC-DC Converter

### Features

#### Step-up DC-DC Converter

- Integrated Step-up Power Switch up to 36 V
- Wide Operating Voltage Range of 2.7 to 5.5 V
- Adjustable Step-up Output Voltage by  $V_{CON}$
- Adjustable Step-up Switch Current Limit
- Zero Current Detector (ZCD)
- Internal Soft-Start
- Built-in Protection Circuit
  - Under-Voltage Protection (UVP)
  - Over-Voltage Protection (OVP)

#### Piezo Actuator Driver

- Integrated Half-Bridge Switches ( $V_{DS}=75$  V)
- Dual Half-Bridge Piezoelectric Driver
- Built-in Shutdown Function

#### Package Information

- Small 4.0 mm × 4.0 mm MLP

### Applications

- Piezoelectric Actuator

### Description

The FAN8841 is a single-chip piezoelectric actuator driver consisting of a step-up DC-DC converter with integrated 36 V boost switch and the dual half-bridge output stages. The step-up DC-DC converter operates in Critical Conduction Mode (CRM) in order to reduce switching loss at the DC-DC converter for high efficiency. It is optimized to work in a coupled-inductor configuration to provide output voltages in excess of 60 V. The step-up DC-DC converter has a soft-start capability that limits the inrush current during startup. Over-voltage protection and over-current protection are included. Under-voltage protection is used to disable the dual half-bridge gate driver when the step-up DC-DC converter output voltage is lower than the specified threshold voltage. The boost voltage is set using external resistors and analog voltage at the  $V_{CON}$  pin and step-up current limit is programmable via the external resistor at the OCP pin. The output Half-bridge is integrated with 75 V P- and N-channel for the piezoelectric actuator driving. An open drain Fault-out (FO) signal indicates if an abnormal over-voltage has occurred.

### Ordering Information

| Part Number | Operating Temperature Range | Package                                                | Packing Method |
|-------------|-----------------------------|--------------------------------------------------------|----------------|
| FAN8841MPX  | -40°C to +125°C             | 24-Lead, 4.0 mm × 4.0 mm Molded Leadless Package (MLP) | Tape & Reel    |

## Typical Application

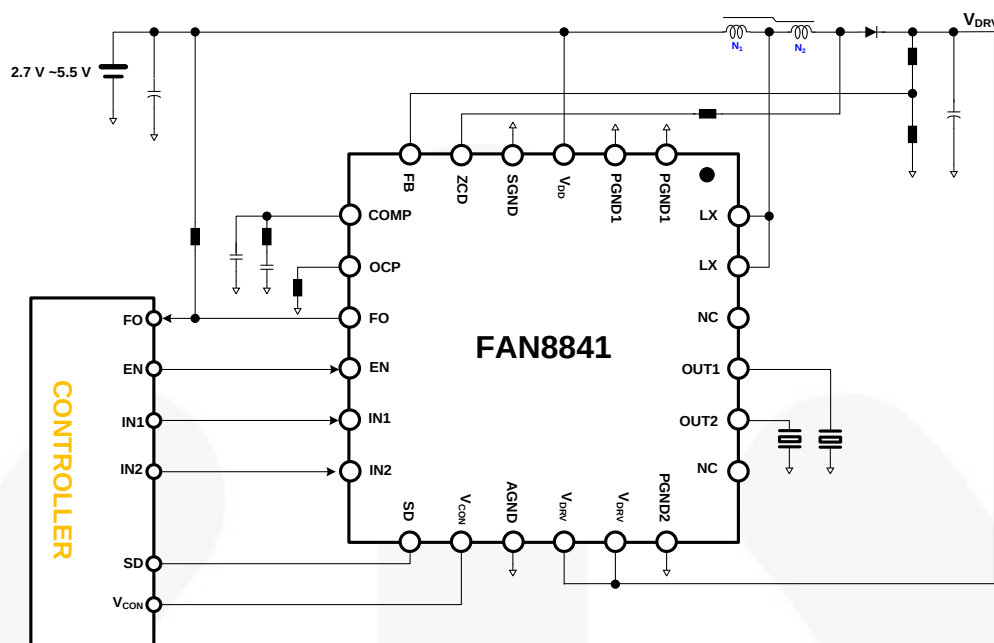


Figure 1. Typical Application Circuit for Piezo Actuator Driver

## Block Diagram

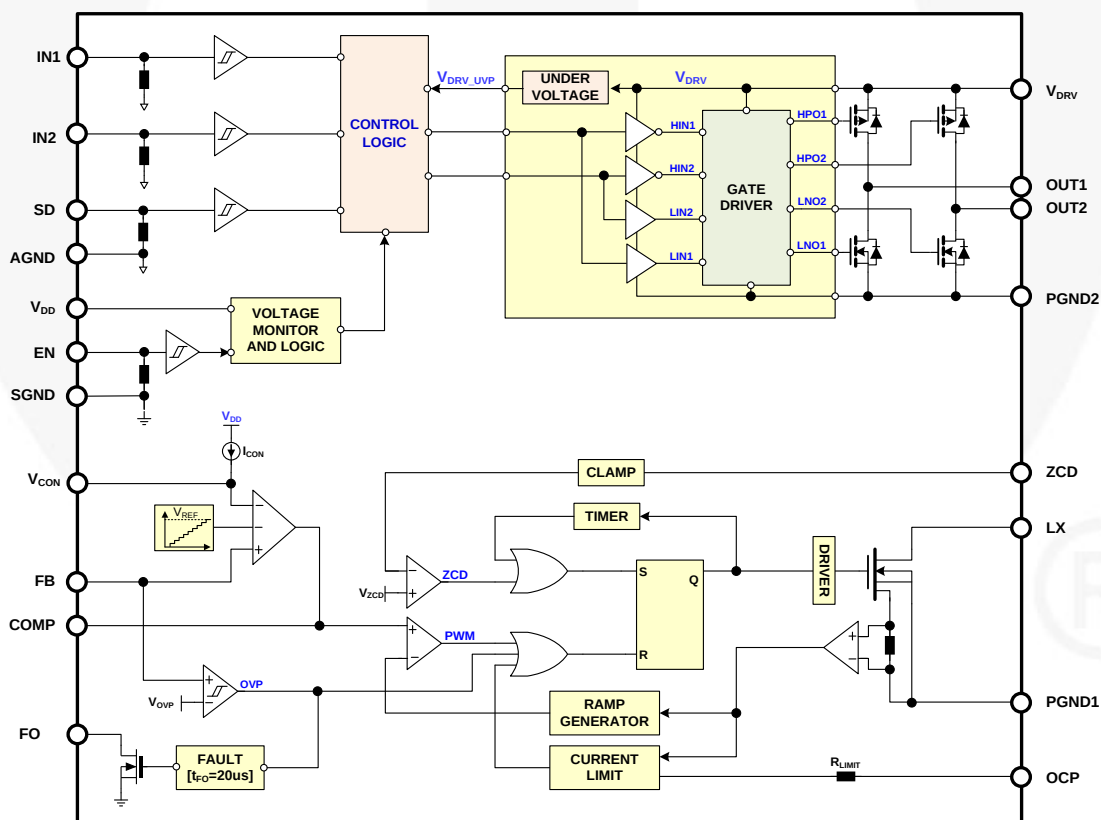


Figure 2. Block Diagram

## Pin Configuration

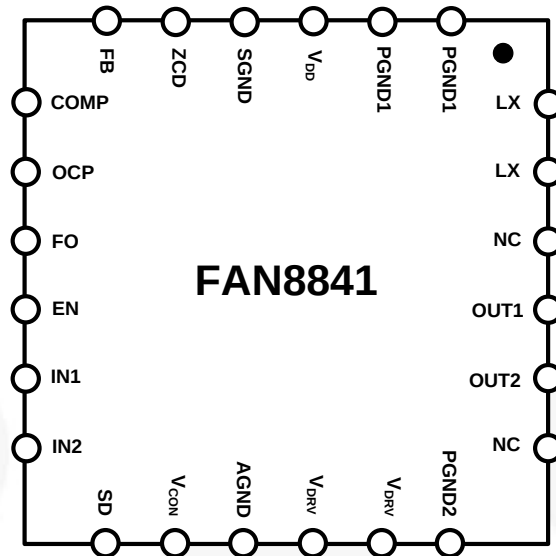


Figure 3. Pin Assignment

## Pin Definitions

| Pin #  | Name             | Description                                                                   |
|--------|------------------|-------------------------------------------------------------------------------|
| 1, 2   | PGND1            | Power Ground 1. It is connected to the source of the step-up switch.          |
| 3      | V <sub>DD</sub>  | Power supply of step-up DC-DC converter.                                      |
| 4      | SGND             | Signal Ground. The signal ground for step-up DC-DC converter circuitry.       |
| 5      | ZCD              | The input of the Zero Current Detection                                       |
| 6      | FB               | Step-up DC-DC converter output voltage feedback input.                        |
| 7      | COMP             | Output of the transconductance error amplifier.                               |
| 8      | OCP              | Sets Step-up DC-DC converter current limit                                    |
| 9      | FO               | Fault Output.                                                                 |
| 10     | EN               | Enable pin to turn on and off the overall system. (Active Low Shutdown Mode). |
| 11     | IN1              | Logic input for Half-Bridge 1                                                 |
| 12     | IN2              | Logic input for Half-Bridge 2                                                 |
| 13     | SD               | Shutdown input for H-Bridge 1 and 2. (Active Low Shutdown Mode).              |
| 14     | V <sub>CON</sub> | Control input for output voltage of step-up DC-DC converter                   |
| 15     | AGND             | Analog Ground. The signal ground for H-bridge driver circuitry                |
| 16, 17 | V <sub>DRV</sub> | Power supply of each H-bridge driver                                          |
| 18     | PGND2            | Power Ground 2. The power ground for Half-bridge driver                       |
| 19     | NC               | Not Connected                                                                 |
| 20     | OUT2             | Output for Half-bridge 2                                                      |
| 21     | OUT1             | Output for Half-bridge 1                                                      |
| 22     | NC               | Not Connected                                                                 |
| 23, 24 | LX               | Switch Node. This pin is connected to the inductor.                           |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol             | Parameter                                                 |                                       | Min. | Max.                 | Unit |
|--------------------|-----------------------------------------------------------|---------------------------------------|------|----------------------|------|
| V <sub>DRV</sub>   | DC Link Input Voltage Drain-Source Voltage of each MOSFET |                                       |      | 75                   | V    |
| V <sub>DD</sub>    | DC Supply Voltage for DC-DC Converter                     |                                       | -0.3 | 5.5                  | V    |
| V <sub>INPUT</sub> | EN, SD, IN1, IN2, FB and COMP to SGND and AGND            |                                       | -0.3 | V <sub>DD</sub> +0.3 | V    |
| V <sub>CON</sub>   | V <sub>CON</sub> to SGND                                  |                                       | -0.3 | V <sub>DD</sub> +0.3 | V    |
| V <sub>LX</sub>    | LX to PGND                                                |                                       | -0.3 | 40                   | V    |
| P <sub>D</sub>     | Power Dissipation <sup>(2)</sup>                          | 1S0P with thermal vias <sup>(3)</sup> |      | 0.98                 | W    |
|                    |                                                           | 1S2P with thermal vias <sup>(4)</sup> |      | 2.9                  |      |
| θ <sub>JA</sub>    | Thermal Resistance Junction-Air <sup>(1)</sup>            | 1S0P with thermal vias <sup>(3)</sup> |      | 127                  | °C/W |
|                    |                                                           | 1S2P with thermal vias <sup>(4)</sup> |      | 43                   |      |
| T <sub>A</sub>     | Operating Ambient Temperature Range                       |                                       | -40  | 125                  | °C   |
| T <sub>J</sub>     | Operating Junction Temperature                            |                                       | -55  | 150                  | °C   |
| T <sub>STG</sub>   | Storage Temperature Range                                 |                                       | -55  | 150                  | °C   |
| ESD                | Electrostatic Discharge Capability                        | Human Body Model, JESD22-A114         |      | 2                    | KV   |
|                    |                                                           | Charged Device Model, JESD22-C101     |      | 500                  | V    |

### Notes:

1. All voltage values, except differential voltages, are given with respect to SGND, AGND and PGND pin.
2. JEDEC standard: JESD51-2, JESD51-3. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
3. 1S0P with thermal via: one signal layer with zero power plane and thermal via.
4. 1S2P with thermal via: one signal layer with two power plane and thermal via.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol           | Parameter                                 | Min. | Max.            | Unit |
|------------------|-------------------------------------------|------|-----------------|------|
| V <sub>DRV</sub> | Supply Voltage for Half-Bridge Driver     | 13   | 60              | V    |
| V <sub>LX</sub>  | Boost Switch Voltage                      |      | 36              | V    |
| V <sub>CON</sub> | Output Voltage Control of DC-DC Converter | 0.1  | V <sub>DD</sub> | V    |
| V <sub>DD</sub>  | Operating Voltage for DC-DC Converter     | 2.8  | 5.0             | V    |
| R <sub>OCP</sub> | Current Limit Control Resistor            | 3.3  | 150             | kΩ   |

## Electrical Characteristics

$V_{DD}=3.0\text{ V}$ ,  $V_{DRV}=60\text{ V}$ , and  $T_A=-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . Typical values  $T_A=25^\circ\text{C}$ , unless otherwise specified.

| Symbol                                                     | Parameter                                       | Conditions                                           | Min.  | Typ. | Max. | Unit            |
|------------------------------------------------------------|-------------------------------------------------|------------------------------------------------------|-------|------|------|-----------------|
| <b>Power Supply Section</b>                                |                                                 |                                                      |       |      |      |                 |
| $I_{Q,DD}$                                                 | Quiescent Current for $V_{DD}$ <sup>(5)</sup>   | $V_{EN}=V_{COMP}=V_{DD}$ ,                           |       | 800  | 1200 | $\mu\text{A}$   |
| $I_{Q,DRV}$                                                | Quiescent Current for $V_{DRV}$                 | $V_{FB}=1.0\text{ V}$ , $V_{IN1}=V_{IN2}=0\text{ V}$ |       | 400  | 800  | $\mu\text{A}$   |
| $I_{SD,DD}$                                                | Shutdown Current for $V_{DD}$                   | $V_{EN}=0\text{ V}$ ,                                |       |      | 1    | $\mu\text{A}$   |
| $I_{SD,DRV}$                                               | Shutdown Current for $V_{DRV}$                  | $V_{DD}=V_{DRV}=3\text{ V}$                          |       | 8    | 15   | $\mu\text{A}$   |
| $V_{DDSTART}$                                              | Start Threshold Voltage                         |                                                      | 2.6   | 2.7  | 2.8  | V               |
| $V_{DDUVHYS}$                                              | $V_{DD}$ UVLO Hysteresis Voltage                |                                                      | 0.10  | 0.2  |      | V               |
| <b>Error Amplifier Section</b>                             |                                                 |                                                      |       |      |      |                 |
| $V_{FB}$                                                   | Feedback Reference Voltage                      | $T_A=25^\circ\text{C}$                               | 0.99  | 1.00 | 1.01 | V               |
| $I_{FB}$                                                   | FB pin Bias Current                             | $V_{FB}=0\text{ V} \sim 2\text{ V}$                  |       |      | 1    | $\mu\text{A}$   |
| $\Delta V_{FB1}$                                           | Feedback Voltage Line Regulation <sup>(6)</sup> | $2.7\text{ V} < V_{DD} < 5\text{ V}$ ,               |       | 0.5  | 1.5  | %/V             |
| $G_m$                                                      | Transconductance                                | $T_A=25^\circ\text{C}$                               |       | 800  |      | $\mu\text{mho}$ |
| <b>Zero Current Detect Section</b>                         |                                                 |                                                      |       |      |      |                 |
| $V_{ZCD}$                                                  | Input Voltage Threshold <sup>(7)</sup>          |                                                      | 1.65  | 1.83 | 2.00 | V               |
| $V_{CLAMPH}$                                               | Input High Clamp Voltage                        | $I_{DET}=2.3\text{ mA}$                              | 3.0   | 3.5  | 4.0  | V               |
| $V_{CLAMPL}$                                               | Input Low Clamp Voltage                         | $I_{DET}=-2.3\text{ mA}$                             | -0.30 | 0.12 | 0.50 | V               |
| $I_{ZCD,SR}$                                               | Source Current Capability                       |                                                      |       |      | -2.3 | mA              |
| $I_{ZCD,SK}$                                               | Sink Current Capability                         |                                                      |       |      | 2.3  | mA              |
| $t_{ZCD,D}$                                                | Delay From ZCD to Output Turn-On <sup>(7)</sup> |                                                      |       | 50   | 200  | ns              |
| <b>Maximum On-Time Section</b>                             |                                                 |                                                      |       |      |      |                 |
| $t_{ON,MAX}$                                               | Maximum On-Time                                 |                                                      | 15    | 25   | 35   | $\mu\text{s}$   |
| <b>Soft-Start Timer Section</b>                            |                                                 |                                                      |       |      |      |                 |
| $t_{SS}$                                                   | Internal Soft-Start                             |                                                      | 16    | 28   | 40   | ms              |
| <b>Restart / Maximum Switching Frequency Limit Section</b> |                                                 |                                                      |       |      |      |                 |
| $t_{RST}$                                                  | Restart Timer                                   |                                                      | 15    | 25   | 35   | $\mu\text{s}$   |
| $f_{MAX}$                                                  | Maximum Switching Frequency <sup>(7)</sup>      |                                                      |       | 900  | 1000 | KHz             |

### Notes:

- This is only the  $V_{DD}$  current consumption with no switching condition. It does not include gate-drive current.
- The line regulation is calculated based on  $\frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{1}{V_{OUT}}$ .
- This parameter, although guaranteed by design, is not tested in production.

## Electrical Characteristics

$V_{DD}=3.0\text{ V}$ ,  $V_{DRV}=60\text{ V}$ , and  $T_A=-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Typical values  $T_A=25^{\circ}\text{C}$ , unless otherwise specified.

| Symbol                           | Parameter                                            | Conditions                                       | Min. | Typ. | Max. | Unit |
|----------------------------------|------------------------------------------------------|--------------------------------------------------|------|------|------|------|
| Current Limit Comparator Section |                                                      |                                                  |      |      |      |      |
| I <sub>OCP</sub>                 | OCP Trip Current                                     | R <sub>OCP</sub> =3.3 KΩ, V <sub>DD</sub> =3.3 V | 1.85 | 2.00 | 2.15 | A    |
|                                  |                                                      | R <sub>OCP</sub> =22 KΩ, V <sub>DD</sub> =3.3 V  | 0.9  | 1.0  | 1.1  | A    |
| t <sub>CS_BLANK</sub>            | Comparator Leading-Edge Blanking Time <sup>(8)</sup> |                                                  | 80   | 130  | 180  | ns   |
| Step-up Output Control Section   |                                                      |                                                  |      |      |      |      |
| I <sub>CON</sub>                 | Internal Current Source for V <sub>CON</sub> Pin     | T <sub>A</sub> =25°C                             | 9.0  | 10   | 11   | μA   |
| V <sub>CON+</sub>                | Positive Going Threshold Voltage <sup>(8)</sup>      |                                                  |      | 1.0  |      | V    |
| V <sub>CON-</sub>                | Negative Going Threshold Voltage <sup>(8)</sup>      |                                                  |      | 0.1  |      | V    |
| Step-up Switch Section           |                                                      |                                                  |      |      |      |      |
| R <sub>DSON</sub>                | N-Channel On Resistance                              | V <sub>DD</sub> =3.3 V, T <sub>A</sub> =25°C     |      | 0.2  | 0.5  | Ω    |
| I <sub>LK_LX</sub>               | LX Leakage Current                                   | V <sub>LX</sub> =36 V                            |      |      | 1.0  | μA   |
| Logic (EN, IN1, IN2, SD) Section |                                                      |                                                  |      |      |      |      |
| V <sub>INPUT+</sub>              | Input Logic High Threshold Voltage                   |                                                  | 1.34 |      |      | V    |
| V <sub>INPUT-</sub>              | Input Logic Low Threshold Voltage                    |                                                  |      |      | 0.5  | V    |
| I <sub>INPUT-</sub>              | Input Low Current                                    | V <sub>EN</sub> =0 V                             |      |      | 1    | μA   |
| I <sub>INPUT+</sub>              | Input High Current                                   | V <sub>EN</sub> =V <sub>DD</sub>                 | 16   | 24   | 32   | μA   |
| R <sub>INPUT</sub>               | Input Logic Pull-Down Resistance                     | V <sub>EN</sub> =V <sub>INPUT</sub> =3 V         |      | 125  |      | KΩ   |
| Full-Bridge Switch Section       |                                                      |                                                  |      |      |      |      |
| R <sub>DS,ONP</sub>              | Output Upper-Side On Resistance                      | T <sub>A</sub> =25°C                             |      | 3.0  | 5.0  | Ω    |
| R <sub>DS,ONN</sub>              | Output Low-Side On Resistance                        |                                                  |      | 3.0  | 5.0  | Ω    |
| t <sub>ON</sub>                  | Turn-on Propagation Delay Time                       | V <sub>DRV</sub> =30 V, T <sub>A</sub> =25°C     |      | 300  |      | ns   |
| t <sub>OFF</sub>                 | Turn-off Propagation Delay Time                      |                                                  |      | 330  |      | ns   |
| Protection (UVP, and OVP )       |                                                      |                                                  |      |      |      |      |
| V <sub>UVP</sub>                 | Under-Voltage Threshold of DC-DC Con.                |                                                  | 11   | 12   | 13   | V    |
| HY <sub>UVP</sub>                | Under-Voltage Hysteresis                             |                                                  |      | 1.0  |      | V    |
| V <sub>OVP</sub>                 | OVP Threshold Voltage                                |                                                  | 1.05 | 1.10 | 1.15 | V    |
| HY <sub>OVP</sub>                | OVP Hysteresis Voltage                               |                                                  |      | 0.1  |      | V    |
| t <sub>FO</sub>                  | Fault Output Duration                                |                                                  |      | 20   | 30   | μs   |
| V <sub>FOL</sub>                 | Fault Output Low Level voltage                       | R <sub>PU</sub> =50 KΩ, V <sub>PU</sub> =3 V     |      | 0.1  | 0.4  | V    |

### Note:

8. This parameter, although guaranteed by design, is not tested in production.

## Design Consideration Information

Figure 4 shows the timing chart for overall system.

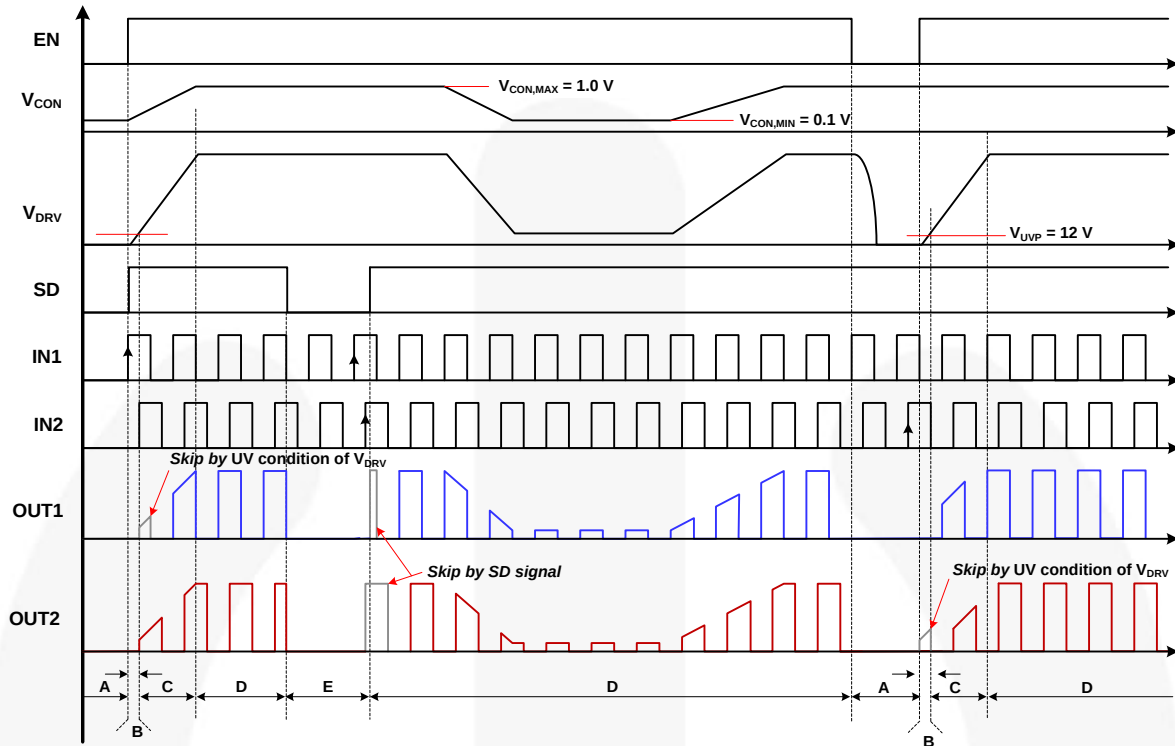


Figure 4. Timing Chart of Overall System

Table 1. Operating Modes

| Input |     |    |    | Output |      | Mode  |                      |          |
|-------|-----|----|----|--------|------|-------|----------------------|----------|
| IN1   | IN2 | EN | SD | OUT1   | OUT2 | State | DC-DC                | H-Bridge |
| X     | X   | L  | X  | L      | L    | A     | Whole System Disable |          |
| X     | X   | H  | L  | L      | L    | E     | Active               | Disable  |
| L     | L   | H  | H  | L      | L    | D     | Normal Operation     |          |
| L     | H   |    |    | L      | H    |       |                      |          |
| H     | L   |    |    | H      | L    |       |                      |          |
| H     | H   |    |    | H      | H    |       |                      |          |

### Notes:

9. X: Don't care (L or H).
10. EN: Whole system is disable mode when EN is LOW state.
11. Soft-start duration: C, under-voltage condition of V<sub>DRV</sub>: B.

## Typical Performance Characteristics

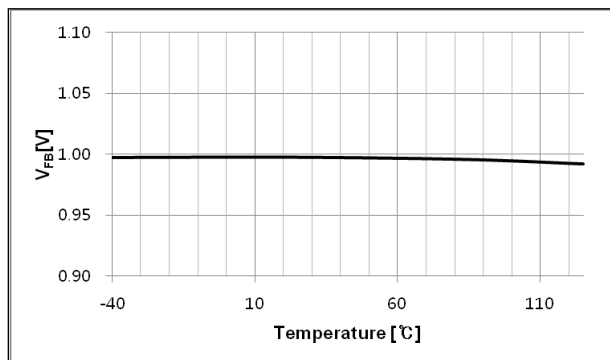


Figure 5. Reference Voltage vs. Temperature

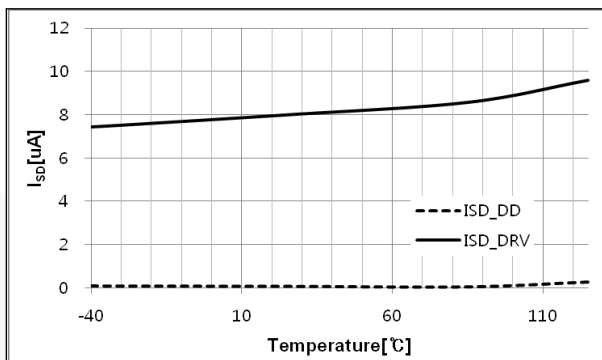


Figure 6. Shutdown Current for  $V_{DD}$  &  $V_{DRV}$  vs. Temperature

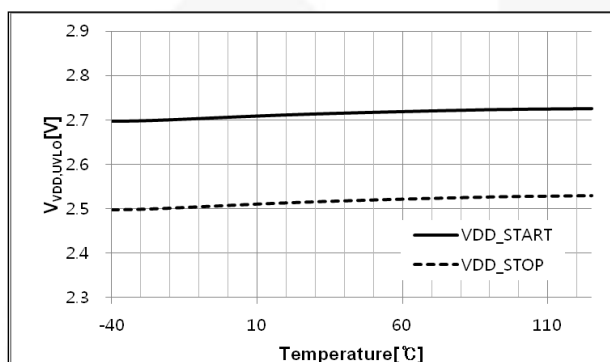


Figure 7.  $V_{DD}$  Threshold vs. Temperature

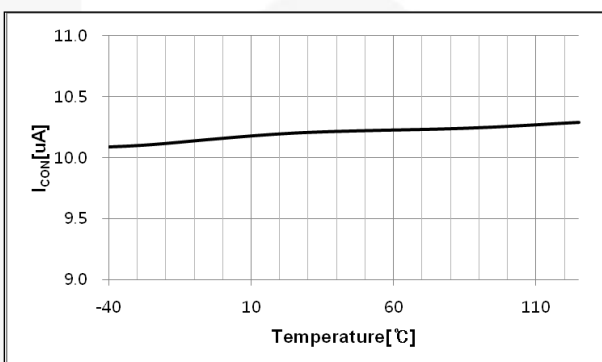


Figure 8.  $V_{CON}$  Current vs. Temperature

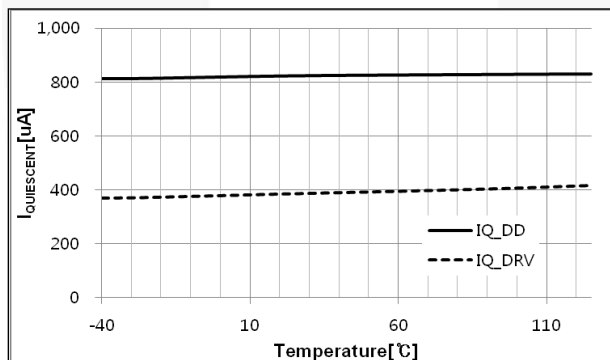


Figure 9. Quiescent Current for  $V_{DD}$  &  $V_{DRV}$  vs. Temperature

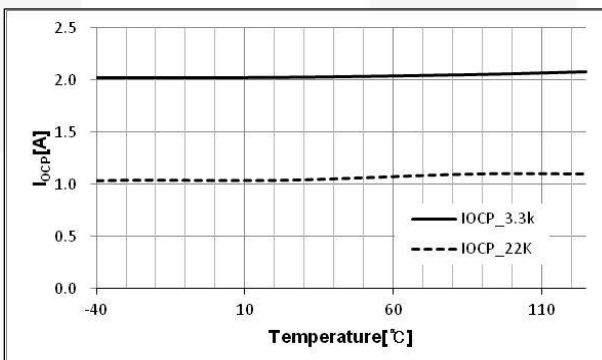


Figure 10. OCP Current vs. Temperature

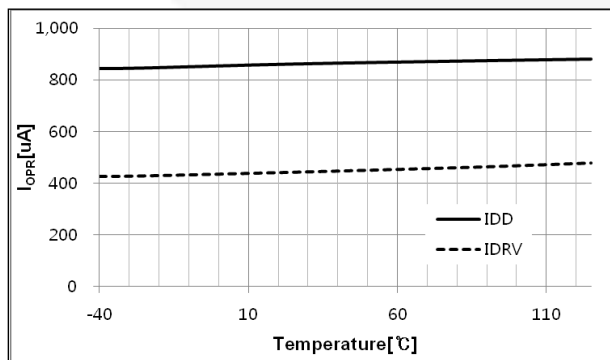


Figure 11. Operating Current for  $V_{DD}$ ,  $V_{DRV}$ , &  $V_{IN}$

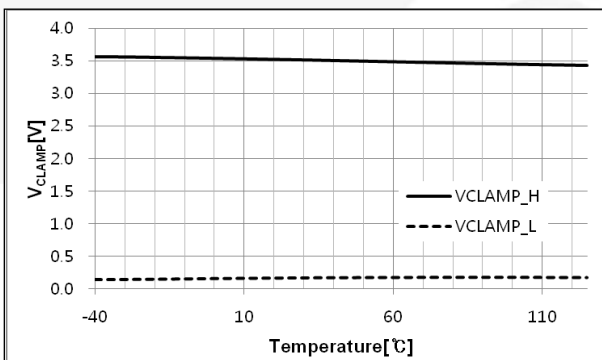


Figure 12. ZDC Clamp Voltage vs. Temperature

vs. Temperature

# Typical Performance Characteristics (Continued)

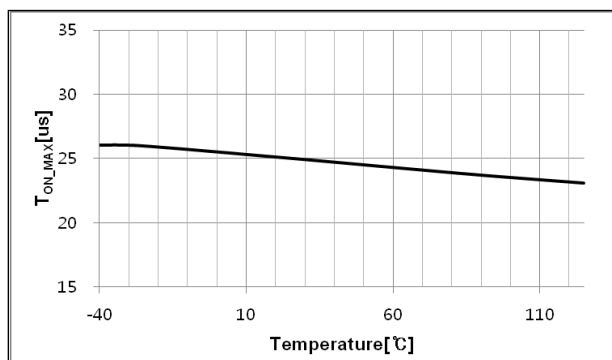


Figure 13. Maximum On-Time vs. Temperature

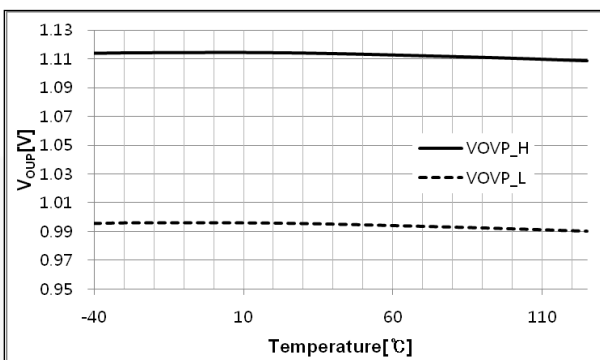


Figure 14. OVP (FB) vs. Temperature

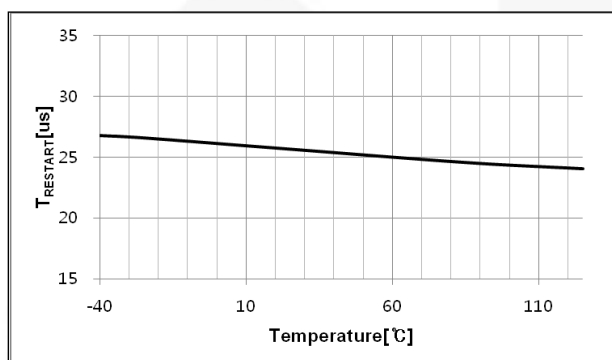


Figure 15. Restart-Time vs. Temperature

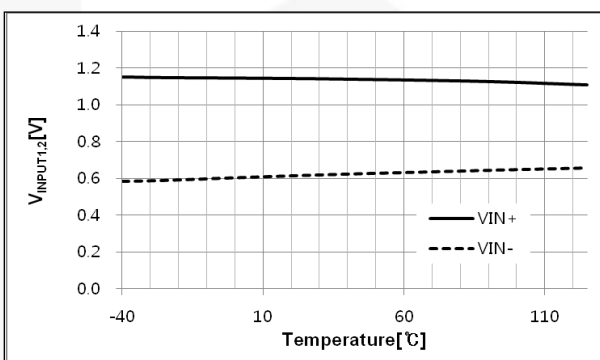


Figure 16. INPUT Threshold vs. Temperature

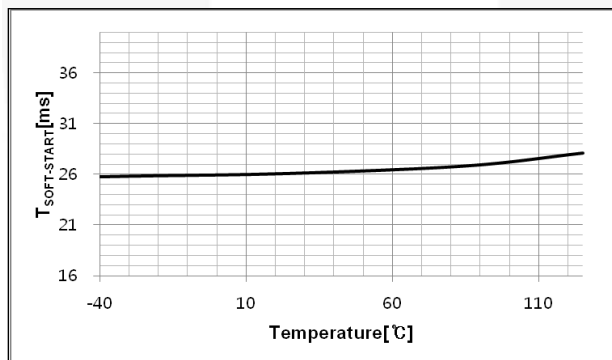


Figure 17. Soft-Start Time vs. Temperature

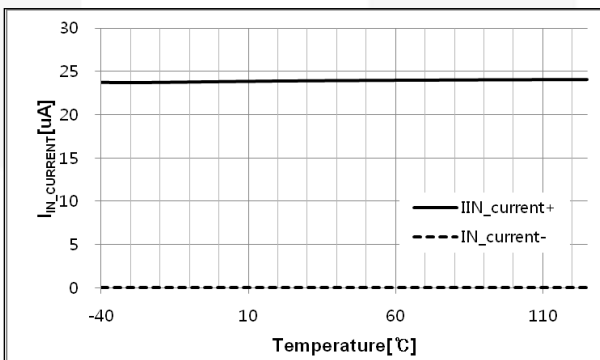


Figure 18. INPUT Logic Current vs. Temperature

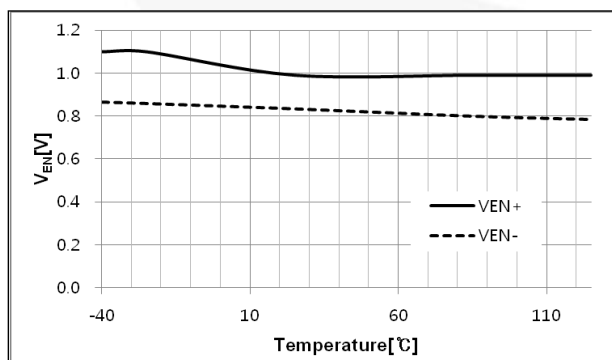


Figure 19. Enable(EN) Threshold Voltage vs. Temperature

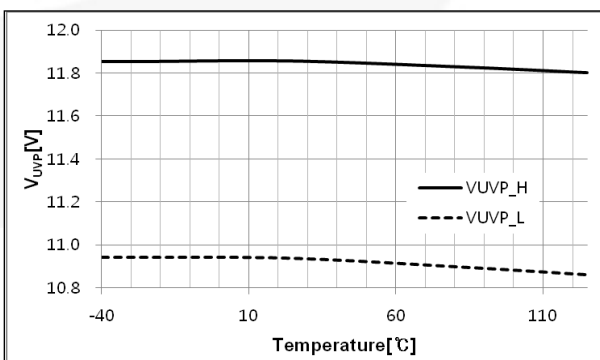


Figure 20. V\_DRV UVP Threshold Voltage vs. Temperature

## Typical Performance Characteristics (Continued)

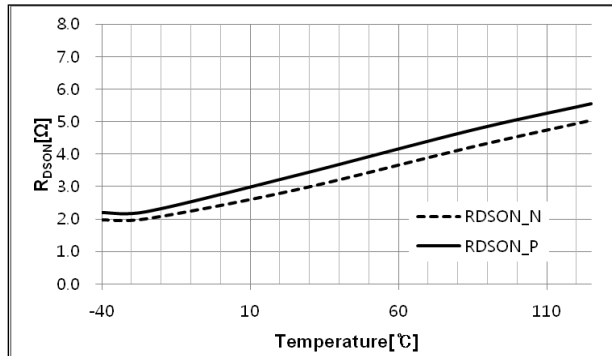


Figure 21. Half-Bridge Switch  $R_{DS(on)}$  vs. Temperature

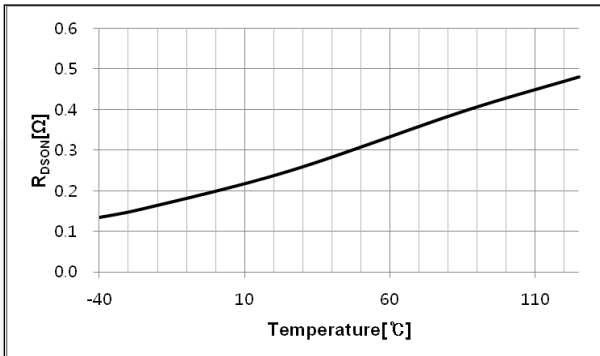


Figure 22. Boost Switch  $R_{DS(on)}$  vs. Temperature

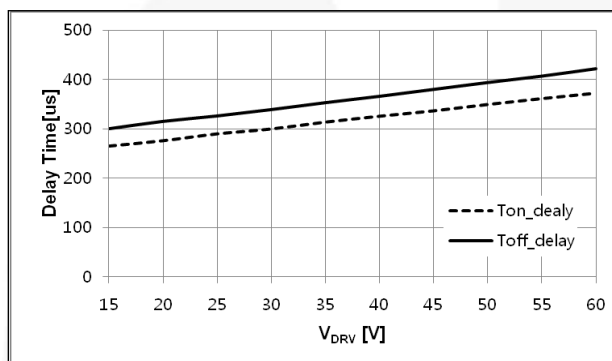


Figure 23. OUT1/2 Delay vs.  $V_{DRV}$

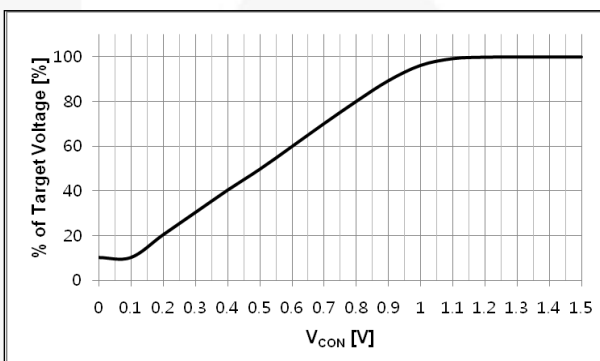


Figure 24. % of OUT Amplitude vs.  $V_{CON}$

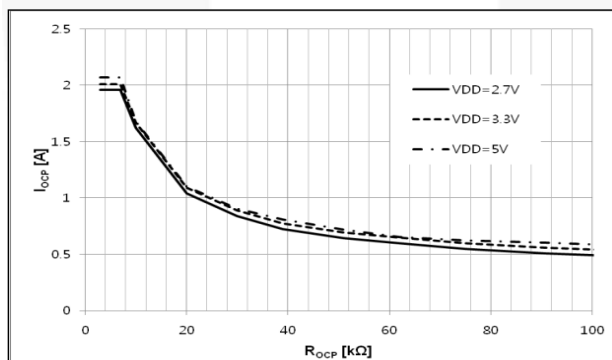


Figure 25.  $I_{OCP}$  vs.  $R_{OCP}$

## Functional Description

The FAN8841 has a basic PWM controller for Step-up DC-DC converter topology in Critical Conduction Mode (CRM) and integrated Dual half-bridge drivers. To increase efficiency of the DC-DC converter, FAN8841 has a Zero Current Detection (ZCD) function for CRM control. It can reduce Step-up DC-DC converter switching loss at MOSFET turn on time. The FAN8841 Step-up DC-DC converter supports output voltage up to 36 V with the use of a commercial inductor since the absolute maximum voltage of internal switching FET  $V_{DS}$  is 40 V. If the use requires a driving voltage higher than 36 V, it is recommended to use a coupled inductor, since the internal half-bridge absolute maximum voltage is 75 V.

The device architecture is that of a current mode controller with an internal sensing resistor connected in series with the NMOS switch. The voltage at the feedback pin tracks the output voltage at the cathode of the external Schottky diode. The internal error amplifier amplifies the difference between the feedback voltage and the internal reference voltage. Its error signal is applied to the input of a compensator and is compared to the current of the main switch which produces the appropriate duty cycle of the main switch in the inner loop. The amplified error voltage serves as a reference voltage to the internal PWM comparator. The PWM comparator resets the latch when the RAMP generator signal meets the error amp output level. The ZCD signal sets the latch and the SR latch turns on the FET switch. Since the comparator input contains information about the output voltage and the control loop is arranged to form a negative feedback loop, the value of the peak inductor current is adjusted to the driving power.

Every time the latch is reset, the FET is turned off and the current flow through the switch is terminated. The latch can be reset by other events as well. Over-current condition is monitored by the current limit comparator which resets the latch and turns off the switch instantaneously within each clock cycle.

## Soft Startup

The FAN8841 has a Soft Startup function to prevent inrush current during the Step-up DC-DC converter startup. When the EN pin voltage goes HIGH from LOW, the Step-up DC-DC converter is turned on, the COMP is pre-charged, and inverting input of the internal error amplifier reference voltage starts up gradually with regular slope. This time is typically 28 ms at the maximum  $V_{CON}$ .

## Adjustable $V_{DRV}$ Voltage ( $V_{CON}$ Control)

The FAN8841 can control the Step-up DC-DC converter output voltage without changing the resistive feedback divider using the  $V_{CON}$  pin. The  $V_{CON}$  is controlled directly by the external DC voltage or external resistance value.  $V_{CON}$  control range is fixed from 0.1 to 1.0 V. If  $V_{CON}$  voltage decreases below 0.1 V or increases higher than 1.0 V,  $V_{DRV}$  voltage fixed on minimum or maximum voltage due to the internal clamp level. If the user wants a fixed  $V_{DRV}$  voltage, it is

recommended that the  $V_{CON}$  pin is connected with  $V_{DD}$  voltage.

## Zero Current Detection (ZCD)

The Step-up DC-DC converter of the FAN8841 operates in CRM method with ZCD function. The ZCD is detected instantly when the inductor current goes to zero voltage switching operation. Once the boost inductor current becomes zero, the output capacitor of the main FET ( $C_{OSS}$ ) and the magnetizing inductor of the coupled inductor ( $L1$ ) resonate together, and the drain voltage of the main switch decreases, as shown in Figure 26. Since the ZCD pin can be connected to the switching diode anode, the FAN8841 detects when the diode anode voltage reaches its minimum value directly. The threshold voltage to detect the anode voltage inside the ZCD pin is typically 1.83 V. Therefore, the next switching begins after the anode voltage reaches 1.83 V, and has a 200 ns maximum delay to the next gate turn-on.

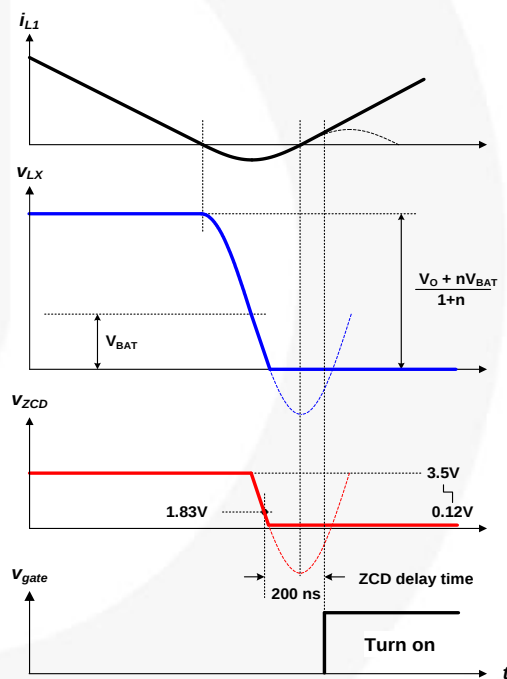


Figure 26. Waveforms for ZCD

The resistor  $R_{ZCD}$  is obtained as follows:

$$R_{ZCD} \geq \frac{(V_{DRV} + 0.7) - V_{CLAMPH}}{I_{ZCD}} \quad (1)$$

## Over-Current Protection (OCP)

The Over-Current Protection (OCP) function of the FAN8841 limits the inductor peak current of the Step-up DC-DC converter via an external resistor  $R_{OCP}$ . The adjustable current limit should be less than the rated saturation limit of the inductor by the user to avoid the damage to both the inductor and FAN8841.

## V<sub>DRV</sub> Under-Voltage Protection

The driving voltage of the internal dual Half-bridge is received from the V<sub>DRV</sub> pin. The internal 5 V LDO for driving the internal gate driver is also received from the V<sub>DRV</sub> pin. For supplying a stable power to the internal gate driver, V<sub>DRV</sub> has an under-voltage protection function. If the V<sub>DRV</sub> voltage is less than 11 V typically, during normal operation, the internal gate driver is turned off. When the V<sub>DRV</sub> voltage exceeds 12 V typically, the internal gate driver is turned on.

## Over-Voltage Protection (OVP)

The FAN8841 features a unique V<sub>DRV</sub> monitoring to maximize the safety when the feedback voltage is higher than the specified threshold voltage. The OVP comparator shuts down the output drive block when the voltage of the FB pin is higher than 1.1 V.

At the normal operating condition, Fault Out signal maintains on V<sub>DD</sub> voltage, but the abnormal over-voltage has occurred at V<sub>DRV</sub>, Fault Out signal goes low during typ. 20  $\mu$ s.

## Application information

### Setting the Output Voltage

The internal reference is 1.0 V (Typical) and it controlled by the V<sub>CON</sub> voltage. The output voltage is divided by the external resistor divider, R<sub>FB1</sub> and R<sub>FB2</sub> to the FB pin. The output voltage is given by:

$$V_{DRV} = V_{REF} \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad (2)$$

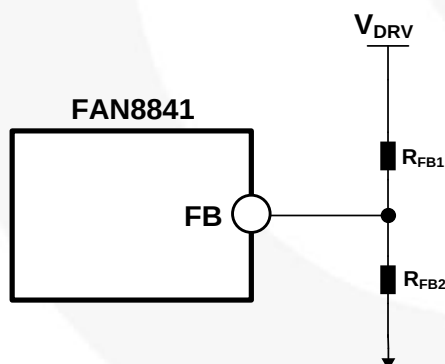


Figure 27. Feedback Circuit

### Inductor Selection

To prevent the absolute maximum voltage in the operating condition, the switching voltage V<sub>LX</sub> should be lower than 36 V, as shown in Figure 28.

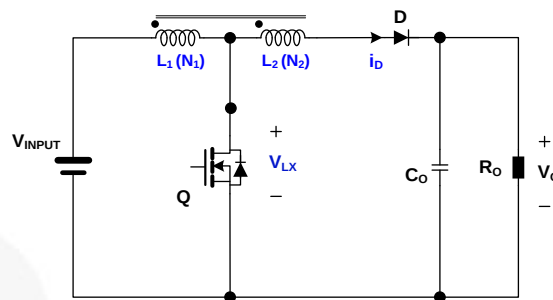


Figure 28. Schematic of Coupled Inductor Boost Converter

V<sub>LX</sub> is determined by the output voltage, input voltage and coupled inductor turn ratio. The V<sub>LX</sub> voltage is calculated as follows:

$$V_{LX} = V_{INPUT} + \frac{V_O - V_{INPUT}}{n + 1} = \frac{V_O + nV_{INPUT}}{n + 1} \quad (3)$$

Therefore, the turn's ratio can be easily obtained as the following equations:

$$n = \frac{V_O - V_{LX}}{V_{LX} - V_{INPUT}} \quad (4)$$

To determine the turn's ratio, the input voltage variation has to be considered as well.

The inductor parameters are directly related to the device performance, saturation current and DC resistance. The lower the DC resistance, the higher efficiency. Usually a trade-off between inductor size, cost and overall efficiency is needed to make the optimum choice.

The inductor saturation current should be rated around 2 A at maximum power in the FAN8841. If to use a low saturation current inductor under 2 A due to inductor size, it is possible using the OCP level control.

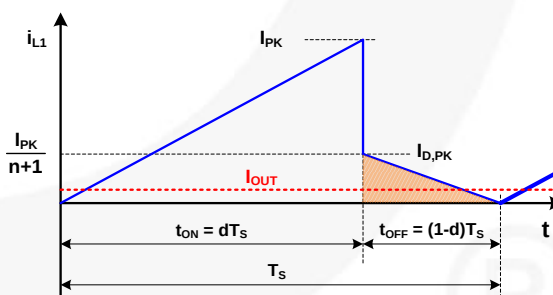


Figure 29. Current Waveform

In CRM operation, the inductance can be obtained from the slope of the inductor current, as shown in Figure 29. During FET turn off period, the inductor current flows through the diode. The diode peak current is expressed as follows:

$$I_{D,PK} = \frac{2I_{OUT}}{1 - d} \quad (5)$$

And then, the peak current of the main switch is obtained as follows:

$$I_{PK} = \frac{2I_{OUT}(1+n)}{1-d}, \text{ or } I_{PK} = \frac{V_{INPUT}}{L_1} dT_s \quad (6)$$

The inductance value obtained as follows:

$$L_1 = \frac{V_{INPUT} dT_s}{I_{PK}} = \frac{V_{INPUT} d(1-d)T_s}{2I_{OUT}(1+n)} \quad (7)$$

If a user wants a commercial inductor at output voltage under 35 V condition, n(turns ratio at using coupled inductor) should be substituted the value zero, (turns ratio at using coupled inductor).

### Output Capacitor Selection

The value of the output capacitor can be selected based on the output voltage ripple requirements. Without consideration of the effect of Equivalent Series Resistance (ESR) as output capacitors, the output voltage ripple in a peak-to-peak manner is obtained as follows:

$$V_{ripple,pp} = \frac{\left(2d + \frac{(1-d)^2}{2}\right) \cdot I_{OUT} \cdot T_s}{2C_O} \quad (8)$$

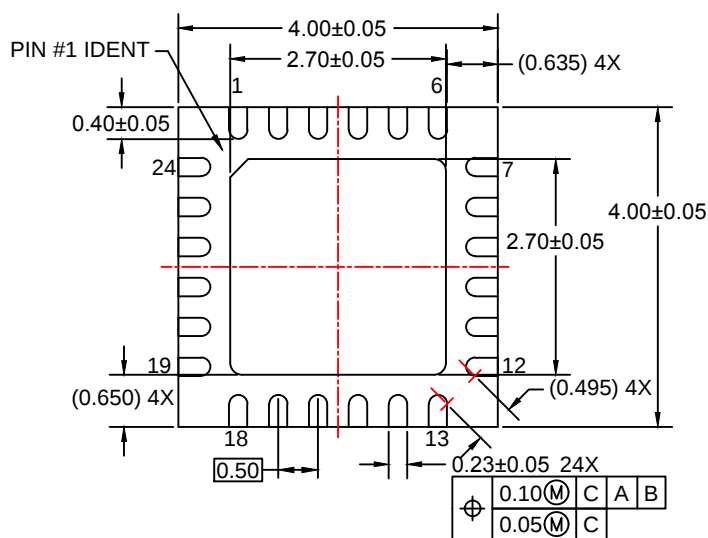
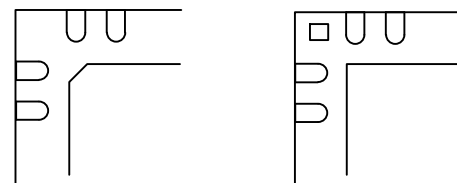
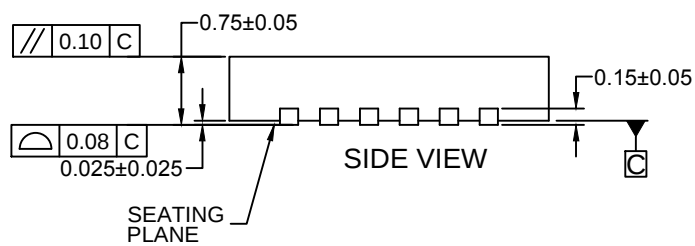
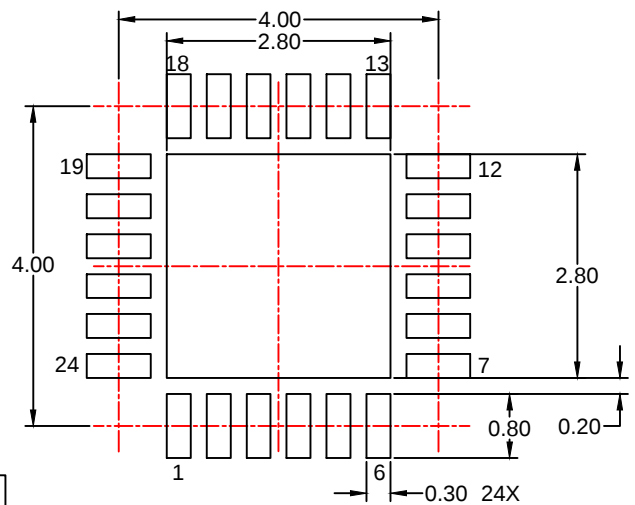
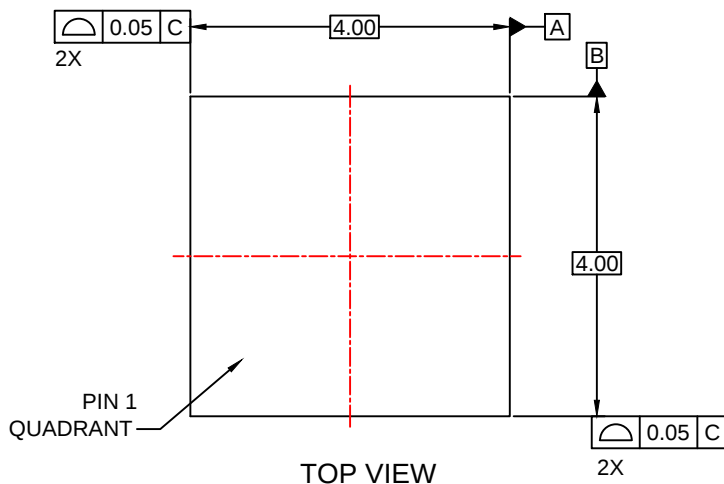
where  $V_{ripple,pp}$  is the output voltage ripple in peak-to-peak manner. Therefore, the output capacitance can be selected with the given output voltages ripple specification as follows:

$$C_O \geq \frac{\left(2d + \frac{(1-d)^2}{2}\right) \cdot I_{OUT} \cdot T_s}{2V_{ripple,pp}} \quad (9)$$

### Diode Selection

The external diode used for the rectification is usually a Schottky diode. It's average forward current and reverse voltage maximum ratings should exceed the load current and the voltage at the output of the converter respectively.

A care should be taken to avoid any short circuit of  $V_{OUT}$  to GND, even with the IC disabled, since the diode can be instantly damaged by the excessive current.



#### NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WGGD-6.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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