Synchronous TINYBOOST® Regulator with Bypass Mode, 2500 mA

FAN48623

WLCSP16 1.81 × 1.81 × 0.586
CASE 567QZ

Description

The FAN48623 allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built−in power transistors, synchronous rectification, and low supply current, this IC provides a compact solution for systems using advanced Li−Ion battery chemistries.

The FAN48623 is a boost regulator designed to provide a minimum output voltage from a single−cell Li−Ion battery, even when the battery voltage is below system minimum. The output voltage regulation is guaranteed up to a maximum load current of 2500 mA. The regulator transitions smoothly between Bypass and normal Boost Mode. The device can be forced into Bypass Mode to reduce quiescent current.

The FAN48623 is available in a 16−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

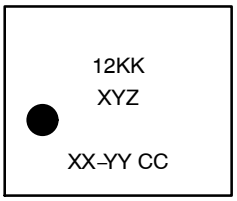
Features

- Maximum Continuous Load Current: 2500 mA at V_{IN} of 2.5 V Boosting V_{OUT} to 3.3 V
- Maximum Pulse Load Current of 3.5 A for GSM PAs (1 Slot) and PMIC Support Simultaneously, V_{IN} = 3.1 V, V_{OUT} = 3.4 V
- Up to 97% Efficient
- 4 External Components: 2520 case 0.47 μH Inductor and 0603 Case Size Input and Output Capacitors
- Input Voltage Range: 2.5 V to 5.5 V
- Fixed Output Voltage Options: 3.0 V to 5.0 V
- True Bypass Operation when V_{IN} > Target V_{OUT}
- Integrated Synchronous Rectifier
- True Load Disconnect
- Forced Bypass Mode
- V_{SEL} Control to Optimize Target V_{OUT}
- Short−Circuit Protection (SCP)
- Low Operating Quiescent Current
- 16−Bump, 1.81 mm x 1.81 mm, 0.4 mm Pitch, WLCSP
- This is a Pb−Free Device

Applications

- Boost for Low−Voltage Li−ion Batteries, Brownout Prevention, System PMIC LDOs Supplies, and 2G/3G/4G RF PA Supplies
- Smart Phones, Tablets, Portable Devices

MARKING DIAGRAM



Line 1:
12 = Device Marking Code
(See Ordering Information for specific device code)
KK = Lot Run Code

Line 2:
XY = 2−Date Code
Z = Assembly Plant Code

Line 3: **onsemi** internal use only

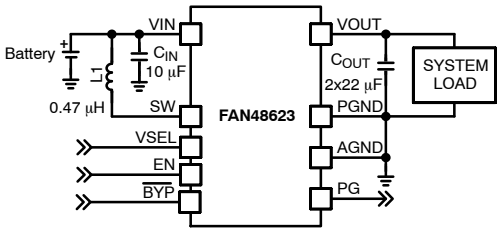


Figure 1. Typical Application

ORDERING INFORMATION

See detailed ordering and shipping information on page 16 of this data sheet.

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Typical Application

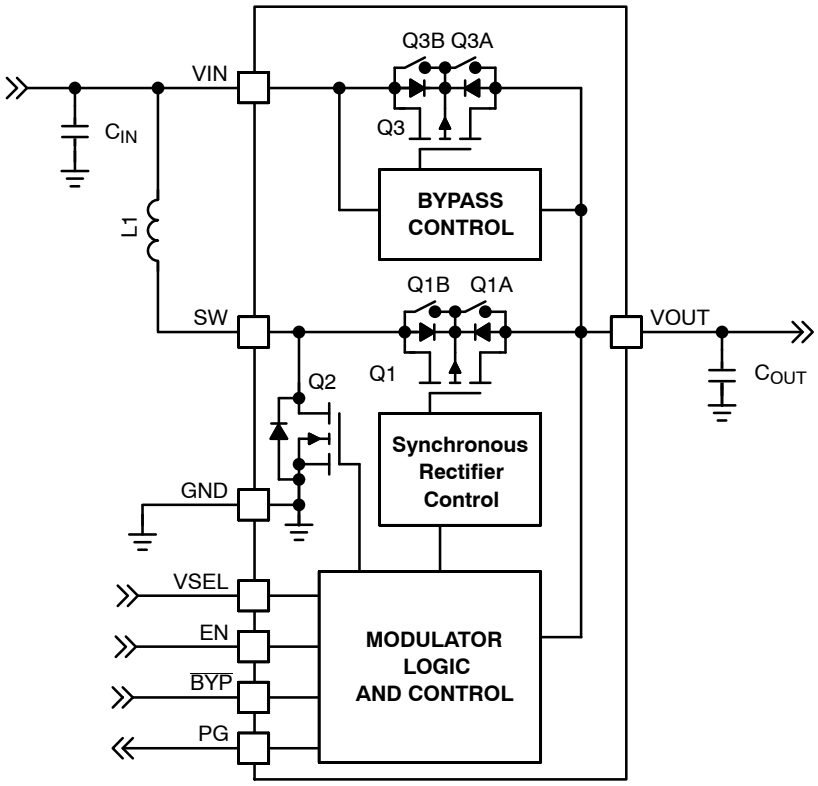


Figure 2. Block Diagram

Table 1. RECOMMENDED COMPONENTS

Component	Description	Vendor	Typical Value	Unit
L1	0.47 μH, 6.7 A (Isat), 23 mΩ (DCRmax), 2520	Murata: DFE252012F−R47M	0.47	μH
CIN	10 μF, 20%, 10 V, X5R, 0603	TDK: C1608X5R1A106M	10	μF
COUT	2 x 22 μF, 20%, 10 V, X5R, 0603	Taiyo Yuden: LMK107BBJ226MA−T	44	μF

Pin Configuration

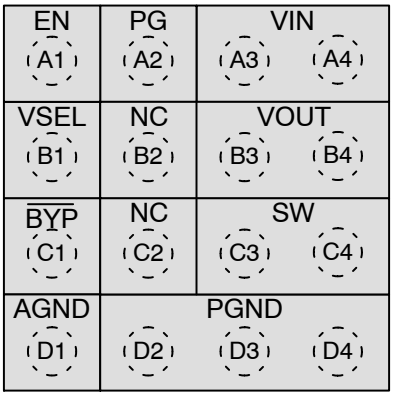


Figure 3. Top−Through View (Bumps Down)

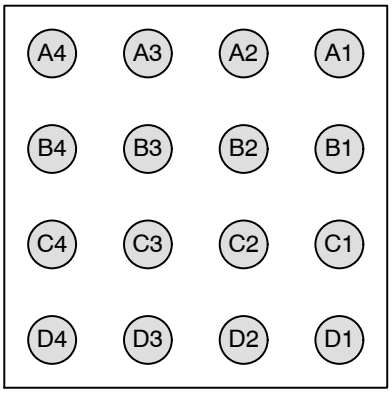


Figure 4. Bottom View (Bumps Up)

PIN DESCRIPTIONS

Pin #	Name	Description
A1	EN	*Enable*. When this pin is HIGH, the circuit is enabled.
A2	PG	*Power Good*. This is an open−drain output. PG is actively pulled LOW if output falls out of regulation due to overload or if thermal protection threshold is exceeded.
A3, A4	VIN	*Input Voltage*. Connect to Li−Ion battery input power source.
B1	VSEL	*Output Voltage Select*. When boost is running, this pin can be used to select the output voltage.
B3, B4	VOUT	*Output Voltage*. Place C_{OUT} as close as possible to the device.
C1	$\overline{BYP}$	*Bypass*. This pin can be used to activate Forced Bypass Mode. When this pin is LOW, the bypass switches (Q3 and Q1) are turned on and the IC is otherwise inactive.
C3, C4	SW	*Switching Node*. Connect to inductor.
D1	AGND	*Analog Ground*. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin. AGND should be connected to PGND at a single point.
D2−D4	PGND	*Power Ground*. This is the power return for the IC. The C_{OUT} bypass capacitor should be returned with the shortest path possible to these pins.
B2, C2	NC	No Internal Connection. Note: Bumps are present and should be tied to PGND or AGND.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{IN}	V_{IN} Input Voltage		−0.3	6.5	V
V_{OUT}	V_{OUT} Output Voltage		−0.3	6.0	V
V_{SW}	SW Node Voltage	DC	−0.3	6.0	V
		Transient: 10 ns, 3 MHz	−1.0	8.0	
	Other Pins		−0.3	6.5 (Note 1)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	2.0		kV
		Charged Device Model, JESD22−C101	1.5		
T_J	Junction Temperature		−40	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds		−	+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 6.5 V or V_{IN} + 0.3 V.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{IN}	Supply Voltage	2.5	5.5 (Note 2)	V
I_{OUT}	Output Current	0	2500	mA
T_A	Ambient Temperature	−40	+85	°C
T_J	Junction Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. When V_{IN} nears V_{OUT} the part will go into Automatic Bypass, depending on load current.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance	60	°C/W

NOTE: Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four−layer **onsemi** evaluation boards (1 oz copper on all layers). Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

ELECTRICAL CHARACTERISTICS (Note 3)

Unless otherwise noted and per Figure 1 minimum and maximum values are from V_{IN} = 2.5 V to 4.5 V and T_A = −40°C to +85°C. Typical values are at V_{IN} = 3.0 V and T_A = 25°C for all output voltage options.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_Q	V_{IN} Quiescent Current	Automatic Bypass Mode, V_{OUT_TARGET} = 3.3 V, V_{IN} = 3.6 V	–	140	190	μA
		Boost Mode, V_{OUT} = 3.3 V, V_{IN} = 3.0 V	–	135	180	
		Shutdown, EN = 0 V, V_{IN} = 3.0 V	–	4.0	12.0	
		Forced Bypass Mode, V_{IN} = 3.6 V	–	6.0	12.0	
I_{LK}	V_{OUT} to V_{IN} Reverse Leakage	V_{OUT} = 5.0 V, EN = 0 V, V_{IN} = 0 V	–	0.5	1.0	μA
I_{LK_OUT}	V_{IN} to V_{OUT} Leakage Current	V_{OUT} = 0 V, EN = 0 V, V_{IN} = 4.2 V	–	0.1	1.5	μA
V_{UVLO}	Under−Voltage Lockout	V_{IN} Rising	–	2.20	2.35	V
V_{UVLO_HYS}	Under−Voltage Lockout Hysteresis		–	200	–	mV
V_{IH}	Logic Level High EN, VSEL, $\overline{BYP}$		1.05	–	–	V
V_{IL}	Logic Level Low EN, VSEL, $\overline{BYP}$		–	–	0.4	V
R_{LOW}	Logic Control Pin Pull Downs (LOW Active)	$\overline{BYP}$, VSEL, EN	–	300	–	kΩ
I_{PD}	Weak Current Source Pull−Down	$\overline{BYP}$, VSEL, EN	–	100	–	nA
V_{REG}	Output Voltage Accuracy	2.5 V ≤ V_{IN} ≤ V_{OUT_TARGET} −100 mV, DC, 0 to 2500 mA	−1.0	–	4.0	%
		2.5 V ≤ V_{IN} ≤ V_{OUT_TARGET} −100 mV, DC, PWM (CCM) Operation	−1.0	–	2.5	
I_{V_LIM}	Boost Valley Current Limit	V_{IN} = 2.5 V, V_{OUT} = 3.3 V	4.7	5.3	–	A
$I_{V\_LIM\_SS}$	Boost Valley Current Limit During Soft Start	V_{IN} = 2.5 V, V_{OUT} = 3.3 V	–	2.6	–	A
t_{SS}	Soft−Start EN HIGH to Regulation	50 Ω Load, V_{OUT_TARGET} = 3.3 V (Time from EN Rising Edge to 90% of V_{OUT_TARGET})	–	300	–	μs
t_{RST}	FAULT Restart Timer		–	20	–	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Minimum and Maximum limits are verified by design, test, or statistical analysis. Typical (Typ.) numbers are not verified, but represent typical results.

TYPICAL CHARACTERISTICS

Unless otherwise specified, T_A = 25°C; circuit and components according to Figure 1.

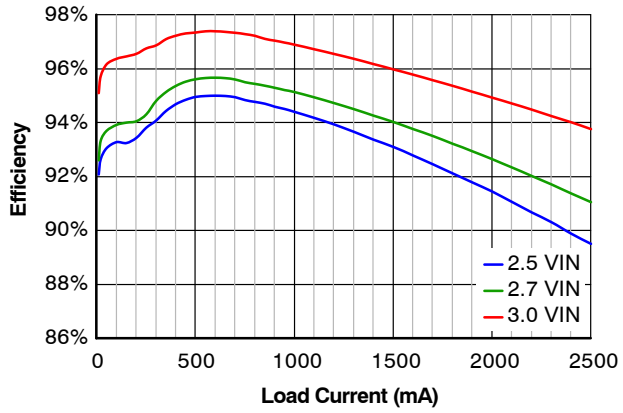


Figure 5. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 3.15 V

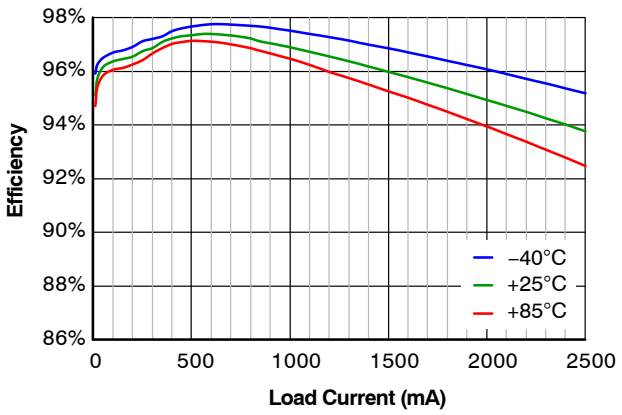


Figure 6. Efficiency vs. Load Current and Temperature, V_{IN} = 3.0 V, V_{OUT} = 3.15 V

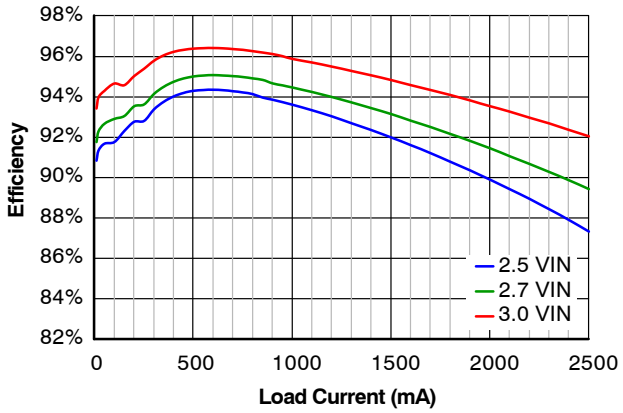


Figure 7. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 3.3 V

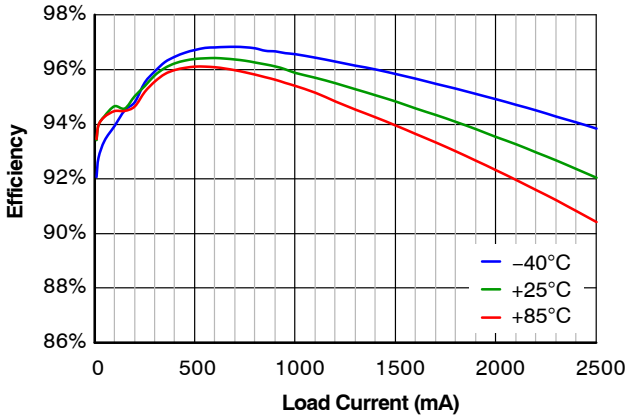


Figure 8. Efficiency vs. Load Current and Temperature, V_{IN} = 3.0 V, V_{OUT} = 3.3 V

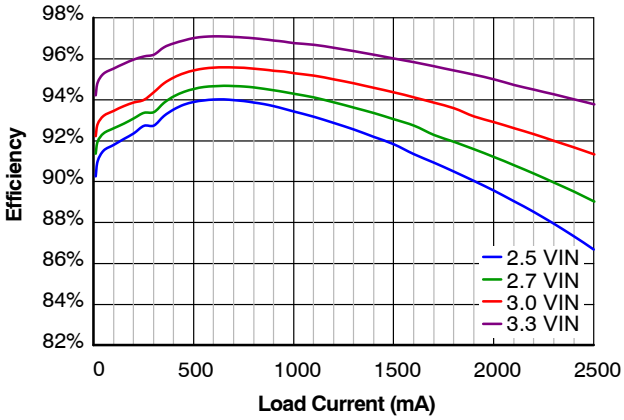


Figure 9. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 3.5 V

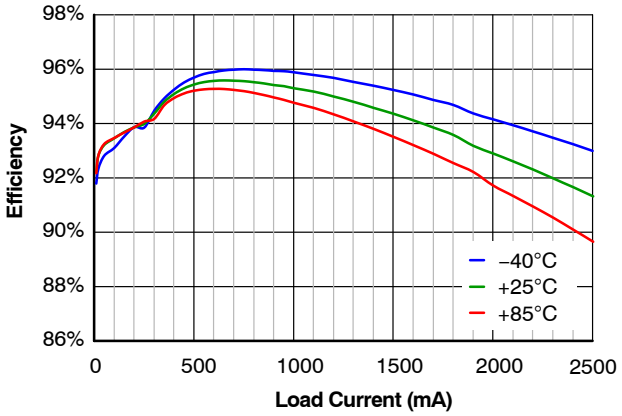


Figure 10. Efficiency vs. Load Current and Temperature, V_{IN} = 3.0 V, V_{OUT} = 3.5 V

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C; circuit and components according to Figure 1.

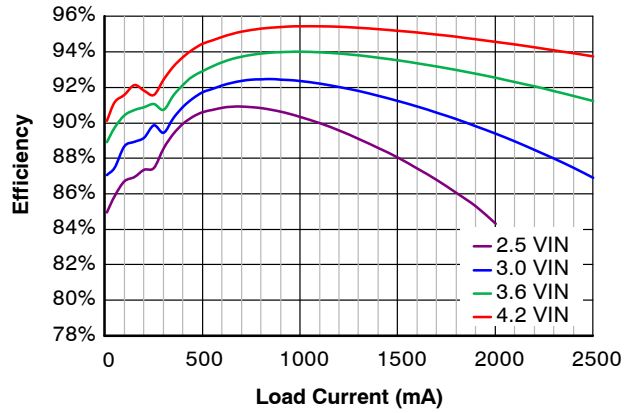


Figure 11. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 5.0 V

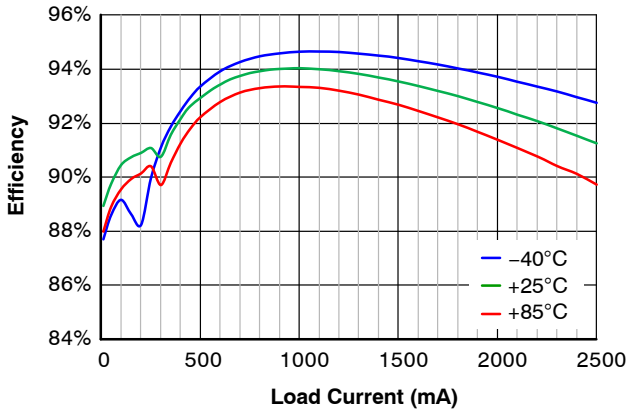


Figure 12. Efficiency vs. Load Current and Temperature, V_{IN} = 3.6 V, V_{OUT} = 5.0 V

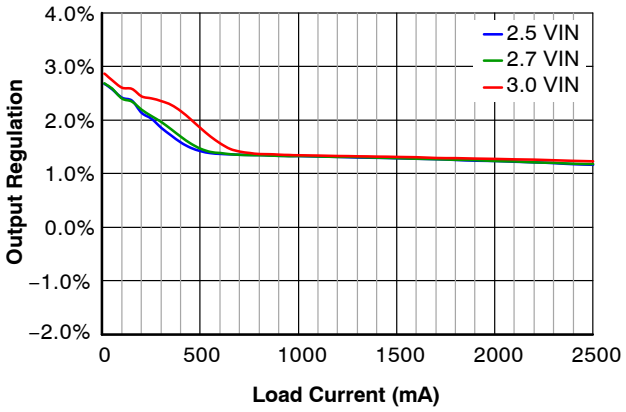


Figure 13. Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 3.15 V

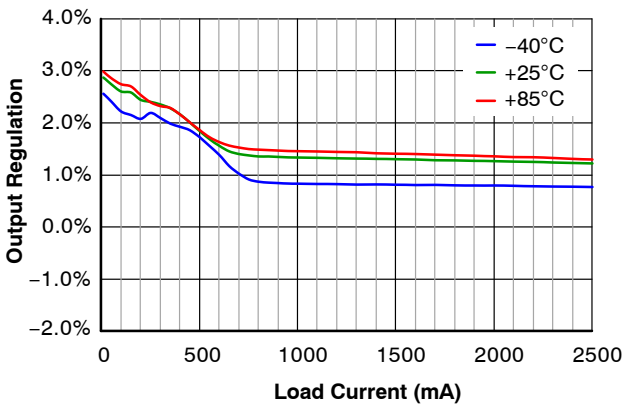


Figure 14. Output Regulation vs. Load Current and Temperature, V_{IN} = 3.0 V, V_{OUT} = 3.15 V

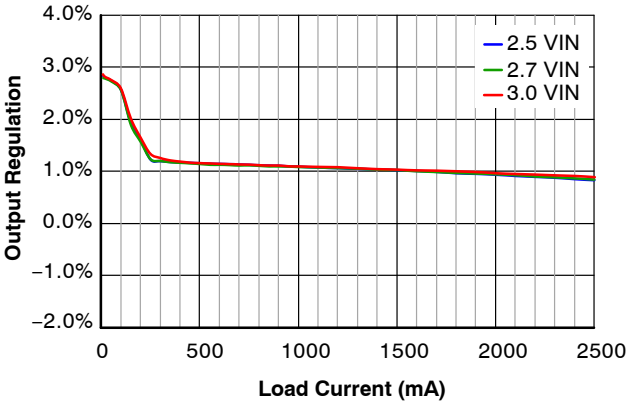


Figure 15. Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 3.3 V

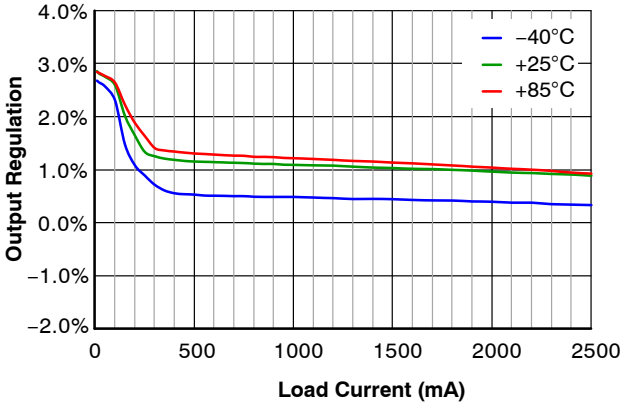


Figure 16. Output Regulation vs. Load Current and Temperature, V_{IN} = 3.0 V, V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C; circuit and components according to Figure 1.

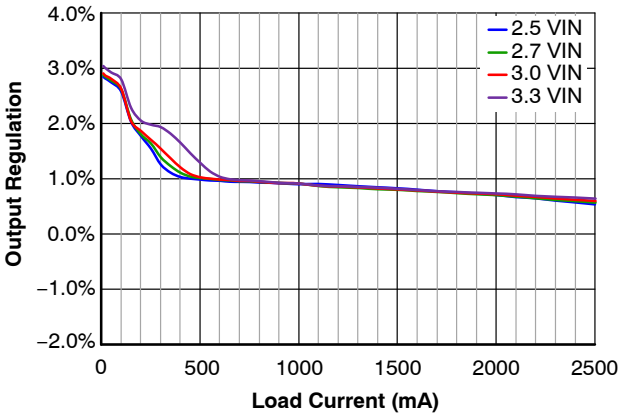


Figure 17. Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 3.5 V

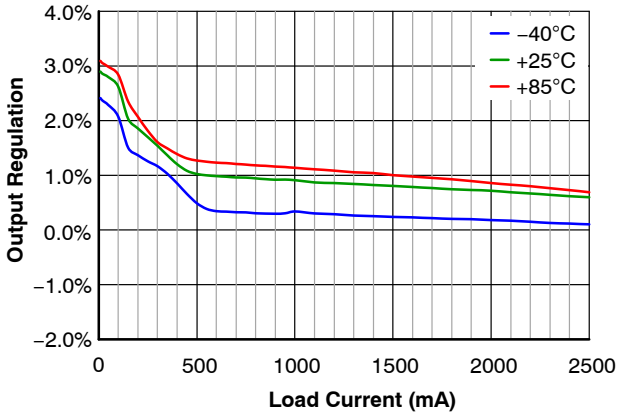


Figure 18. Output Regulation vs. Load Current and Temperature, V_{IN} = 3.0 V, V_{OUT} = 3.5 V

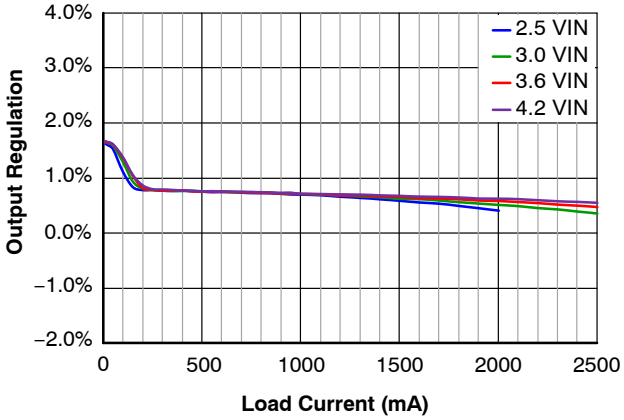


Figure 19. Output Regulation vs. Load Current and Input Voltage, V_{OUT} = 5.0 V

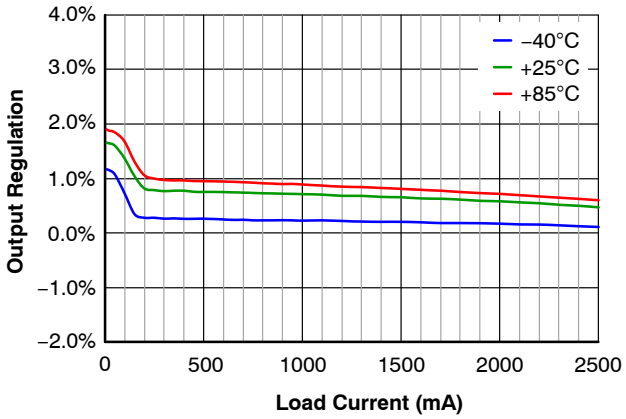


Figure 20. Output Regulation vs. Load Current and Temperature, V_{IN} = 3.6 V, V_{OUT} = 5.0 V

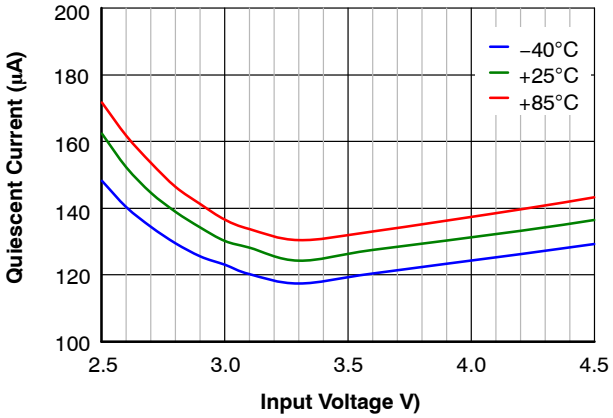


Figure 21. Quiescent Current vs. Input Voltage and Temperature, V_{OUT} = 3.15 V, Auto Bypass

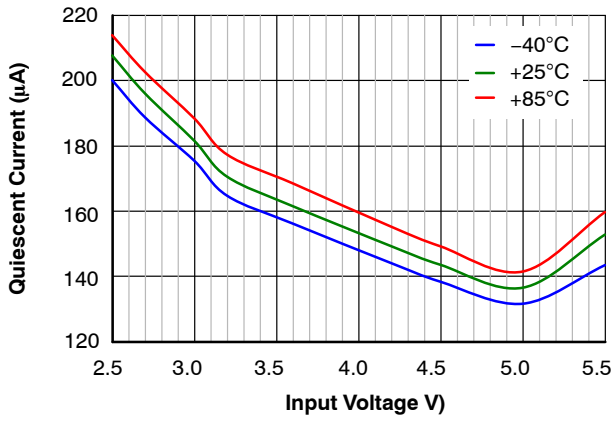


Figure 22. Quiescent Current vs. Input Voltage and Temperature, V_{OUT} = 5.0 V, Auto Bypass

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C; circuit and components according to Figure 1.

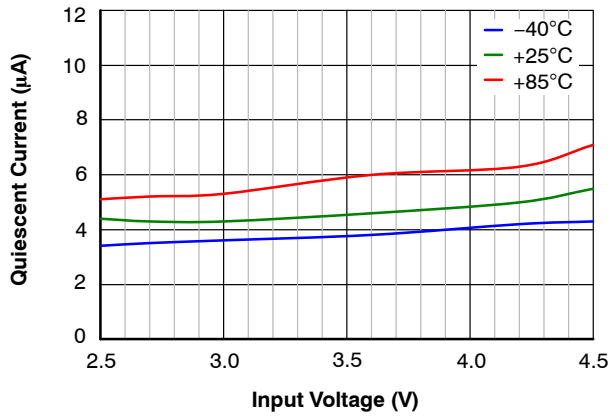


Figure 23. Quiescent Current vs. Input Voltage and Temperature, V_{OUT} = 3.3 V, Forced Bypass

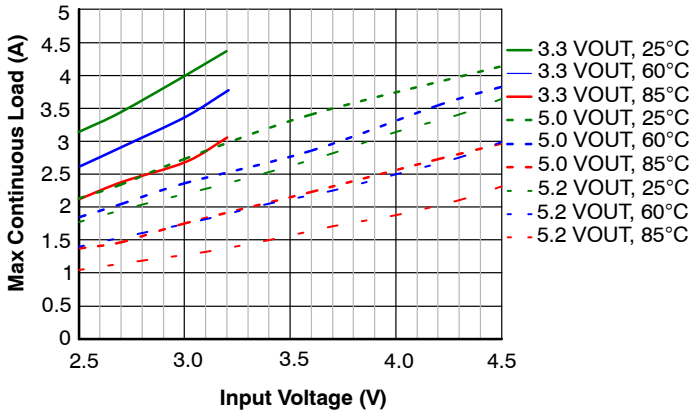


Figure 24. Typical Maximum Continuous Load vs. Input Voltage, Temperature and Output Voltage

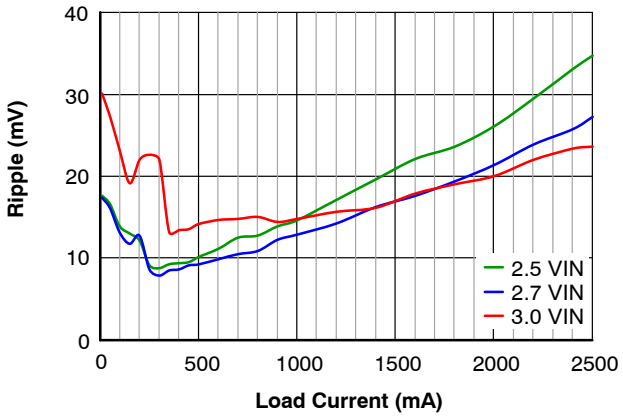


Figure 25. Output Ripple vs. Load Current and Input Voltage, V_{OUT} = 3.15 V

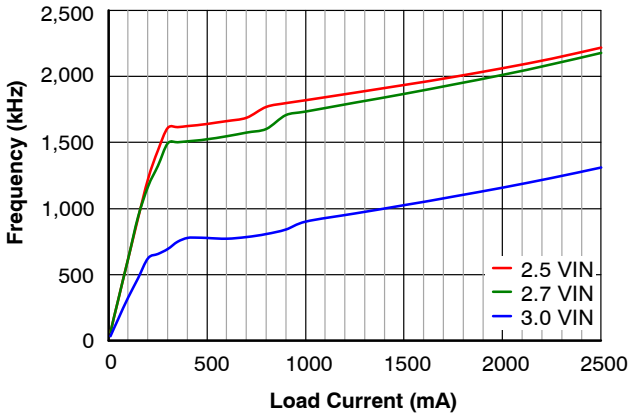


Figure 26. Frequency vs. Load Current and Input Voltage, V_{OUT} = 3.15 V

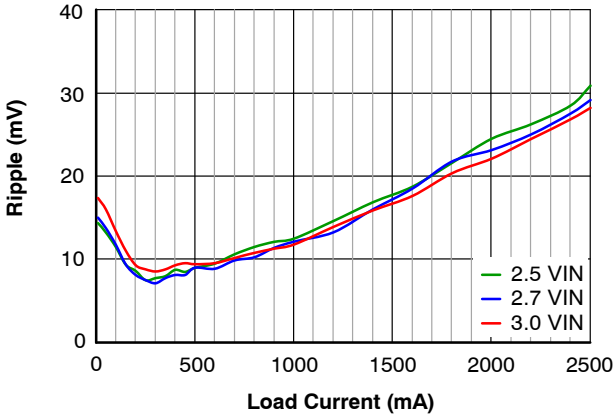


Figure 27. Output Ripple vs. Load Current and Input Voltage, V_{OUT} = 3.3 V

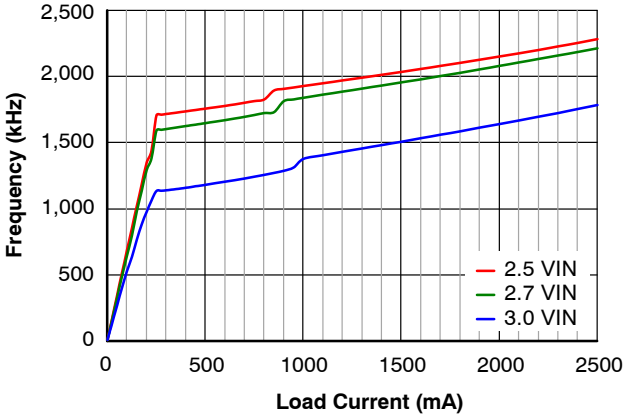


Figure 28. Frequency vs. Load Current and Input Voltage, V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C; circuit and components according to Figure 1.

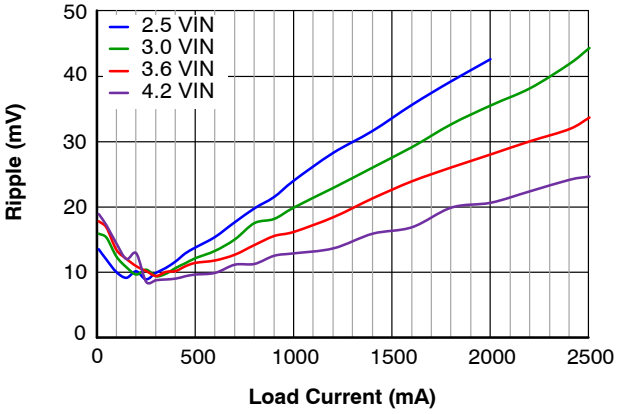


Figure 29. Output Ripple vs. Load Current and Input Voltage, V_{OUT} = 5.0 V

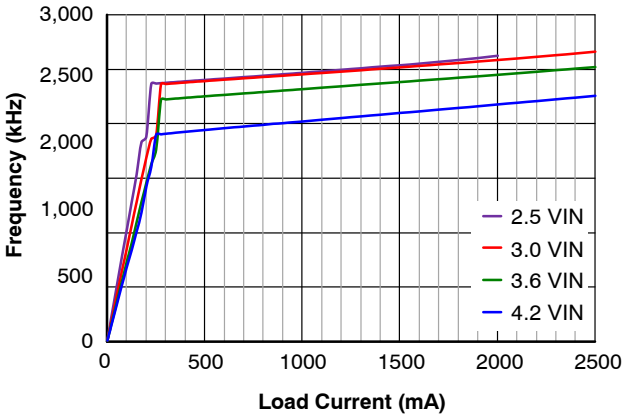


Figure 30. Frequency vs. Load Current and Input Voltage, V_{OUT} = 5.0 V

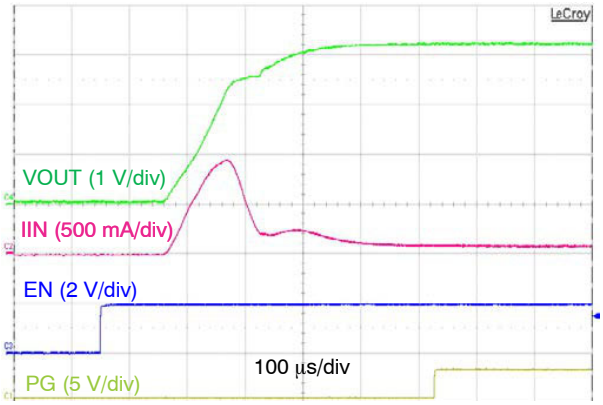


Figure 31. Startup, 50 Ω Load, V_{IN} = 2.5 V, V_{OUT} = 3.15 V

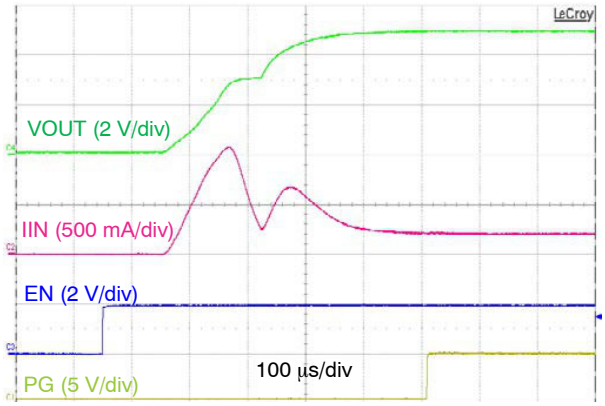


Figure 32. Startup, 50 Ω Load, V_{IN} = 3.0 V, V_{OUT} = 5.0 V

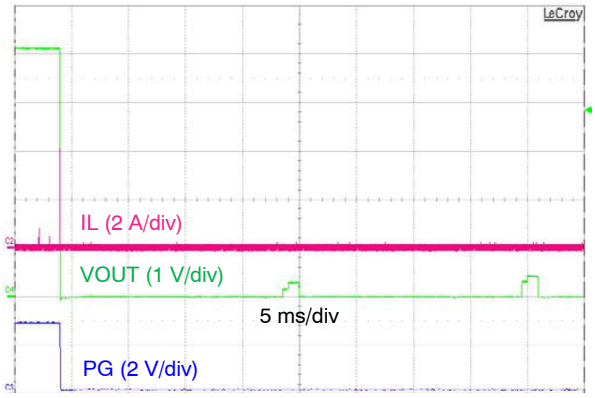


Figure 33. Overload Protection, V_{IN} = 3.0 V, V_{OUT} = 5.0 V

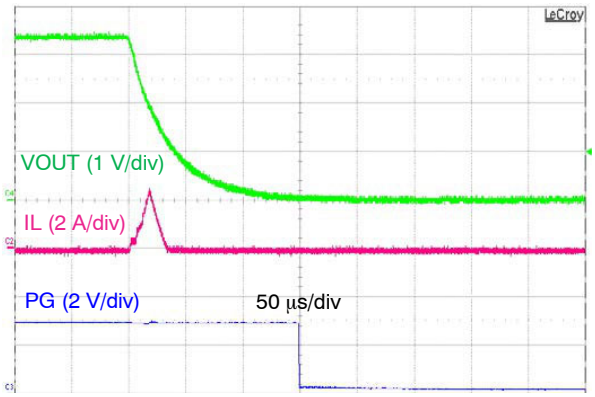


Figure 34. Output Fault, V_{IN} = 3.0 V, V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_A = 25°C; circuit and components according to Figure 1.

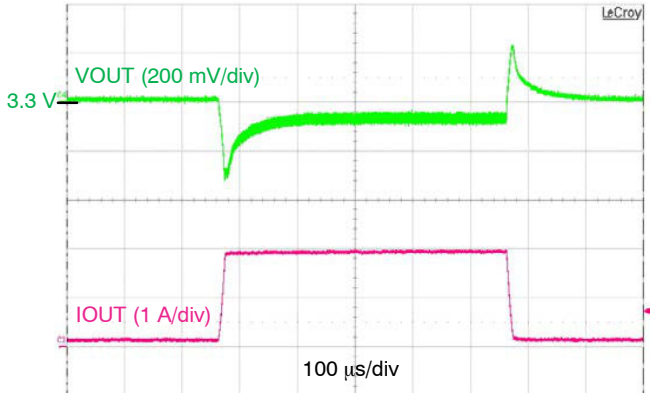


Figure 35. Load Transient, 150–2000 mA, 10 µs Edge, V_{IN} = 3.0 V, V_{OUT} = 3.3 V

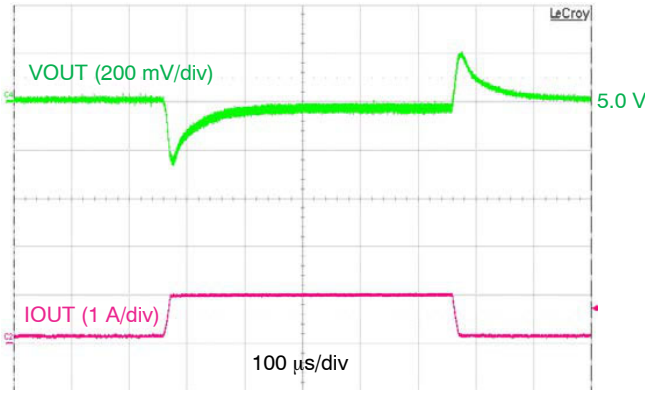


Figure 36. Load Transient, 150–1000 mA, 10 µs Edge, V_{IN} = 3.6 V, V_{OUT} = 5.0 V

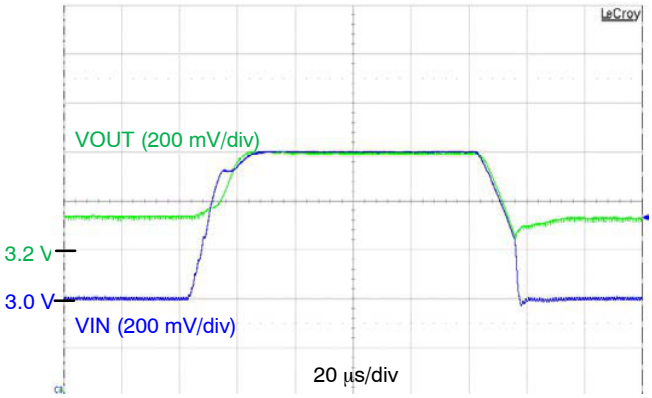


Figure 37. Line Transient, 3.0–3.6 V_{IN}, 10 µs Edge, 500 mA Load, V_{OUT} = 3.3 V

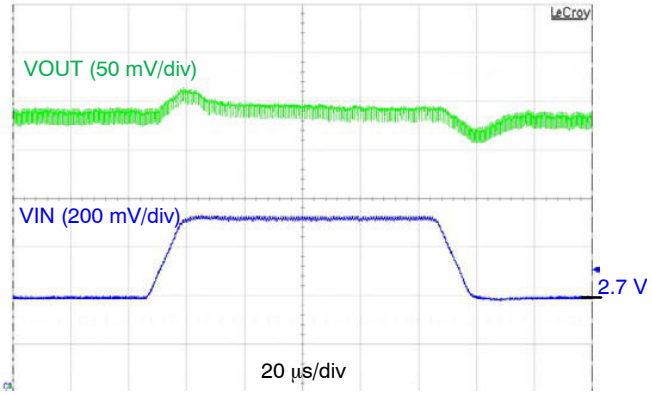


Figure 38. Line Transient, 2.7–3.0 V_{IN}, 10 µs Edge, 500 mA Load, V_{OUT} = 3.3 V

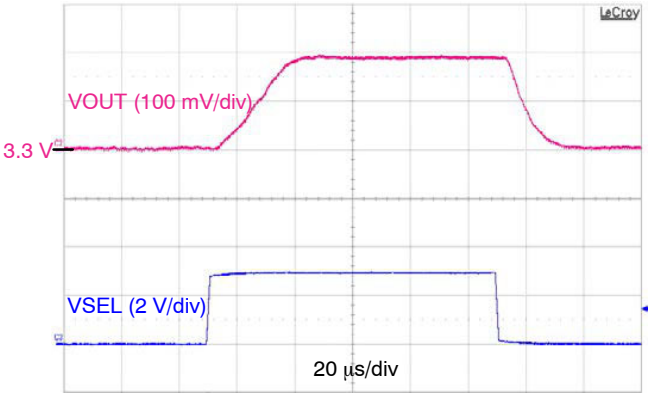


Figure 39. V_{SEL} Step, V_{IN} = 3 V, V_{OUT} = 3.3 V, 500 mA Load

CIRCUIT DESCRIPTION

FAN48623 is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low V_{IN} voltages. At light load, the regulator operates at Discontinuous Conduction Mode (DCM) to maintain high efficiency.

FAN48623 uses a current−mode modulator to achieve excellent transient response and smooth transitions between CCM and DCM operation.

The regulator includes a Bypass Mode that automatically activates when V_{IN} is above the boost regulator's set point.

Table 2. OPERATING STATES

Mode	Description	Invoked When
LIN	Linear Startup	$V_{IN} > V_{OUT}$
SS	Soft−Start Mode	$V_{IN} < V_{OUT} < V_{OUT\_TARGET}$
BST	Boost Operating Mode	$V_{OUT} = V_{OUT\_TARGET}$
BPS	Bypass Mode	$V_{IN} > V_{OUT\_TARGET}$

Startup and Shutdown (EN Pin)

If EN is LOW, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, current flow is prevented from VIN to VOUT, as well as reverse flow from VOUT to VIN. During startup, keep DC current draw below 500 mA until the device successfully executes startup. It is recommended not to connect EN directly to VIN but use a GPIO voltage of 1.8 V to set the logic for the EN pin. The following table describes the startup sequence.

Table 3. BOOST STARTUP SEQUENCE

Start Mode	Entry	Exit	End Mode	Time-out (μs)
LIN1	$V_{IN} > V_{UVLO}$, EN = 1	$V_{OUT} > V_{IN} - 300$ mV	SS	
		TIMEOUT	LIN2	512
LIN2	LIN1 Exit	$V_{OUT} > V_{IN} - 300$ mV	SS	
		TIMEOUT	FAULT	1024
SS	LIN1 or LIN2 Exit	$V_{OUT} = V_{OUT\_TARGET}$	BST	

Linear Startup (LIN)

When EN is HIGH and $V_{IN} > V_{UVLO}$, the regulator attempts to bring V_{OUT} within 300 mV of V_{IN} using the internal fixed current source from V_{IN} (Q3). The current is limited to the LIN1 (~1 A) set point.

If V_{OUT} reaches V_{IN}−300 mV during LIN1 Mode, SS Mode is initiated. Otherwise, LIN1 times out after 512 μs and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented to approximately 2 A. If V_{OUT} fails to reach V_{IN}−300 mV after 1024 μs, a fault state is declared.

Soft−Start Mode (SS)

Upon successful completion of the LIN Mode ($V_{OUT} \geq V_{IN} - 300$ mV), SS Mode begins and the regulator starts switching with boost valley current limited to 50% of nominal level at Boost Mode.

During SS Mode, V_{OUT} is ramped up by stepping the internal reference. If V_{OUT} fails to reach the voltage required during the SS ramp sequence within 64 μs, a fault state is declare

Boost Mode (BST)

This is a normal operating state of the regulator.

Bypass Mode (BPS)

If V_{IN} is above V_{OUT_TARGET} when the SS Mode successfully completes, the device transitions directly to BPS Mode.

Table 4. EN AND $\overline{BYP}$ LOGIC TABLE

EN	$\overline{BYP}$	Mode	V_{OUT}
0	0	Shutdown	0
	1	Shutdown	0
1	0	Forced Bypass	V_{IN}
	1	Auto Bypass	V_{OUT_TARGET} or V_{IN} (if $V_{IN} > V_{OUT\_TARGET}$)

FAULT State

The regulator enters the FAULT state under any of the following conditions:

- V_{OUT} fails to achieve the voltage required to advance from LIN state to SS state.
- V_{OUT} fails to achieve the voltage required to advance from SS state to BST state.
- Boost valley current limit triggers for 2 ms during the BST state.
- V_{IN} to V_{OUT} voltage drop exceeds 160 mV during BPS state.
- $V_{IN} < V_{UVLO}$

If a fault is triggered, the regulator stops switching and presents a high−impedance path between VIN and VOUT. After waiting 20 ms, an automatic restart is attempted.

Power Good

Power good is defined as a 0−FAULT, 1−POWER GOOD, open−drain output. The Power Good pin (PG) signals when the regulator has successfully completed soft−start with no faults occurring. Power Good also functions as a warning flag for high die temperature.

- PG is released HIGH when the soft−start sequence is successfully completed.
- Any FAULT state causes PG to be de−asserted.

- PG is not asserted during Forced Bypass exit to Boost Mode until the soft−start sequence is successfully completed.

Over−Temperature

When the die temperature exceeds 125°C, PG de−asserts and the output remains regulated. PG is re−asserted when the device cools by approximately 20°C.

The regulator shuts down if the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

Automatic Bypass

In normal operation, the device automatically transitions from Boost Mode to Bypass Mode if V_{IN} goes above V_{OUT_TARGET}. In Bypass Mode, the device fully enhances both Q1 and Q3 to provide a very low impedance path from VIN to VOUT. Entry into the Bypass Mode is triggered when $V_{IN} > V_{OUT\_TARGET}$ and no switching has occurred during the past 10 μs. To soften the entry into Bypass Mode, Q3 is driven as a linear current source for the first 5 μs. Bypass Mode exit is triggered when VOUT reaches V_{OUT_TARGET}. During Automatic Bypass Mode, the device is short−circuit protected by voltage comparator tracking the voltage drop from V_{IN} to V_{OUT}; if the drop exceeds 160 mV, a fault state is declared.

With sufficient load to enforce CCM operation, the Bypass Mode to Boost Mode transition occurs at the target V_{OUT}. The Bypass Mode exit threshold has a 50 mV hysteresis imposed at V_{OUT} to prevent cycling between modes. The corresponding input voltage at the transition point is:

$$V_{IN} \le V_{OUT} + I_{LOAD} \cdot \left(DCR_L + R_{DS(ON)P}\right) \parallel R_{DS(ON)BYP} - 50\ mV \quad \text{(eq. 1)}$$

The Bypass Mode entry threshold has a 30 mV hysteresis imposed at V_{OUT} to prevent cycling between modes. The transition from Boost Mode to Bypass Mode occurs at the target V_{OUT} + 30 mV. The corresponding input voltage is:

$$V_{IN} \le V_{OUT} + I_{LOAD} \cdot \left(DCR_L + R_{DS(ON)P}\right) + 30\ mV \quad \text{(eq. 2)}$$

Forced Bypass

Forced Bypass Mode is activated by pulling $\overline{BYP}$ pin LOW. Forced Bypass Mode initiates with a current limit on Q3 and then proceeds to the Bypass Mode with both Q1 and Q3 fully enhanced. To prevent reverse current to the battery, the device waits until output discharges below V_{IN} before entering Forced Bypass Mode.

After the transition is complete, most of the internal circuitry is disabled to minimize quiescent current. OCP, UVLO and OTP are inactive in Forced Bypass Mode.

By pulling $\overline{BYP}$ pin HIGH, the part transitions from Forced Bypass Mode to Boost Mode. During the transition, Q1 is off and Q3 is driven as a linear current source for the first 5 μs before entering Boost Mode.

APPLICATION INFORMATION

Output Capacitance (C_{OUT})

Stability

The effective capacitance (CEFF – Note 4) of small, high−value, ceramic capacitors decrease as bias voltage increases, as illustrated in Figure 40.

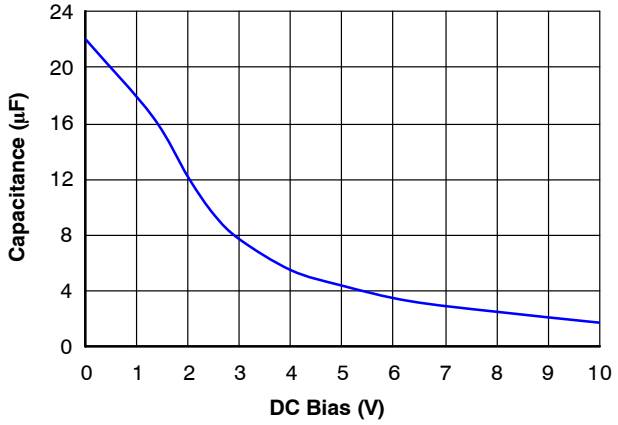


Figure 40. C_{EFF} for 22 μF, 0603, X5R, 10 V−Rated Capacitor (TDK C1608X5R1A226M080AC)

Stable operation is guaranteed with the minimum value of C_{EFF} ($C_{EFF(MIN)}$), as outlined in Table 5.

Table 5. MINIMUM C_{EFF} REQUIRED FOR STABILITY

Operating Conditions		
V_{OUT} (V)	I_{LOAD} (mA)	$C_{EFF(MIN)}$ (μF)
3.15	0 to 2500	9
5.0	0 to 2500	6

4. C_{EFF} varies with manufacturer, material, and case size.

Inductor Selection

Recommended nominal inductance value is 0.47 μH.

The FAN48623 employs valley−current limiting. Peak inductor current can reach 6.5 A for a short duration during overload conditions. Saturation effects cause the inductor current ripple to become higher under high loading as only the valley of the inductor current ripple is controlled.

Startup Inrush Current Limit

Input current limiting is in effect during soft−start, which limits the current available to charge C_{OUT} and any additional capacitance on the V_{OUT} line. If the output fails to achieve regulation within the set limit, a FAULT occurs, causing the circuit to shut down then restart after 20 ms. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high−current load and high capacitance are both present during soft−start, the circuit may fail to achieve regulation and continually attempts soft−start, only to have the output capacitance discharged by the load when in a FAULT state.

Output Voltage Ripple

Output voltage ripple is inversely proportional to C_{OUT}. During t_{ON}, when the boost switch is on, all load current is supplied by C_{OUT}. Output ripple is calculated as:

$$V_{RIPPLE(P-P)} = t_{ON} \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 3)}$$

and

$$t_{ON} = t_{SW} \cdot D = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{(eq. 4)}$$

therefore:

$$V_{RIPPLE(P-P)} = t_{SW} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \cdot \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 5)}$$

and

$$t_{SW} = \frac{1}{f_{SW}} \quad \text{(eq. 6)}$$

As can be seen from Equation 5, the maximum V_{RIPPLE} occurs when V_{IN} is at minimum and I_{LOAD} is at maximum.

Voltage at VOUT

For applications where a foreign voltage source could be applied at VOUT, care should be taken to ensure V_{OUT} never exceeds the Absolute Maximum Rating.

LAYOUT RECOMMENDATIONS

The layout recommendations below highlight various layers using different colors.

To minimize spikes at V_{OUT}, C_{OUT} must be placed as close as possible to PGND and VOUT, as shown in Figure 41.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

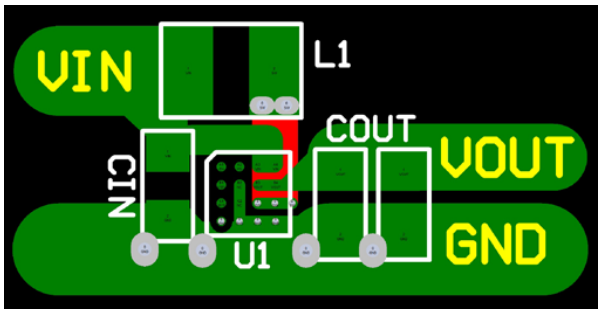


Figure 41. Layout Recommendation

Refer to the section below for detailed layout recommendations for each layer.

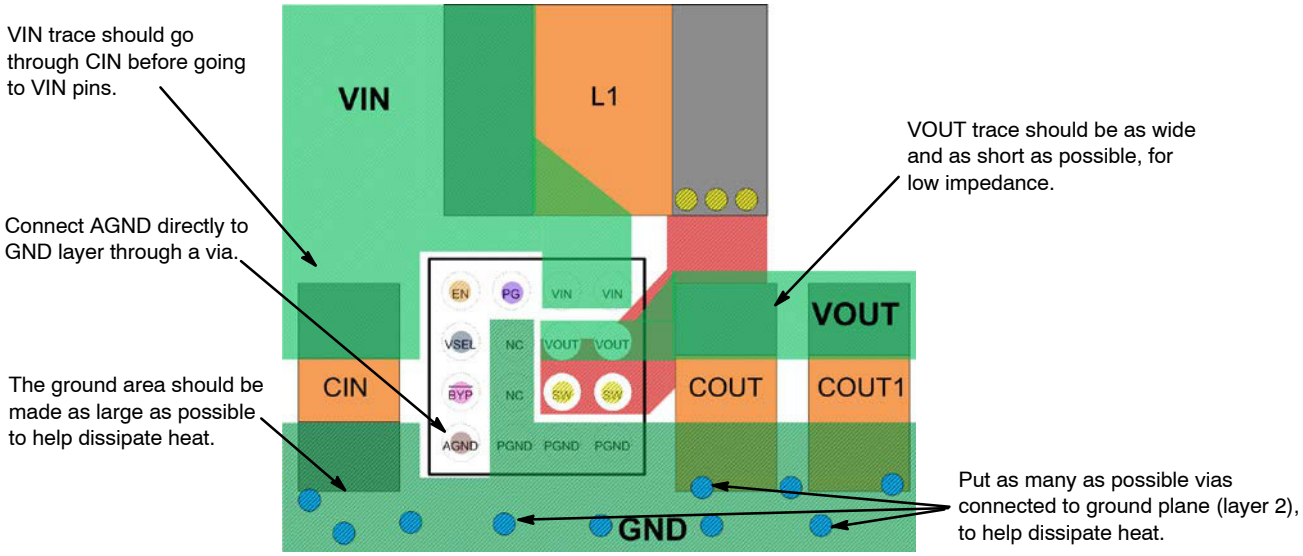
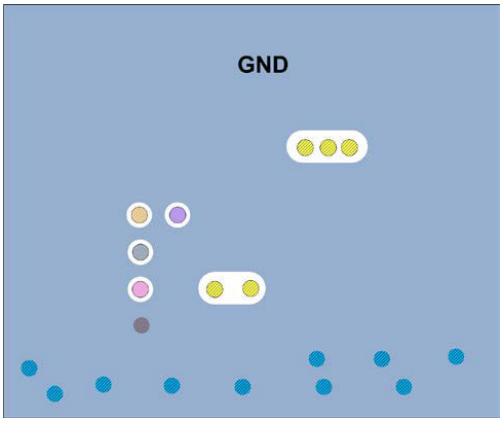


Figure 42. Top Layer



- Layer 2 should be a solid ground layer, to shield VOUT from capacitive coupling of the fast edges of SW node.
- Logic signals can be routed on this layer.

Figure 43. Layer 2

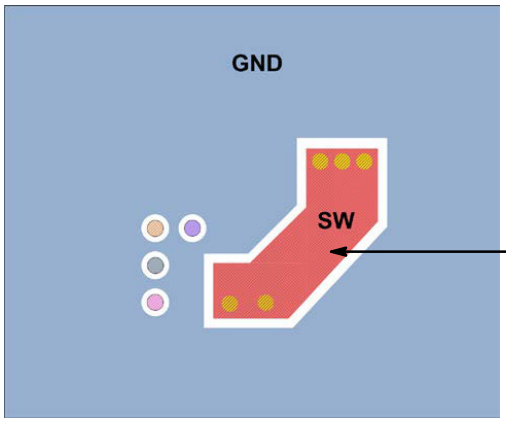


Figure 44. Layer 3

ORDERING INFORMATION

Part Number	Output Voltage V_{SEL0}/V_{SEL1} (Note 5)	Operating Temperature	Package	Shipping†	Device Marking
FAN48623UC315X	3.150 / 3.330	−40°C to 85°C	16−Ball, 4x4 Array, 0.4 mm Pitch, 250 mm Ball, Wafer−Level Chip−Scale Package (WLCSP)	3000 / Tape & Reel	JK
FAN48623UC32JX	3.20 / 3.413				JD
FAN48623UC33X	3.300 / 3.489				JE
FAN48623UC35X	3.5 / 3.7				JF
FAN48623UC36FX	3.64 / 3.709				JG
FAN48623UC50X	5.000 / 5.286				JL
FAN48623UC50GX	5.000 / 5.190				JM

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. Other output voltages are available on request. Please contact a **onsemi** representative.

PRODUCT−SPECIFIC DIMENSIONS

Product	D	E	X	Y
FAN48623UC315X	1.810 ±0.030	1.810 ±0.030	0.305	0.305
FAN48623UC32JX	1.810 ±0.030	1.810 ±0.030	0.305	0.305
FAN48623UC33X	1.810 ±0.030	1.810 ±0.030	0.305	0.305
FAN48623UC35X	1.810 ±0.030	1.810 ±0.030	0.305	0.305
FAN48623UC36FX	1.810 ±0.030	1.810 ±0.030	0.305	0.305
FAN48623UC50X	1.810 ±0.030	1.810 ±0.030	0.305	0.305
FAN48623UC50GX	1.810 ±0.030	1.810 ±0.030	0.305	0.305

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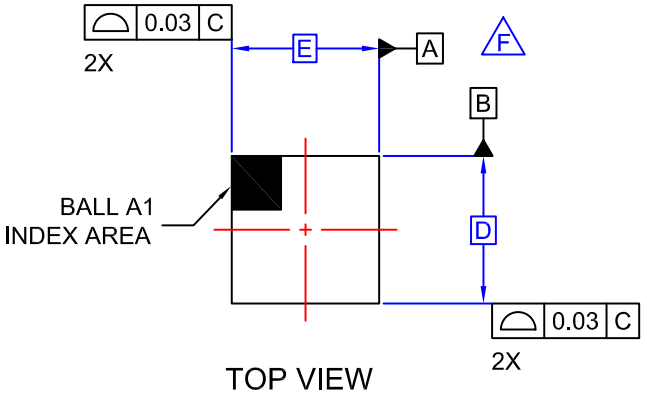
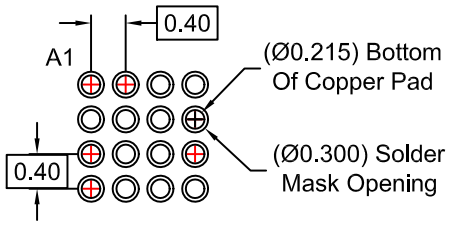
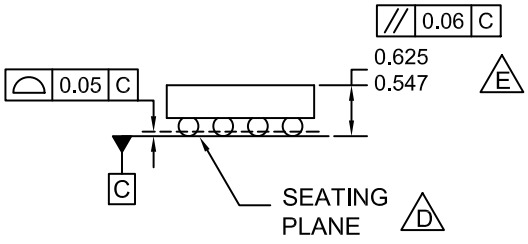
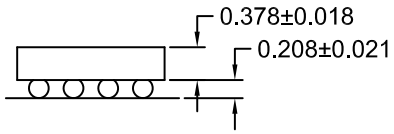


TOP VIEW

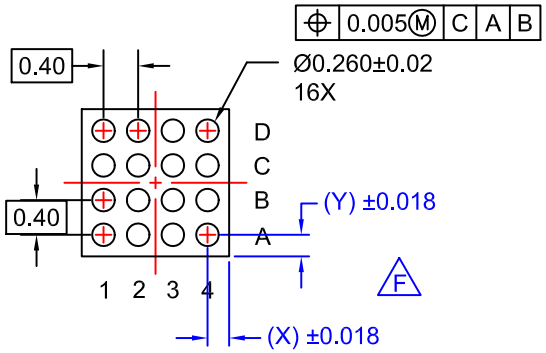


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

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