EVBUM2282/D

KLI-2113/KLI-8023 Image Sensors Evaluation Kit User's Manual

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EVAL BOARD USER'S MANUAL

Purpose, Scope

The purpose of the KLI−2113/KLI−8023 Evaluation Board is to allow ON Semiconductor customers to quickly and easily operate and evaluate the performance of these image sensors.

The Evaluation Board provides a complete Tri-linear CCD imaging acquisition sub-system for the following devices:

- KLI−2113 Image Sensor
- KLI−8023 Image Sensor

OVERVIEW

The Evaluation Board set consists of two circuit boards, a Timing Generator Board and a CCD specific Sensor (Imager) Board (Note: The KLI−2113 requires the 3E8207 imager board and the KLI−8023 requires the 3E8206 imager board.)

The Timing Generator Board generates the digital clock signals necessary to operate the CCD, the digital signals needed to operate the three A/D converters, and the Frame Grabber and External sync signals. The positive and negative DC power supply inputs are regulated on the Timing Generator Board. The outputs of the voltage regulators are routed from the Timing Generator Board to the CCD Sensor Board.

Inputs to the CCD Sensor Board include the TTL timing signals from the Timing Generator Board and the regulated positive and negative DC power supplies. Clock drivers on the CCD Sensor Board generate the clock voltages necessary to operate the KLI series CCD. The CCD Sensor Board also generates the necessary CCD bias voltages from the positive regulated power supply input.

For digital output operation, each of the three CCD VOUT signals are buffered by emitter follower circuits and then routed back to the Timing Generator Board to be processed by an Analog Front End (AFE) integrated circuit. The AFE chip contains a correlated double sampling (CDS) circuit, an 8 bit programmable DC offset compensation circuit, an 8 bit programmable gain amplifier, and a 12 bit A/D converter.

For analog output operation, each of the three CCD VOUT signals are A/C coupled to remove the large DC component of the waveform and then routed to a non-inverting operational amplifier configured with a gain of two. The output of the amplifier is then driven off the Sensor board via a 50 Ω coaxial cable.

SPECIFICATIONS

Digital Output Data Rate:	Maximum 6 MHz
Analog Output Data Rate:	CCD Dependent (Maximum 10 MHz)
Resolution:	12 Bits per Channel Digital
Line Rate:	Depends on Data rate, Integration time and CCD

Outputs

R [11..0]:	Red Output Channel, Differential TTL
G [11..0]:	Green Output Channel, Differential TTL
B [11..0]:	Blue Output Channel, Differential TTL
Frame Grabber Syncs:	Differential TTL
External Syncs:	Differential TTL

Inputs

TTL

Serial Clock:	10 MHz Maximum
PGA Gain Range:	1X to 6X
PGA Gain Resolution:	256 Steps
Offset Range:	−100 mV to +100 mV
Offset Resolution:	256 Steps
Temperature Range Board:	0 − 70°C
Temperature Range CCD:	−50 to +70°C

Power Supplies

Table 1. POWER SUPPLIES REQUIREMENTS

Voltage				Current	
Supply	**Minimum**	**Nominal**	**Maximum**	**Typical**	**Maximum**
+5 V	+4.9 V	+5 V	+5.1 V	1000 mA	2000 mA
+20 V	+17 V	+18 V	+20 V	500 mA	1000 mA
−20 V	−20 V	−18 V	−17 V	100 mA	250 mA

BLOCK DIAGRAMS

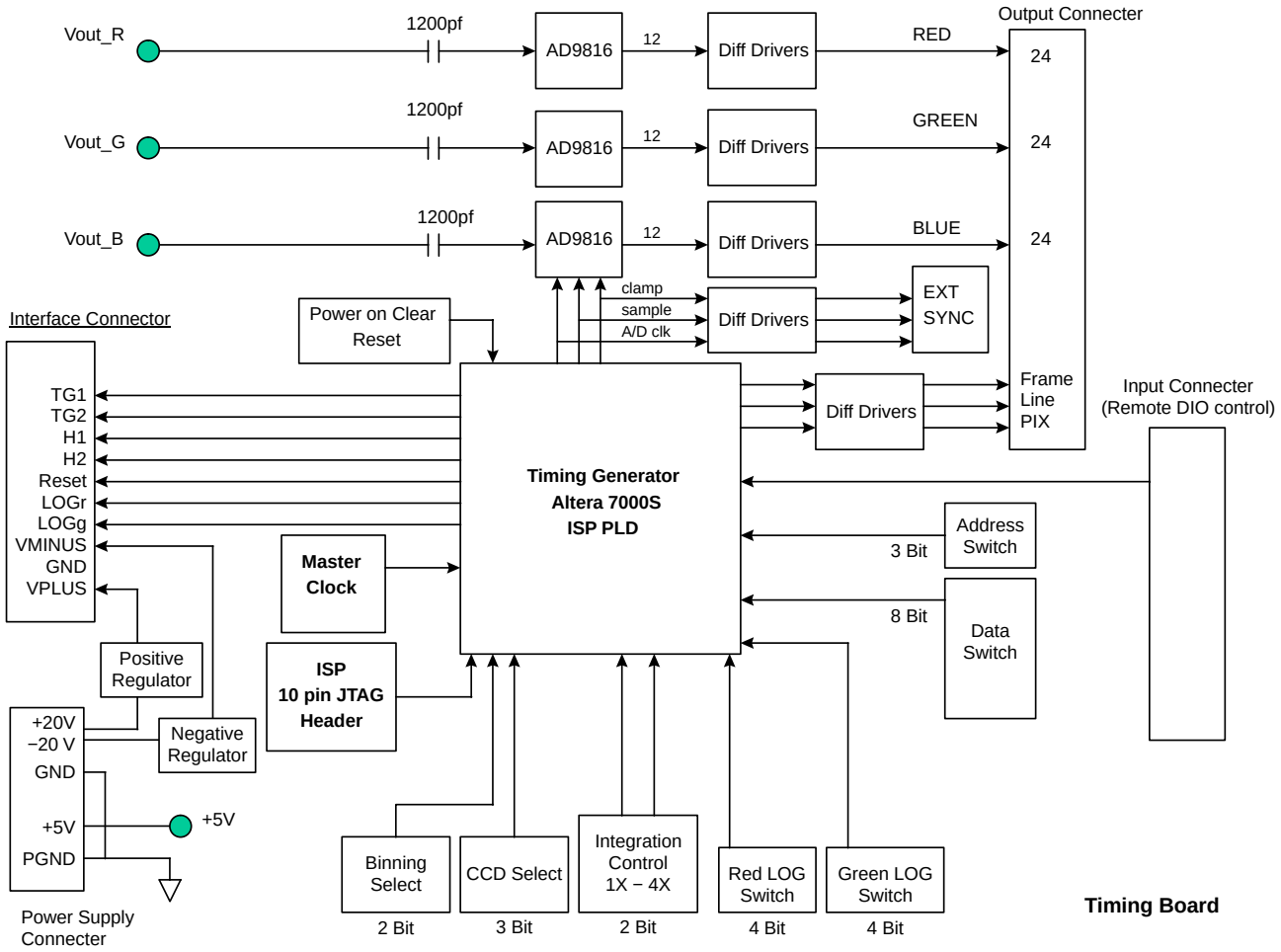


Figure 1. Timing Board Block Diagram (3E8205)

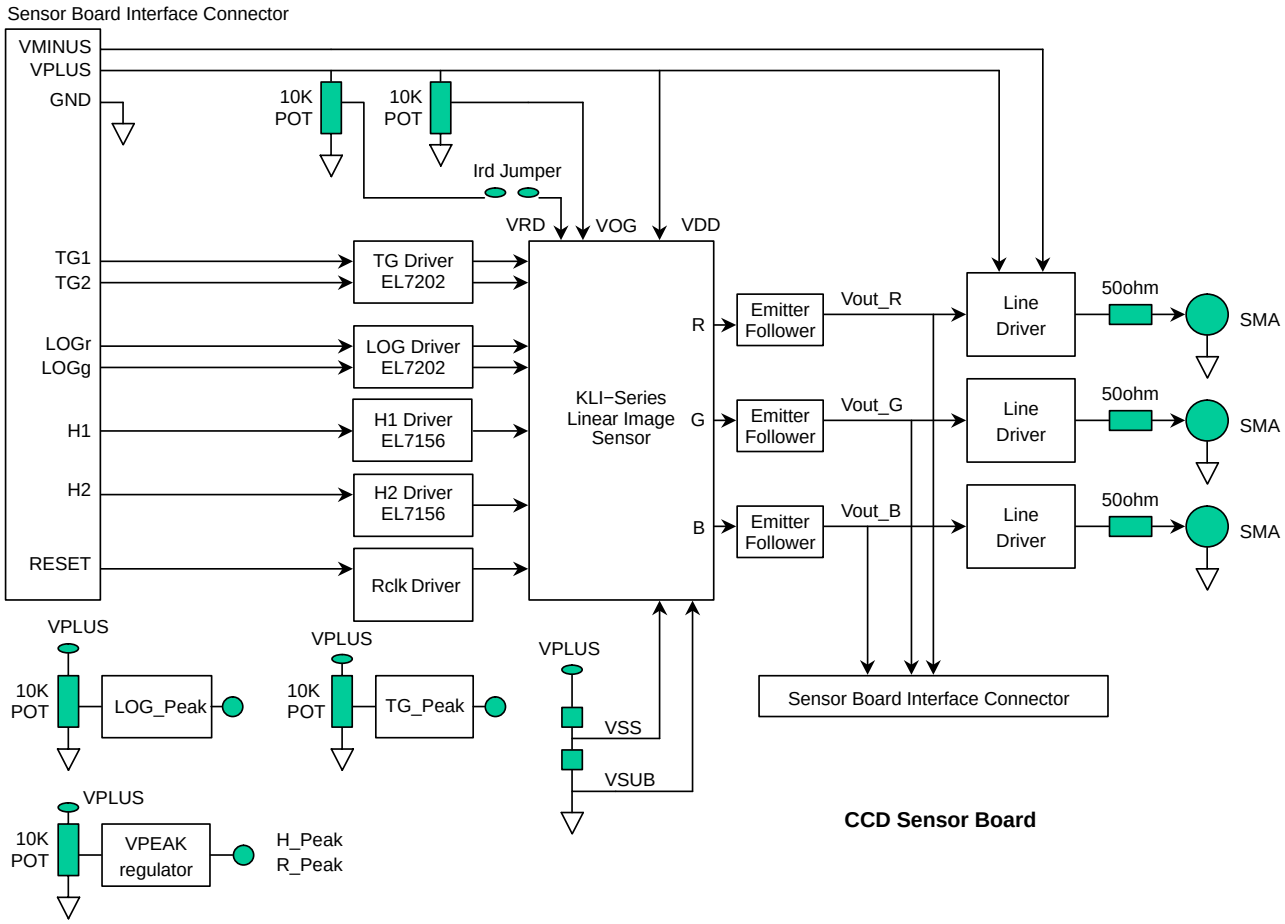


Figure 2. CCD Imager Board Block Diagram (3E8206)

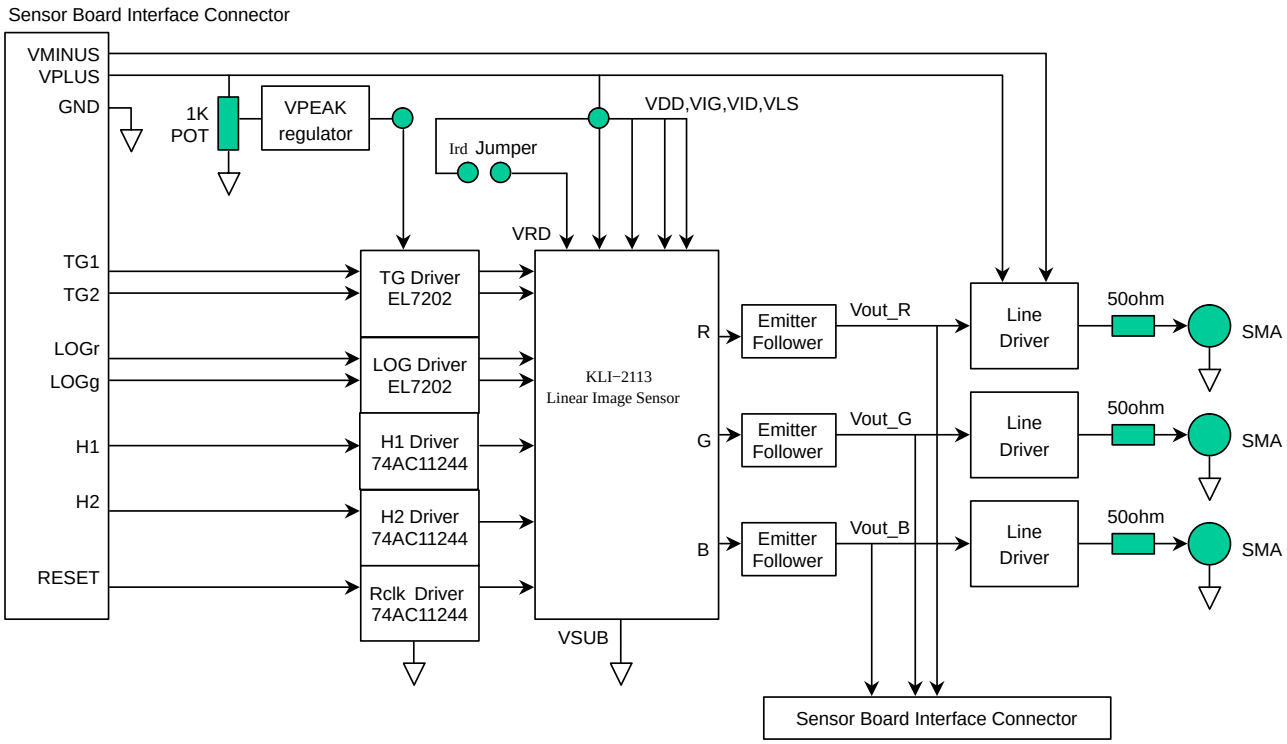


Figure 3. CCD Imager Board Block Diagram (3E8207)

ARCHITECTURE, HIGH LEVEL DESIGN

Timing Generator Board

See Figure 1 for reference.

Master Clock

The Pixel clock frequency is one tenth the Master Clock frequency. The maximum pixel clock frequency is 10 MHz; therefore the maximum master clock frequency is 100 MHz. For slower Pixel clock frequencies, decrease the master clock frequency.

The source of the master clock can be an on-board oscillator, or the clock can be provided via an external timing generator hooked up to the Timing Generator Board via the clock input SMA connector. The default setting of the evaluation board is an on-board 50 MHz master clock, with a pixel clock frequency of 5 MHz.

Timing Generator PLD

The Timing Generator PLD controls the operational flow of the evaluation board. This PLD generates the CCD clock timing, A/D converter timing and frame grabber sync signals timing. The PLD controls the image line length depending on the CCD switch settings. The PLD controls the pixel rate signal generation depending on the binning mode BIN jumper settings. The PLD controls the Transfer Gate timing depending on the integration mode INT switch setting. The PLD also controls the programming of the A/D converters.

A/D Converter: Analog Devices AD9816

The AD9816 is a 12 bit, 6 MSPS CCD analog signal processor. The IC provides on board correlated double sampling (CDS), 8 bit programmable gain, and 8 bit DC offset adjust. The necessary timing signals for the AD9816 are provided by the Timing Generator PLD. Default serial programming of the A/D's registers is provided by the PLD at power up. Alternate programming of its registers can be achieved via external serial interface or by manually setting the address and data switches on the board and pressing the Adjust A/D button.

Power on Clear/Reset

Resets and initializes the board on power up, or when the Board_Reset button in pressed.

JTAG Header

10 pin header, provides the user with the ability to reprogram the Altera 7000S PLDs in system via Altera's ByteBlaster programming hardware.

Input Connector

This connector provides digital input control signals to the evaluation board. This is an optional feature, all control lines can be set via on board switches. No external digital inputs are needed to operate the evaluation board.

Digital Output Connectors

For each channel, Red, Green, and Blue: 12 bits of digital information are output in RS422 differential TTL. Additionally, three frame grabber sync signals are provided in RS422 differential TTL.

EXT_SYNC Connector

This connector provides the Clamp, Sample, A/D clock, and Line_Start signals. These signals can be used to sync up digital conversion of the Analog output of the CCD Sensor Board.

Board Interface Connectors

Provides interface between timing board and sensor boards. The sensor boards route the clock traces from the timing Board to the CCD clock drivers.

Power Supplies

The Timing board is designed to require only a 5 V, 2 A external power supply.

Power connector

The power connector is a 5 pin connector with +5 V, +20 V, −20 V and two AGND connections. Although the Timing board only requires the +5 V supply, all the necessary supplies are brought into the Timing board via this single connector. The power supplies are then regulated and routed up to the Sensor board via the board interface connector.

CCD Imager Board 3E8206

See Figure 2 for reference.

Power Supplies

Power is supplied to the CCD Sensor Board via the Timing Board interface connector. In order to operate, the CCD Sensor board requires a +15 V, 1000 mA external power supply. If it is desired to utilize the analog output mode of operation, an additional −15 V, 200 mA external power supply is required for the video line drivers.

Horizontal Clock Delay Pots

The Φ1 and Φ2 TTL signals can be delayed slightly by adjusting the delay pots on the Sensor board. This allows the Φ1 and Φ2 signals to be adjusted with respect to one another to achieve better crossover points in the Φ1 and Φ2 CCD clocks signals.

CCD Clock Drivers

Φ1, Φ2 Elantec clock drivers are used to generate the Φ clocks. These devices take TTL inputs from the Timing Board and output the voltage levels required by the CCD. The supply voltage of these drivers is regulated and adjustable via a potentiometer (V_PEAK).

TG1, TG2: Elantec clock drivers, designed to drive large capacitance clock gates of a CCD image sensor, are used to

generate the TG clocks. These drivers take TTL inputs from the Timing Board and output the voltage levels required by the CCD. The drivers can source up to 2 A per channel of drive current. The drivers' peak output voltage is adjustable via potentiometer.

LOGr, LOGg: Elantec clock drivers, designed to drive large capacitance clock gates of a CCD image sensor, are used to generate the LOG clocks. These drivers take TTL inputs from the Timing Board and output the voltage levels required by the CCD. The drivers can source up to 2 A per channel of drive current. The drivers' peak output voltage is adjustable via potentiometer.

ΦR: The reset clock driver is a pair of fast switching transistors that can drive the lower capacitance reset gate. The drivers supply voltage is regulated and is adjustable via a potentiometer (V_PEAK).

CCD Bias Voltages

VDD: The VDD bias is de-coupled at the device pin.

VRD: The Reset Drain CCD bias voltage is adjustable via a potentiometer. VRD is de-coupled at the device pin. Access is provided to this bias via a jumper. This allows measurement of the current IRD from which the number of electrons flowing through the Reset Drain can be calculated.

VOG: The Output Gate bias is adjustable via a potentiometer. VOG is de-coupled at the device pin.

VSS: This CCD bias voltage is fixed to be a diode drop above VSUB, about 0.7 V.

VLS: The Light Shield bias voltage is fixed by a resistor divider. The voltage varies depending on which CCD is being operated.

VID: The Input Diode test pin is biased to VDD.

VIG: This Input Gate test pin bias is connected to VSUB. On the L24 sensor board, this pin is biased to VDD.

CCD Image Sensor

This evaluation board supports the KLI−8023 Linear CCD sensor.

Emitter Follower

The video out of the CCD is buffered using a bipolar junction transistor in the emitter follower configuration.

CCD Imager Board 3E8207

See Figure 3 for reference.

Power Supplies

Power is supplied to the CCD Sensor Board via the Timing Board interface connector. In order to operate, the CCD Sensor board requires a +12 V, 1000 mA external power supply. If it is desired to utilize the analog output mode of operation, an additional −15 V, 200 mA external power supply is required for the video line drivers.

CCD Clock Drivers

Φ1, Φ2 CMOS clock drivers are used to generate the Φ clocks. These devices take TTL inputs from the Timing Board and output the voltage levels required by the CCD. The supply voltage of these drivers is regulated and adjustable via a potentiometer (V_PEAK).

TG1, TG2: Elantec clock drivers, designed to drive large capacitance clock gates of a CCD image sensor, are used to generate the TG clocks. These drivers take TTL inputs from the Timing Board and output the voltage levels required by the CCD. The drivers can source up to 2 A per channel of drive current. The drivers' peak output voltage is adjustable via potentiometer (V_PEAK).

LOGr, LOGg: Elantec clock drivers, designed to drive large capacitance clock gates of a CCD image sensor, are used to generate the LOG clocks. These drivers take TTL inputs from the Timing Board and output the voltage levels required by the CCD. The drivers can source up to 2 A per channel of drive current. The drivers' peak output voltage is adjustable via potentiometer (V_PEAK).

ΦR: A CMOS clock driver is used to drive the lower capacitance reset gate. The drivers supply voltage is adjustable via a potentiometer (V_PEAK).

CCD Bias Voltages

VDD: The VDD bias is de-coupled at the device pin.

VID: The Input Diode test pin is biased to VDD.

VIG: The Input Gate test pin is biased to VDD.

VRD: VRD is de-coupled at the device pin. Access is provided to this bias via a jumper. This allows measurement of the current IRD from which the number of electrons flowing through the Reset Drain can be calculated.

CCD Image Sensor

This evaluation board supports the KLI−2113 Linear CCD sensor.

Emitter Follower

The video out of the CCD is buffered using a bipolar junction transistor in the emitter follower configuration.

Board Requirements

Power Supply

The Timing board operates from a +5 V, 2 A or greater power supply.

The Sensor board requires a +20 V, 1000 mA or greater power supply to operate.

If analog output is desired, an additional −20 V, 200 mA external power supply is required for the video line drivers.

Although extensive filtering is done on board, the power supplied to the board must be quiet and stable in order to achieve the best performance possible.

Inputs

Upon power up, the evaluation board is free running and requires no input signals to begin operating.

See CCD Imager Board 3E8206 section for information on additional optional inputs.

Outputs

R[11..0] (±): 12 bits of Differential TTL Digital information.

G[11..0] (±): 12 bits of Differential TTL Digital information.

B[11..0] (±): 12 bits of Differential TTL Digital information.

FRAME (±): Differential TTL frame grabber vertical synchronization signal.

LINE (±): Differential TTL frame grabber horizontal synchronization signal.

PIX (±): Differential TTL frame grabber PIX synchronization signal.

CLAMP (±): Differential TTL signal in sync with the reset level of the CCD output waveform.

SAMPLE (±): Differential TTL signal in sync with the settled Vout portion of the CCD output waveform.

A/D CLOCK (±): Differential TTL signal that can be used by external A/D to digitize the analog output of the CCD Sensor Board.

LINE_START (±): Differential TTL signal that indicates the start of a CCD line.

JTAG Programming

An Altera 7000S In System Programmable (ISP) PLD is used on this board. A ten pin header (J8) is provided to allow for the programming of these PLD's. Because these parts are re-programmable, custom digital logic can be implemented for timing and mode adjustments or additions. Any custom implementation can be made quickly and easily to via the JTAG programming interface provided by this connector.

CONFIGURATION MODES

Line/Switches Modes

The Line/Switches Jumper (JMP6) Selects whether some of the board settings will be controlled externally through the Digital I/O connector (J10), or via the on board switches. If this switch is set to Line, then the integration time and the Binning mode must be set remotely via digital I/O.

AD_INT/EXT Modes

The board comes with three Analog Devices AD9816 12 bit A/D converters on board, one for each color channel. This A/D has several features, such as multiple configurations, programmable gain and offset registers which require initialization and/or programming on power up. The programming of these registers is done via a three wire serial interface.

EXT: A three wire serial interface is provided on the J10 connector of the board and the AD9816's registers can be controlled remotely via these when the A/D_IN/EX Jumper (JMP5) is set to EXT. See Figure 1 for the AD9816 serial timing diagrams and information.

INT: If it is not desired to control the programming of the A/D's registers remotely, set jumper JMP5 to INT. The Timing generator PLD contains a state machine that serially loads in the following default values to these registers upon power up or board reset.

A/D Default Register Settings

# channels:	1
Mode:	CDS Mode
Input Span:	3 V
Channel Selected:	Green
Red PGA Gain*:	1
Green PGA Gain:	1
Blue PGA Gain*:	1
Red Offset*:	0 mv
Green Offset:	0 mv
Blue Offset*:	0 mv

* Although the Red and Blue A/D converter channels are not used, these registers are still initialized to these default settings.

Adjustments

Adjustments can be made to each A/D's registers during operation of the board by utilizing the DATA Dipswitch (SW7), the ADDRESS switch (SW6) and the ADJ_AD button. After setting SW6 to the desired Address, and SW7 to the desired Data, pressing the ADJ_AD button will load the new value into the Timing generator PLD and a state machine inside the PLD will then serial load the new data into the A/D's register.

Each AD9816 uses the Green Input channel pin for its video input. This is done to ease the default programming of all three A/D's on power up and reset.

When the AD_INT/EXT jumper is set to INT, each channel can be manually adjusted independently of the others by selecting which channel(s) to adjust using the channel select jumpers (JMP2, JMP3, JMP4).

When the AD_INT/EXT jumper is set to EXT, each channel can be remotely adjusted independently of the others by selecting which channel to adjust using the three independent SLOAD signals (SLOAD_R, SLOAD_G, SLOAD_B). See Figure 1 for more information on the AD9816's registers.

CCD Modes

The CCD Select switch (SW5) setting determines the line length timing. This switch should be set according to which CCD sensor board is being used.

See Table 4 for additional information.

Binning Modes

The BIN Select jumper (JMP7) setting determines the Binning mode operation. See Table 5 for additional information.

When no jumper is installed in JMP7, the Timing Generator board will operate according to the CCD device specification sheet timing diagram.

When JMP7 is configured in BIN2 mode the timing will be modified to allow two pixels worth of charge to accumulate on the CCD's floating diffusion before being reset.

When JMP7 is configured in BIN4 mode the timing will be modified to allow four pixels worth of charge to accumulate on the CCD's floating diffusion before being reset.

Integration Modes

The INT Select switch (SW4) settings determine the Integration time. See Table 6 for additional information.

The INT Select switch determines how many line times worth of charge will accumulate in the photodiode before being transferred into the CCD register and clocked out of the CCD.

Exposure Control Modes

The GREEN_LOG switch (SW3) settings determine the green channel exposure control duration. The RED_LOG switch settings determine the red channel exposure control duration.

The LOG switches determine how long the LOG signal will be turned on.

See Table 7 for additional information.

Adjustments

Adjustments that may be made to the circuit boards are addressed in the following sections.

Fixed Bias Voltages

Table 2. FIXED BIAS VOLTAGES

Bias	KLI−2113	KLI−8023
VSUB	0 V	0 V
VSS	−	0.65 V
VIG	12 V	0 V
PHI A	−	−

Variable Clock and Bias Voltages (see Table 3)

Table 3. VARIABLE CLOCK AND BIAS VOLTAGES

Supply	Minimum	Nominal	Maximum
VDD	12 V	15 V	TIMING BOARD
VLS	12 V	15 V	TIMING BOARD
VID	12 V	15 V	TIMING BOARD
VRD	12 V	11 V	SENSOR BOARD
VOG	−	0.75 V	SENSOR BOARD

Voltage	KLI−2113	KLI−8023	Location
TG PEAK	5 V	6.5 V	SENSOR BOARD
LOG PEAK	5 V	6.5 V	SENSOR BOARD
HCLK PEAK	5 V	6.5 V	SENSOR BOARD
RESET PEAK	5 V	6.5 V	SENSOR BOARD

NOTE: These voltages are optimized for the particular CCD being used and are fixed at the factory. Adjustments should not be made to them without consultation with ON Semiconductor.

Timing

Fixed Timing

TG1, TG2, LINE, FRAME

See Figure 4 for additional information.

Variable Timing

Φ1, Φ2 (Depending on CCD Select Switch)
ΦR (Binning Modes)
CLAMP (Binning Modes)
SAMPLE (Binning Modes)
A/D Clock (Binning modes)

See Figure 5 and Figure 6 for additional information.

Other Variable Parameters

Pixel Frequency: The pixel rate frequency can be varied by changing the Master clock oscillator, or by utilizing the external clock feature.

Line Length: (Depends on CCD switch setting)

TG1 Width: (Depends on pixel frequency, 21 pixel counts wide)

TG2 Width: (Depends on pixel frequency, 26 pixel counts wide)

Table 4. CCD MODES

CCD Switch Setting	CCD	Pixels/Line
0	Test 0	2872
1	Test 5	6372
2	KLI−8013	8572
3	Test 3	10372
4	KLI−2113	2472
5	Test 4	14972
6	Test 1	172
7	Test 2	14972

Table 5. BINNING MODES

JMP7 Setting	Binning Mode
No Jumper	1×1
BIN2	2×2
BIN4	4×4

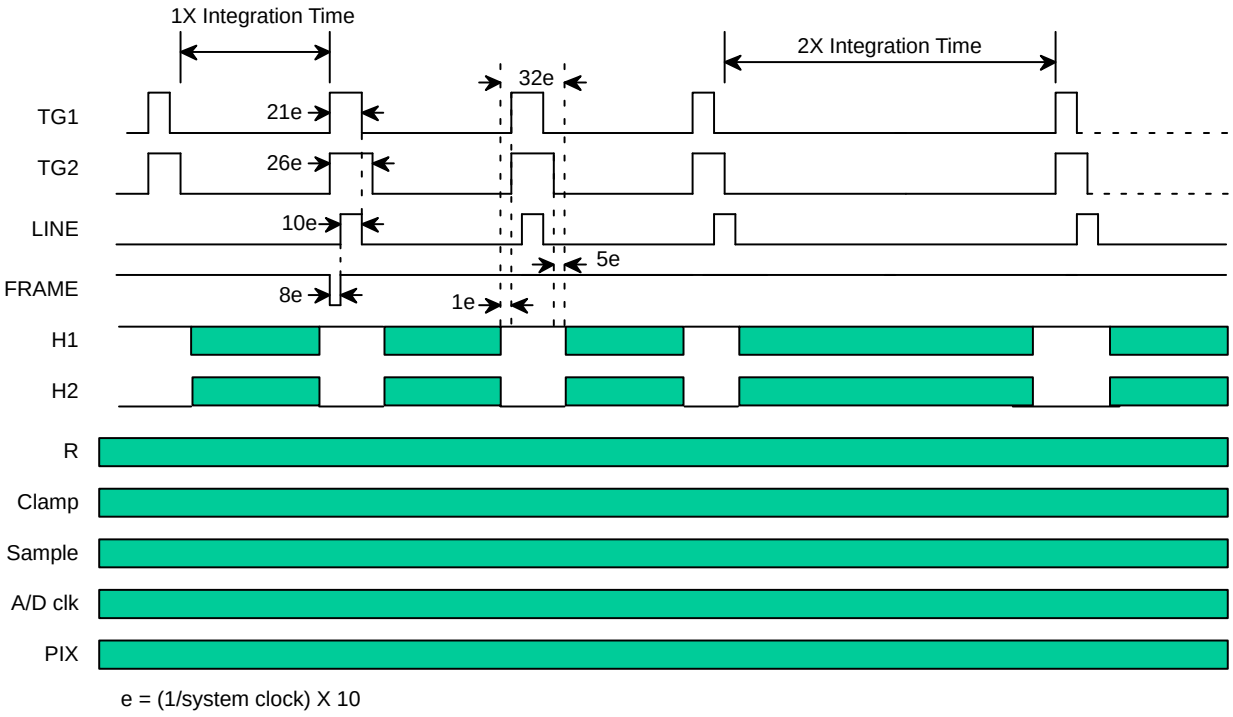
Table 6. INTEGRATION TIMING MODES

INT Switch Setting (SW4)	Integration Time
0	1 × Line Time
1	2 × Line Time
2	3 × Line Time
3	4 × Line Time
4	1 × Line Time
5	2 × Line Time
6	3 × Line Time
7	4 × Line Time

Table 7. LOG MODES

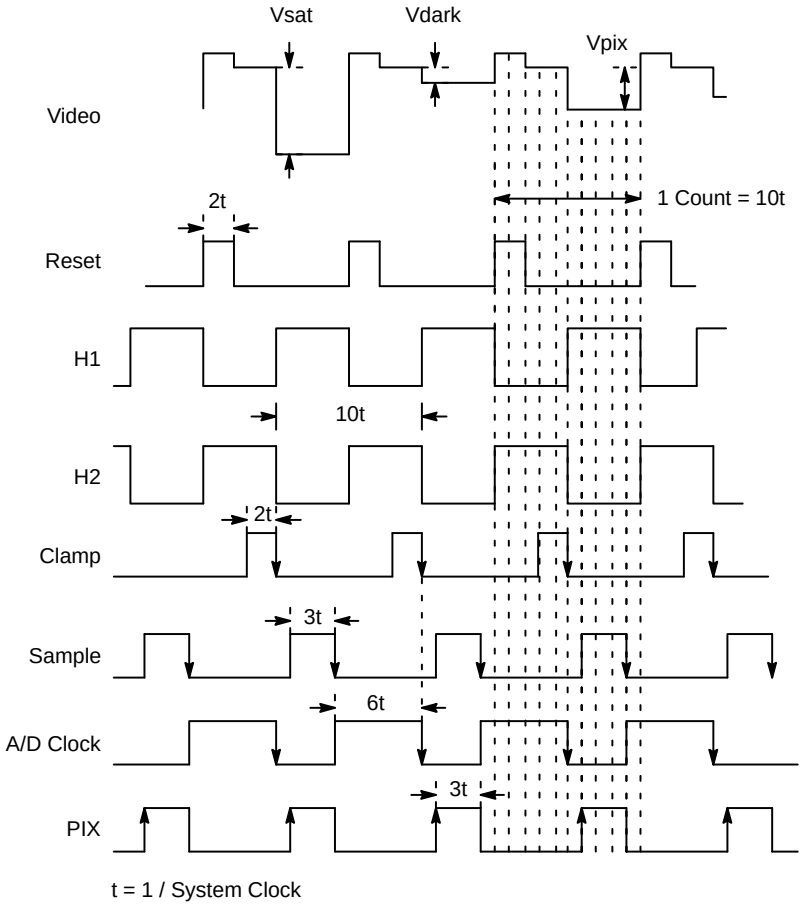
LOG Switch Setting	Number of Pixels per Line
(SW1, SW3)	LOG is ON
0	0 (Never ON, Always LOW)
1	500
2	1000
3	1500
4	2000
5	2500
6	3000
7	3500
8	4000
9	4500
10	5000
11	5500
12	6000
13	6500
14	7000
15	Always ON, LOW Only During TG Period

Frame Timing



e = (1/system clock) X 10

Figure 4. Line Rate Timing



t = 1 / System Clock

Figure 5. Pixel Rate Timing for Devices KLI−8023, KLI−2113

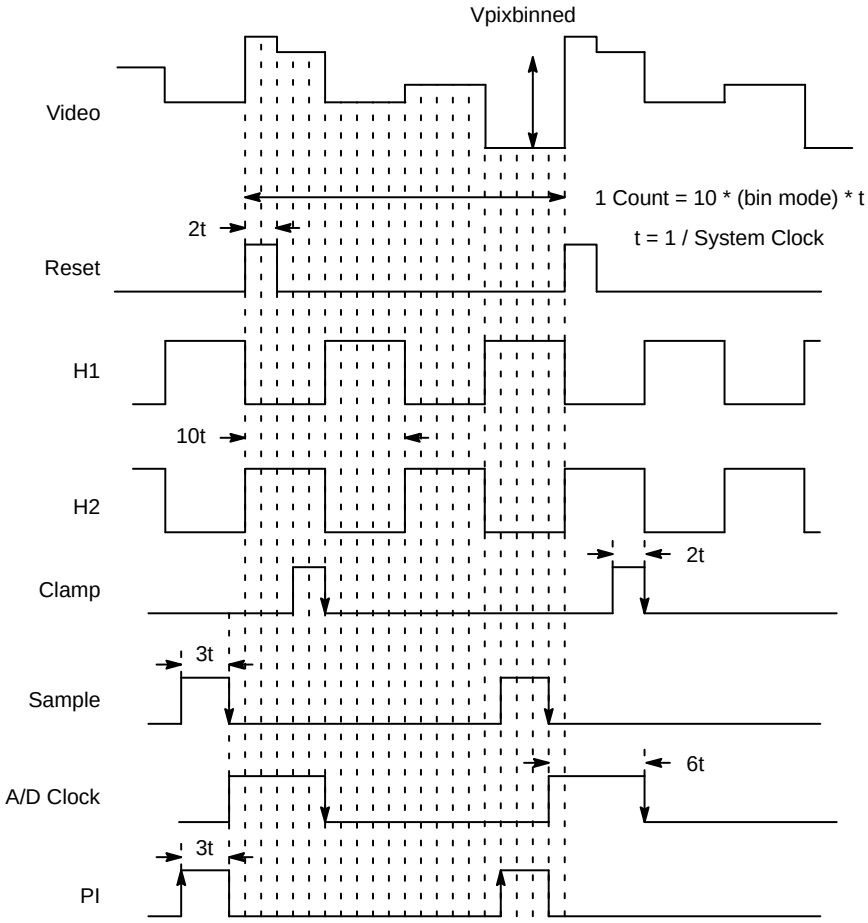


Figure 6. Pixel Summing (2 Pixel Summing Shown)

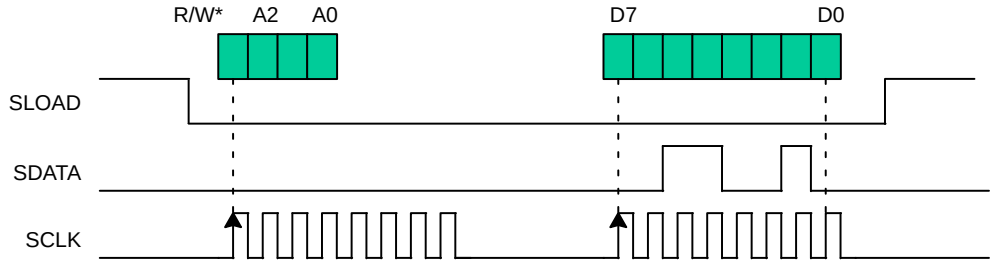
In Binning Modes, the Frequency of the Reset, clamp, sample, A/D, and PIX clocks are decreased in order to allow charge to accumulate on the output node of the CCD before being reset.

AD9816 REGISTER CONFIGURATION

Table 8. AD9816 REGISTER CONFIGURATION

Address	Register		Function	Default Programming
0	Configuration Register			
	Bit 7 MSB	Test Mode Bit	Always 0	0
	Bit 6	Test Mode Bit	Always 0	0
	Bit 5	CDS Mode Bit	High for CDS	1
			Low for SHA Mode	
	Bit 4	Input Span	High for 3 V	1
	Bit 3	Input Span	High for 1.5 V	0
	Bit 2	Channel Mode	High for 3 Channel	0
	Bit 1	Channel Mode	High for 1 Channel	1
	Bit 0	Test Mode Bit	Always 0	0
1	MUX Register			
	Bit 7	Test Mode Bit	Always 0	0
	Bit 6	Channel Sequence	High for BGR	0
	Bit 5	Channel Sequence	High for RGB	0
	Bit 4	Channel Select	High for Red	0
	Bit 3	Channel Select	High for Green	1
	Bit 2	Channel Select	High for Blue	0
	Bit 1	Test Mode Bit	Always 0	0
	Bit 0	Test Mode Bit	Always 1	1
2	Red PGA Register		1X to 6X (Note 1)	0 (1X)
3	Green PGA Register		1X to 6X (Note 1)	0 (1X)
4	Blue PGA Register		1X to 6X (Note 1)	0 (1X)
5	Red Offset Register		−100 mv to 100 mv (Note 2)	0 (0 mV)
6	Green Offset Register		−100 mv to 100 mv (Note 2)	0 (0 mV)
7	Blue Offset Register		−100 mv to 100 mv (Note 2)	0 (0 mV)

1. PGA Gain = 1+ (Gain Code / 51.2)
2. 01111111 = +100 mV, 00000000 = 0 mV, 11111111 = −100 mV



3 Wire Serial Interface Timing
* R/W Low for Write, High for Read

Figure 7. AD9816 Register Configuration

BOARD INPUTS, OUTPUTS, SWITCHES

Switches

LINE/SW	Selects whether operating modes are controlled via DIO or switches on the board.
A/D INT/EXT	Selects whether A/D programming is controlled via DIO or switches on the board.
INT/EXT_CLK	Selects whether Master clock is input via the on board clock IC or external clock source.
DIGITAL _OUTPUTS	ON enables outputs of AD9816's, OFF tri-states outputs and output drivers
CCD [2..0]	Sets line length timing for the CCD selected
INT_SEL [1..0]	Integration timing control settings switch
SW_BIN2, SW_BIN4	Binning mode control settings jumper
GREEN_LOG [3..0]	Green channel exposure control settings switch
RED_LOG [3..0]	Red channel exposure control settings switch
ADDR [2..0]	Register select switch for programming of AD9816's (AD INT/EXT = INT)
DATA [7..0]	Data dipswitch for programming of AD9816's register (AD INT/EXT = INT)
BLUE_SEL	Enables loading of blue channel A/D converter (AD INT/EXT = INT)
RED_SEL	Enables loading of red channel A/D converter (AD INT/EXT = INT)
GREEN_SEL	Enables loading of green channel A/D converter (AD INT/EXT = INT)

Inputs

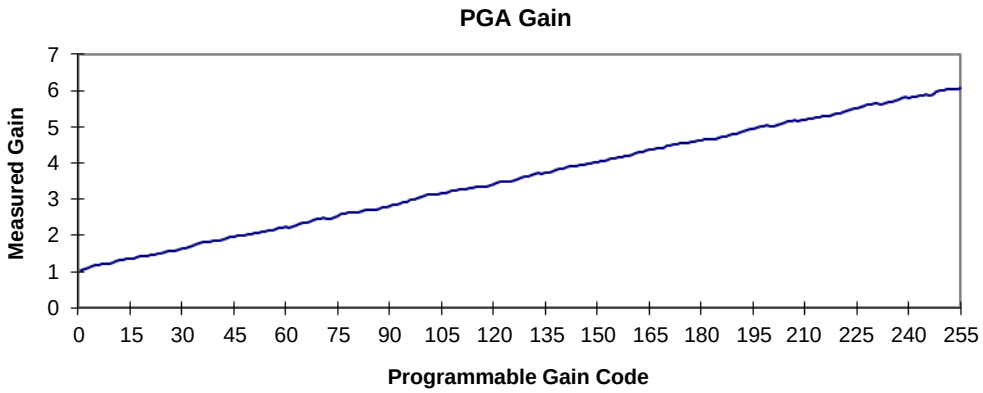
Master_clk	10X Pixel clock (100 MHz maximum)
INT [1..0]	DIO Integration timing control lines
BIN2, BIN4	DIO Binning mode control lines
GLOG [3..0]	DIO Green channel exposure control lines
RLOG [3..0]	DIO Red channel exposure control lines
SCLOCK	Serial clock for external programming of AD9816's registers
SDATA	Serial Data for external programming of AD9816's registers
SLOAD_R	Serial load enable of red channel AD9816
SLOAD_G	Serial load enable of green channel AD9816
SLOAD_B	Serial load enable of blue channel AD9816
JTAG Header	10 pin header for ISP

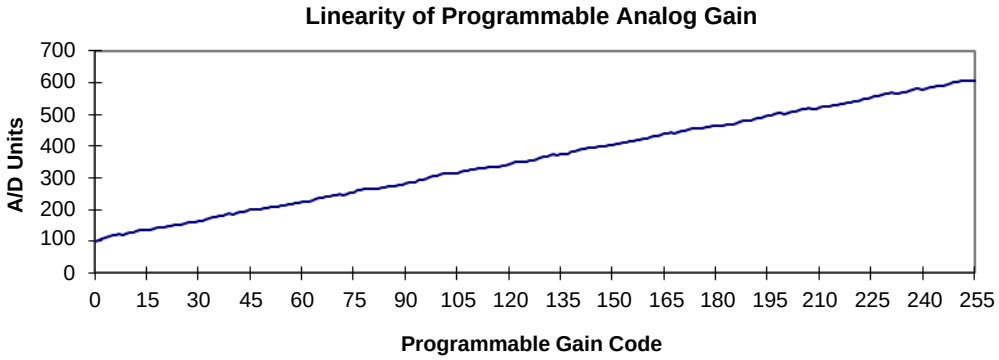
Outputs

R11..0](±)	12 Bits Differential TTL Digital information
G11..0](±)	12 Bits Differential TTL Digital information
B11..0](±)	12 Bits Differential TTL Digital information
FRAME (±)	Differential TTL frame grabber frame sync signal
LINE (±)	Differential TTL frame grabber line sync signal
PIX (±)	Differential TTL frame grabber pixel sync signal
CLAMP (±)	Differential TTL sync signal
SAMPLE (±)	Differential TTL sync signal
A/D CLOCK (±)	Differential TTL sync signal
LINE START (±)	Differential TTL sync signal

Table 9. DYNAMIC RANGE

Dynamic Range vs. KLI-Series CCD (Frequency = 5 MHz)						
KLI-Series CCD	**Maximum System Noise Floor (Electrons)**	**Typical Full Well (Electrons)**	**System Dynamic Range (dB)**	**System Dynamic Range (Bits)**	**System Gain**	**# Electrons per A/D Unit**
KLI−2113	77	170000	66.88	11.11	1X	64
KLI−8023	62	185000	69.5	11.54	1X	52





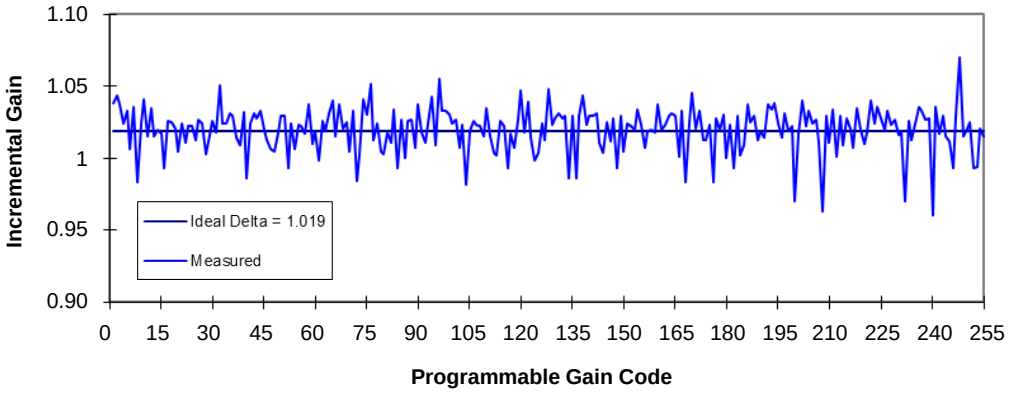
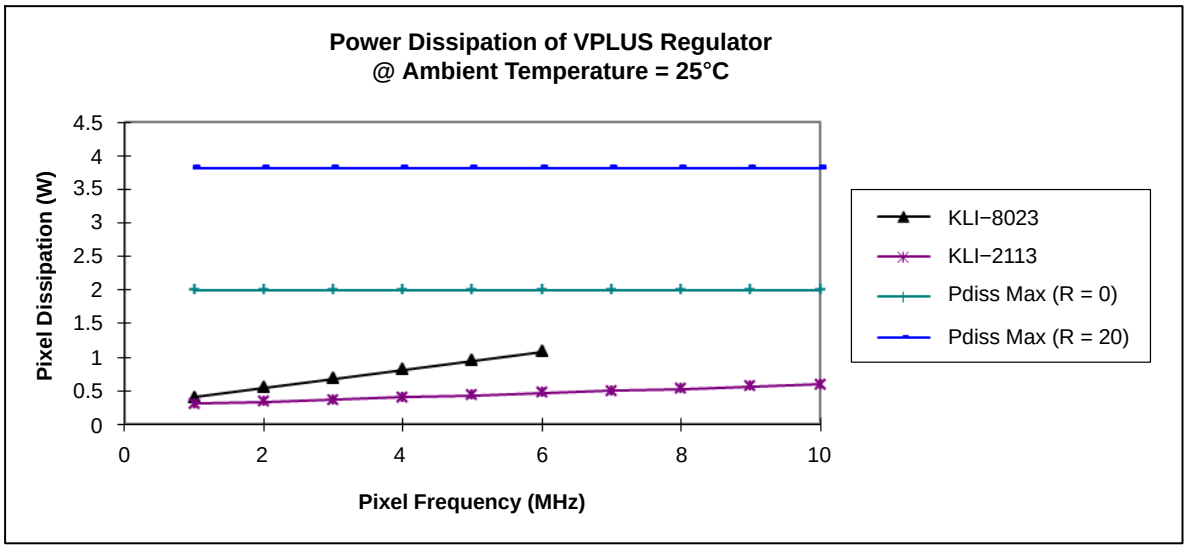


Figure 8. Measured Performance: A/D Programmable Gain



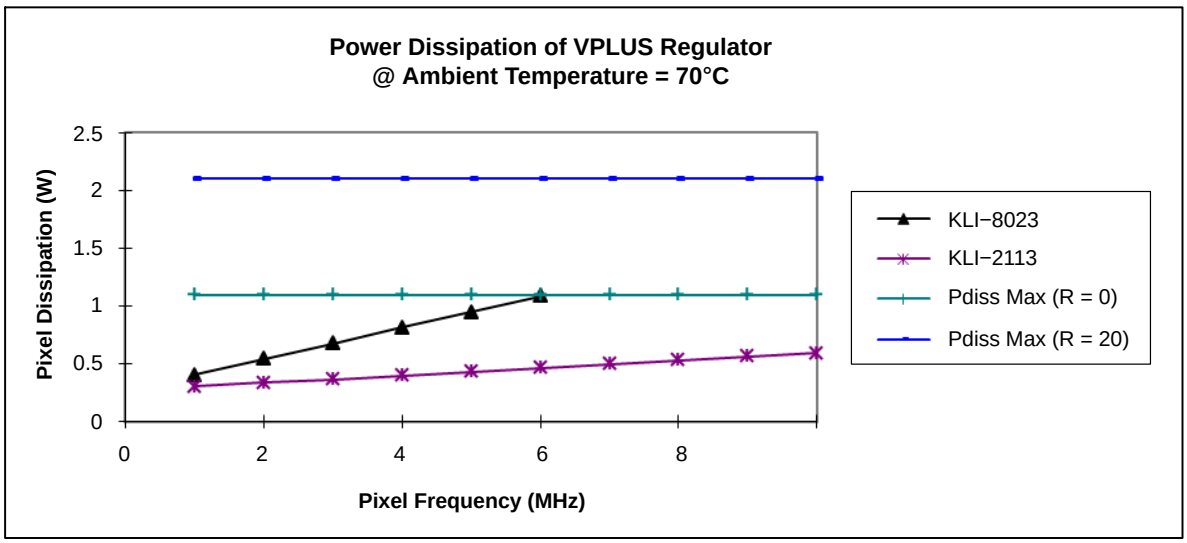
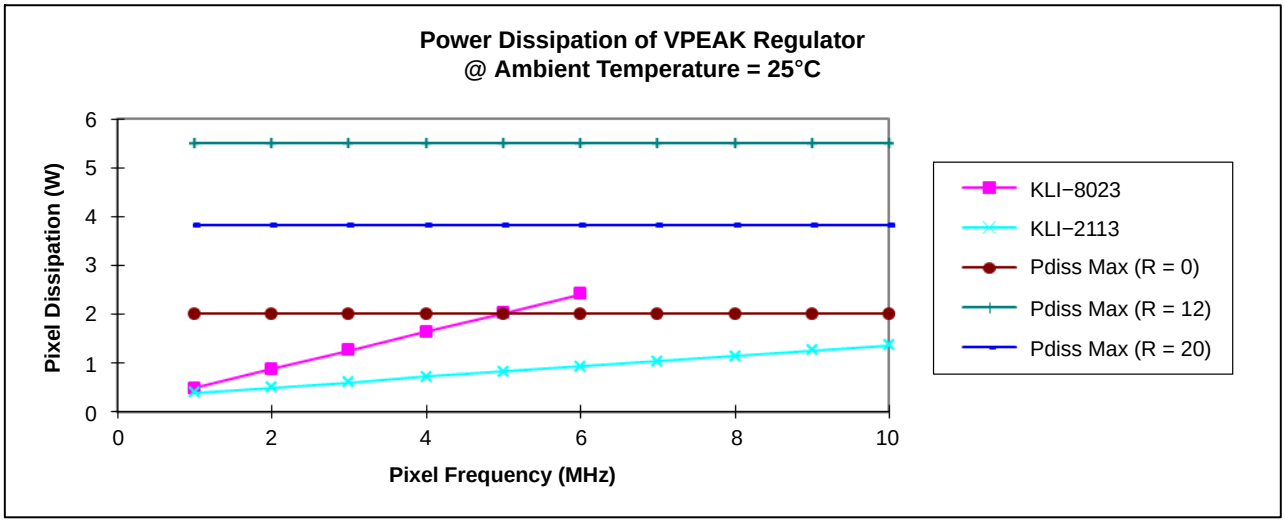


Figure 9. VPLUS Regulator Heatsinking Requirements

NOTE: Depending on the Operating rate and ambient temperature, a heatsink may be required for the VPLUS positive voltage regulator U3. Figure 9 shows the maximum power the regulator can dissipate without a heatsink (R = 0) and with a heatsink with heatsink-to-ambient thermal resistance equal to 20°C per Watt (R = 20)



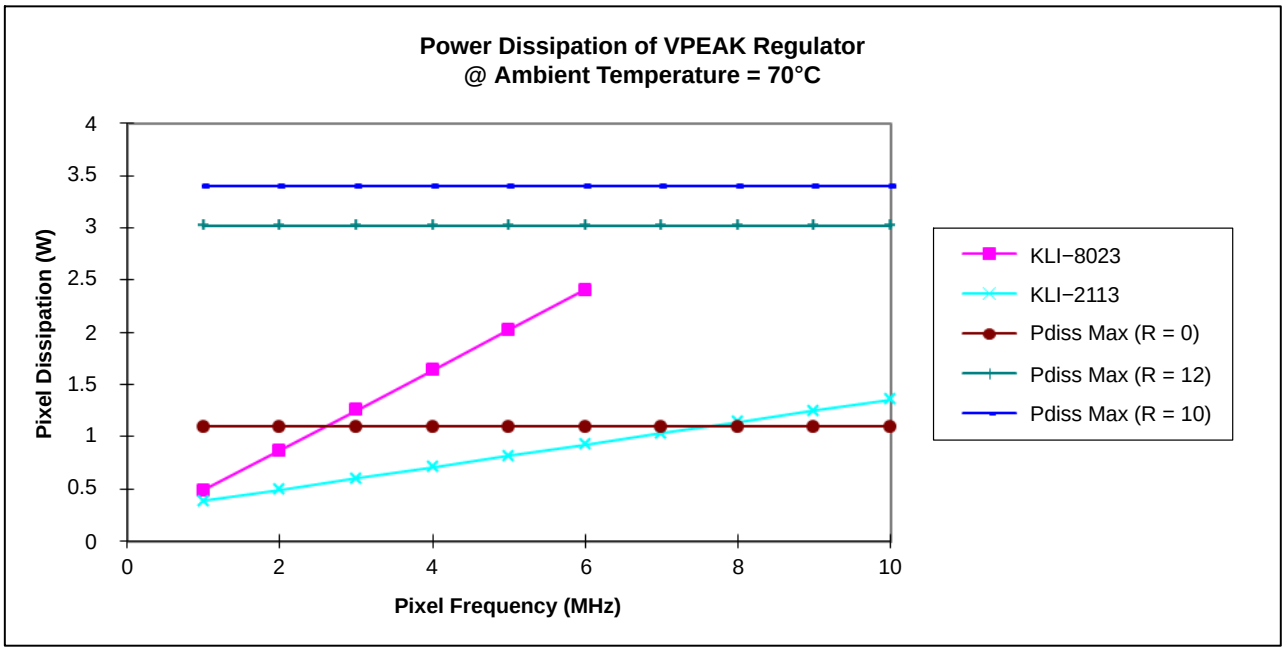


Figure 10. VPEAK Regulator Heatsinking Requirements

NOTE: Depending on the Operating rate and ambient temperature, a heatsink may be required for the VPEAK positive voltage regulator on the CCD Sensor Board. Figure 10 shows the maximum power the regulator can dissipate without a heatsink (R=0) and with heatsinks with heatsink-to-ambient thermal resistance equal to 10 and 12°C per Watt. (R=10, R=12)

CONNECTOR PINOUTS

Table 10. BOARD INTERFACE CONNECTORS J12, J15

Connector	Pin	Assignment	Connector	Pin	Assignment
J12	1	RED_LOG	J15	1	CLAMP_B
J12	2	VSUB	J15	2	VSUB
J12	3	GRN_LOG	J15	3	VIDEO_OUTG
J12	4	VSUB	J15	4	VSUB
J12	5	H2_OUT	J15	5	N.C.
J12	6	H1_OUT	J15	6	VSUB
J12	7	TG1_OUT	J15	7	VIDEO_OUTB
J12	8	VSUB	J15	8	VSUB
J12	9	TG2_OUT	J15	9	N.C.
J12	10	VSUB	J15	10	VSUB
J12	11	N.C.	J15	11	N.C.
J12	12	VSUB	J15	12	VSUB
J12	13	N.C.	J15	13	SAMPLE_B
J12	14	VSUB	J15	14	VSUB
J12	15	N.C.	J15	15	N.C.
J12	16	VSUB	J15	16	VSUB
J12	17	N.C.	J15	17	RESET CLK
J12	18	VSUB	J15	18	VSUB
J12	19	CLAMP_A	J15	19	N.C.
J12	20	VSUB	J15	20	VSUB
J12	21	VIDEO_OUTR	J15	21	VMINUS
J12	22	VSUB	J15	22	VPLUS
J12	23	N.C.	J15	23	VMINUS
J12	24	VSUB	J15	24	VPLUS

Table 11. INPUT CONNECTOR J10

Pin	Assignment	Pin	Assignment
1	RLOG0	2	GND
3	RLOG1	4	GND
5	RLOG2	6	GND
7	RLOG3	8	GND
9	GLOG0	10	GND
11	GLOG1	12	GND
13	GLOG2	14	GND
15	GLOG3	16	GND
17	BIN2	18	GND
19	BIN4	20	GND
21	INT0	22	GND
23	INT1	24	GND
25	SCLOCK	26	GND
27	SDATA	28	GND
29	SLOAD_R	30	GND
31	SLOAD_G	32	GND
33	SLOAD_B	34	GND
35	N.C.	36	GND

Table 11. INPUT CONNECTOR J10 (continued)

Pin	Assignment	Pin	Assignment
37	N.C.	38	GND
39	BOARD_RESET	40	GND

Table 12. GREEN OUTPUT CONNECTOR J6

Connector	Pin	Assignment	Comment
J6	1	G0+	RS422
J6	2	G0−	RS422
J6	3	G1+	RS422
J6	4	G1−	RS422
J6	5	GND	
J6	6	G2+	RS422
J6	7	G2−	RS422
J6	8	G3+	RS422
J6	9	G3−	RS422
J6	10	GND	
J6	11	G4+	RS422
J6	12	G4−	RS422
J6	13	G5+	RS422
J6	14	G5−	RS422
J6	15	GND	
J6	16	G6+	RS422
J6	17	G6−	RS422
J6	18	G7+	RS422
J6	19	G7−	RS422
J6	20	GND	
J6	21	G8+	RS422
J6	22	G8−	RS422
J6	23	G9+	RS422
J6	24	G9−	RS422
J6	25	GND	
J6	26	G10+	RS422
J6	27	G10−	RS422
J6	28	G11+	RS422
J6	29	G11−	RS422
J6	30	GND	
J6	31	FRAME+	RS422
J6	32	FRAME−	RS422
J6	33	LINE+	RS422
J6	34	LINE−	RS422
J6	35	GND	
J6	36	PIX+	RS422
J6	37	PIX−	RS422
J6	38	N.C.	
J6	39	N.C.	
J6	40	N.C.	

Table 13. RED OUTPUT CONNECTOR J7

Connector	Pin	Assignment	Comment
J7	1	R0+	RS422
J7	2	R0−	RS422
J7	3	R1+	RS422
J7	4	R1−	RS422
J7	5	GND	
J7	6	R2+	RS422
J7	7	R2−	RS422
J7	8	R3+	RS422
J7	9	R3−	RS422
J7	10	GND	
J7	11	R4+	RS422
J7	12	R4−	RS422
J7	13	R5+	RS422
J7	14	R5−	RS422
J7	15	GND	
J7	16	R6+	RS422
J7	17	R6−	RS422
J7	18	R7+	RS422
J7	19	R7−	RS422
J7	20	GND	
J7	21	R8+	RS422
J7	22	R8−	RS422
J7	23	R9+	RS422
J7	24	R9−	RS422
J7	25	GND	
J7	26	R10+	RS422
J7	27	R10−	RS422
J7	28	R11+	RS422
J7	29	R11−	RS422
J7	30	GND	
J7	31	FRAME+	RS422
J7	32	FRAME−	RS422
J7	33	LINE+	RS422
J7	34	LINE−	RS422
J7	35	GND	
J7	36	PIX+	RS422
J7	37	PIX−	RS422
J7	38	N.C.	
J7	39	N.C.	
J7	40	N.C.	

Table 14. BLUE OUTPUT CONNECTOR J4

Connector	Pin	Assignment	Comment
J4	1	B0+	RS422
J4	2	B0−	RS422
J4	3	B1+	RS422
J4	4	B1−	RS422
J4	5	GND	
J4	6	B2+	RS422
J4	7	B2−	RS422
J4	8	B3+	RS422
J4	9	B3−	RS422
J4	10	GND	
J4	11	B4+	RS422
J4	12	B4−	RS422
J4	13	B5+	RS422
J4	14	B5−	RS422
J4	15	GND	
J4	16	B6+	RS422
J4	17	B6−	RS422
J4	18	B7+	RS422
J4	19	B7−	RS422
J4	20	GND	
J4	21	B8+	RS422
J4	22	B8−	RS422
J4	23	B9+	RS422
J4	24	B9−	RS422
J4	25	GND	
J4	26	B10+	RS422
J4	27	B10−	RS422
J4	28	B11+	RS422
J4	29	B11−	RS422
J4	30	GND	
J4	31	FRAME+	RS422
J4	32	FRAME−	RS422
J4	33	LINE+	RS422
J4	34	LINE−	RS422
J4	35	GND	
J4	36	PIX+	RS422
J4	37	PIX−	RS422
J4	38	N.C.	
J4	39	N.C.	
J4	40	N.C.	

Table 15. POWER CONNECTOR J11

Connector	Pin	Assignment
J11	1	+5 V
J11	2	SUPPLY GND
J11	3	NEG SUPPLY (−20 V)
J11	4	SUPPLY GND
J11	5	POS SUPPLY (+20 V)

Table 16. JTAG CONNECTOR J8

Connector	Pin	Assignment
J8	1	TCK
J8	2	GND
J8	3	TDO
J8	4	+5 V
J8	5	TMS
J8	6	N.C.
J8	7	N.C.
J8	8	N.C.
J8	9	TDI
J8	10	GND

Table 17. EXT SYNC CONNECTOR J1

Connector	Pin	Assignment
J1	1	CLAMP +
J1	2	CLAMP−
J1	3	SAMPLE+
J1	4	SAMPLE−
J1	5	AD_CLK +
J1	6	AD_CLK−
J1	7	LINE_START+
J1	8	LINE_START−
J1	9	GND
J1	10	GND

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ON Semiconductor is not responsible for customer damage to the Timing Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the Truesense Imaging Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

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REFERENCES

[1] KLI−2113 and KLI−8023 Device Specifications
[2] KLI−2113/KLI−8023 Evaluation Board Schematics
[3] Analog Devices AD9816 Product Data Sheet

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