



# EFC6605R

## N-Channel Power MOSFET 20V, 10A, 13.3mΩ, Dual EFCP

ON Semiconductor®

<http://onsemi.com>

### Features

- 2.5V drive
- Protection diode in
- Halogen free compliance
- Common-drain type
- 2KV ESD HBM

### Applications

- Lithium-ion battery charging and discharging switch

### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Value	Unit
Source to Source Voltage	V <sub>SS</sub>		20	V
Gate to Source Voltage	V <sub>GSS</sub>		±10	V
Source Current (DC)	I <sub>S</sub>		10	A
Source Current (Pulse)	I <sub>SP</sub>	PW≤10μs, duty cycle ≤1%	60	A
Total Dissipation	P <sub>T</sub>	Mounted on ceramic substrate (5000mm <sup>2</sup> ×0.8mm)	1.6	W
Junction Temperature	T <sub>J</sub>		150	°C
Storage Temperature	T <sub>g</sub>		-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Junction to Ambient When mounted on ceramic substrate (5000mm <sup>2</sup> ×0.8mm)	RθJA	78.1	°C/W

#### Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Source to Source Breakdown Voltage	V(BR) <sub>SS</sub>	I <sub>S</sub> =1mA, V <sub>GS</sub> =0V Test Circuit 1	20			V
Zero-Gate Voltage Source Current	I <sub>SSS</sub>	V <sub>SS</sub> =20V, V <sub>GS</sub> =0V Test Circuit 1			1	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±8V, V <sub>SS</sub> =0V Test Circuit 2			±1.0	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>SS</sub> =10V, I <sub>S</sub> =1mA Test Circuit 3	0.5		1.3	V
Forward Transconductance	g <sub>FS</sub>	V <sub>SS</sub> =10V, I <sub>S</sub> =3A Test Circuit 4		11.4		S
Static Source to Source On-State Resistance	R <sub>SS(on)1</sub>	I <sub>S</sub> =3A, V <sub>GS</sub> =4.5V Test Circuit 5	8.8	11.1	13.3	mΩ
	R <sub>SS(on)2</sub>	I <sub>S</sub> =3A, V <sub>GS</sub> =4.0V Test Circuit 5	9.1	11.4	13.7	mΩ
	R <sub>SS(on)3</sub>	I <sub>S</sub> =3A, V <sub>GS</sub> =3.8V Test Circuit 5	9.3	11.6	13.9	mΩ
	R <sub>SS(on)4</sub>	I <sub>S</sub> =3A, V <sub>GS</sub> =3.1V Test Circuit 5	10.0	12.5	15.6	mΩ
	R <sub>SS(on)5</sub>	I <sub>S</sub> =3A, V <sub>GS</sub> =2.5V Test Circuit 5	11.1	13.9	17.4	mΩ

Continued on next page.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

EFC6605R

Continued from preceding page.

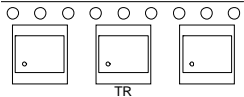
Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Turn-ON Delay Time	$t_{d(on)}$	$V_{SS}=10V, V_{GS}=4.5V, I_S=3A$ Test Circuit 6		154		ns
Rise Time	$t_r$			678		ns
Turn-OFF Delay Time	$t_{d(off)}$			44400		ns
Fall Time	$t_f$			60800		ns
Total Gate Charge	$Q_g$	$V_{SS}=10V, V_{GS}=4.5V, I_S=10A$ Test Circuit 7		19.8		nC
Forward Source to Source Voltage	$V_F(S-S)$	$I_S=3A, V_{GS}=0V$ Test Circuit 8		0.75	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

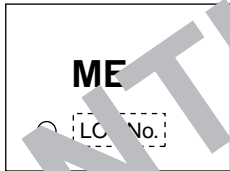
Ordering & Package Information

Device	Package	Shipping	note
EFC6605R-TR	EFCP	5,000 pcs. / reel	Pb-Free and Halogen Free

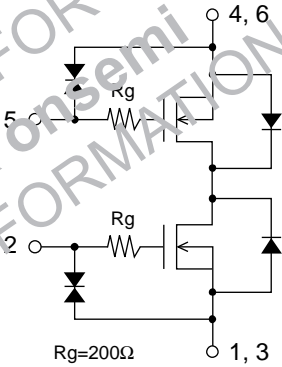
Packing Type: TR



Marking

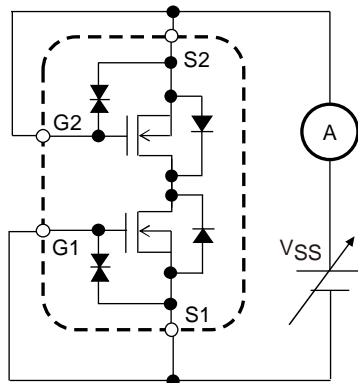


Electrical Connection

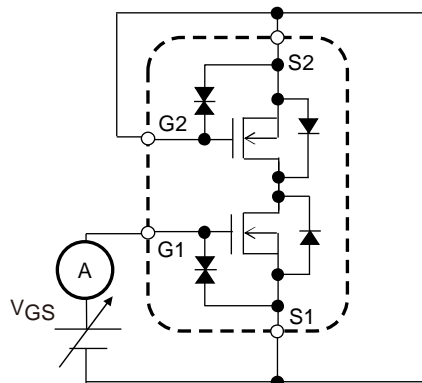


# Test circuits are example of measuring FET1 side

Test Circuit 1  
ISSS

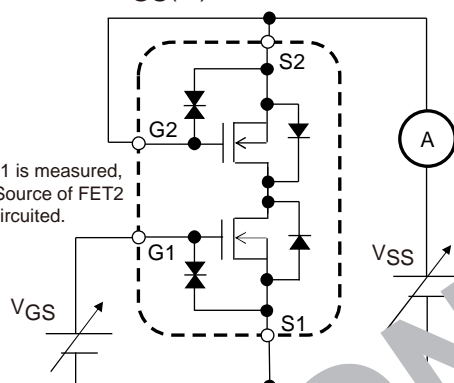


Test Circuit 2  
IGSS



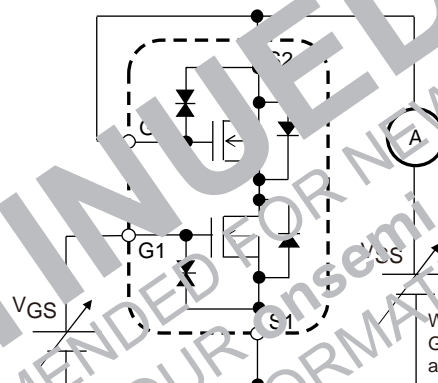
When FET1 is measured,  
Gate and Source of FET2  
are short-circuited.

Test Circuit 3  
VGS(th)



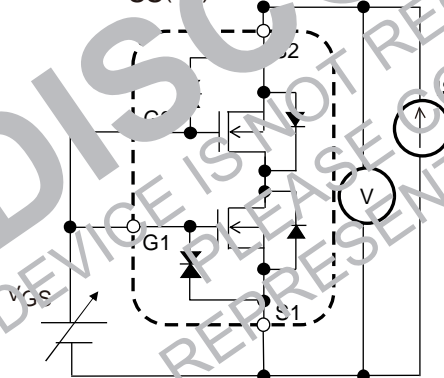
When FET1 is measured,  
Gate and Source of FET2  
are short-circuited.

Test Circuit 4  
gFS

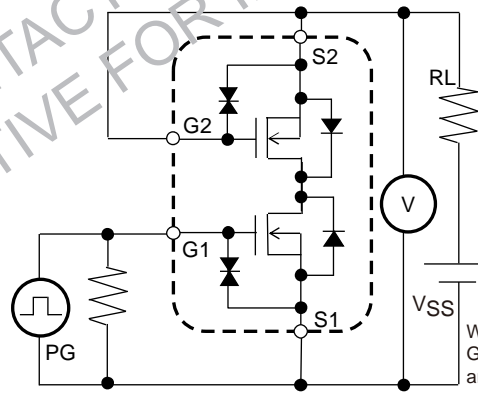


When FET1 is measured,  
Gate and Source of FET2  
are short-circuited.

Test Circuit 5  
RSS(on)

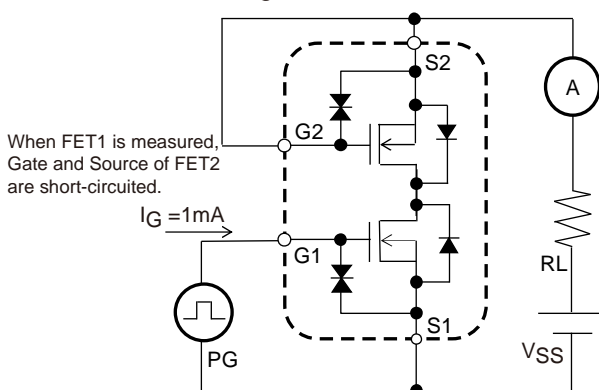


Test Circuit 6  
 $t_d(\text{on})$ ,  $t_r$ ,  $t_d(\text{off})$ ,  $t_f$



When FET1 is measured,  
Gate and Source of FET2  
are short-circuited.

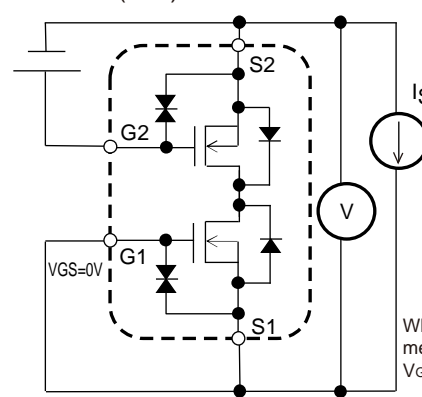
Test Circuit 7  
Qg



When FET1 is measured,  
Gate and Source of FET2  
are short-circuited.

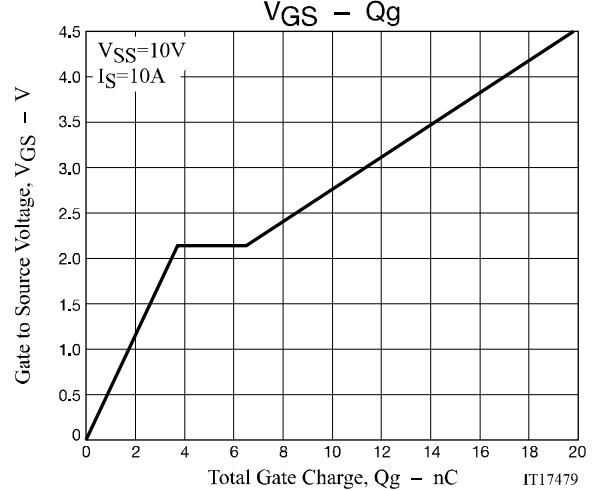
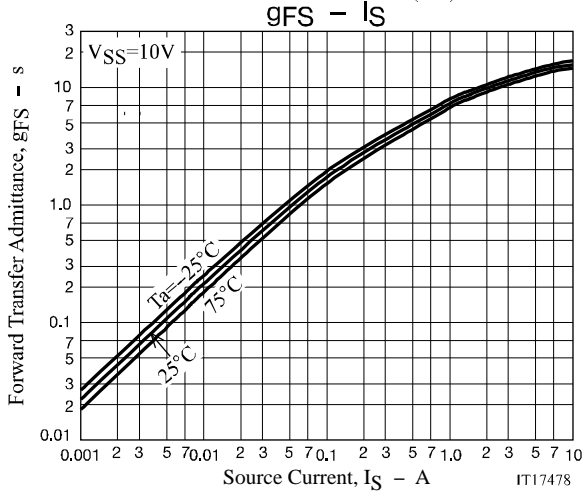
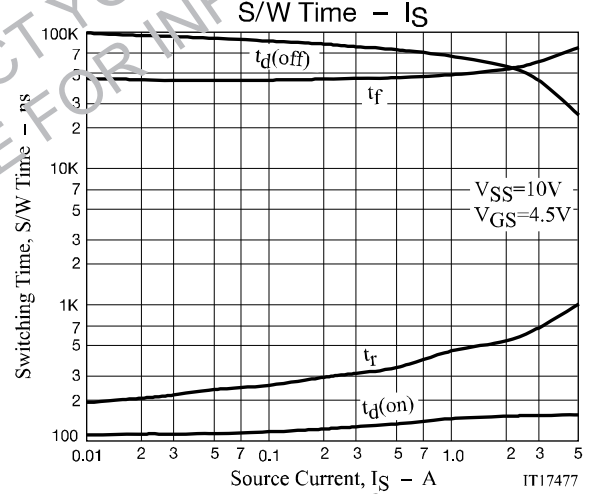
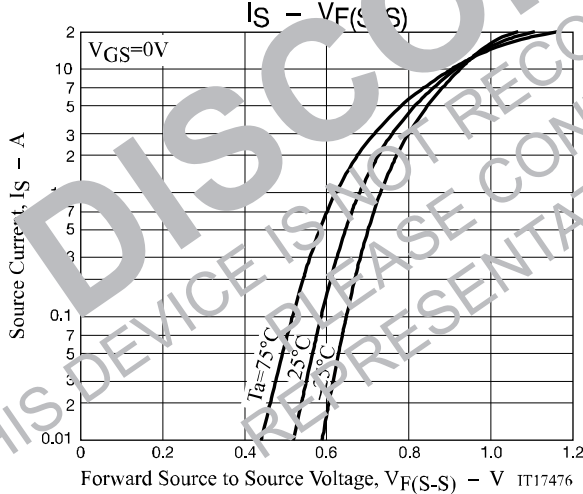
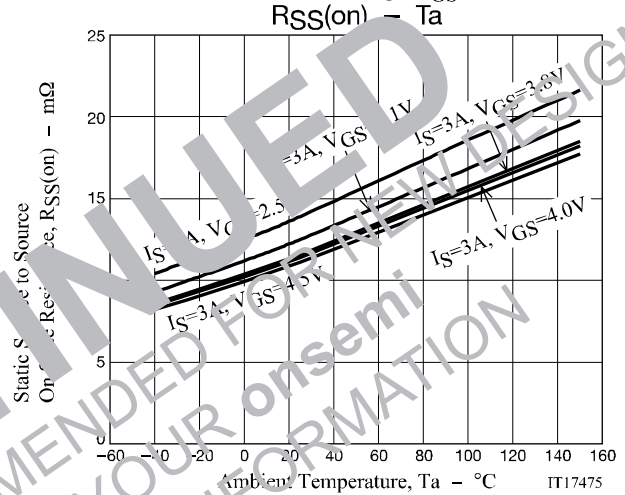
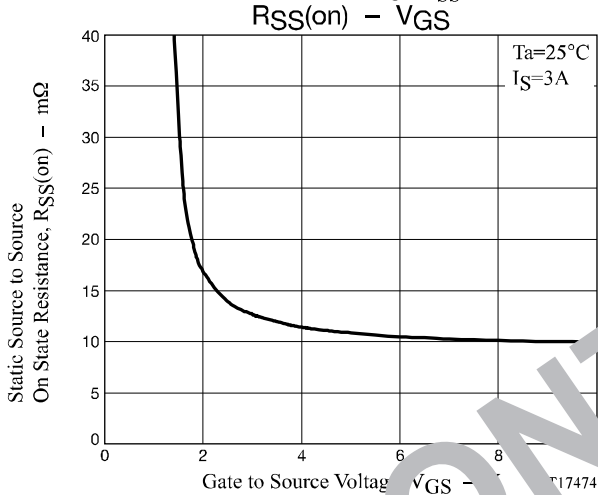
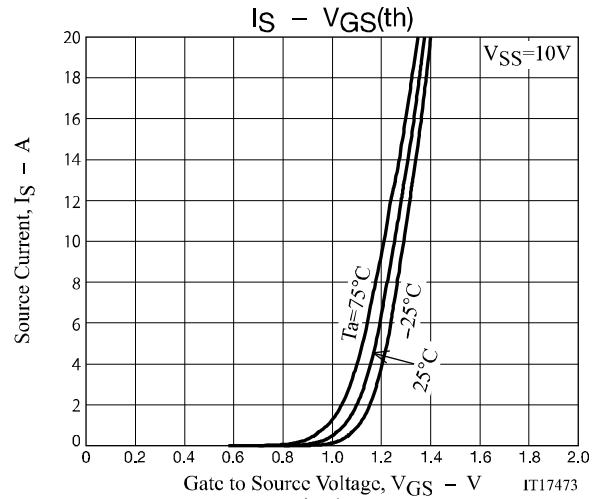
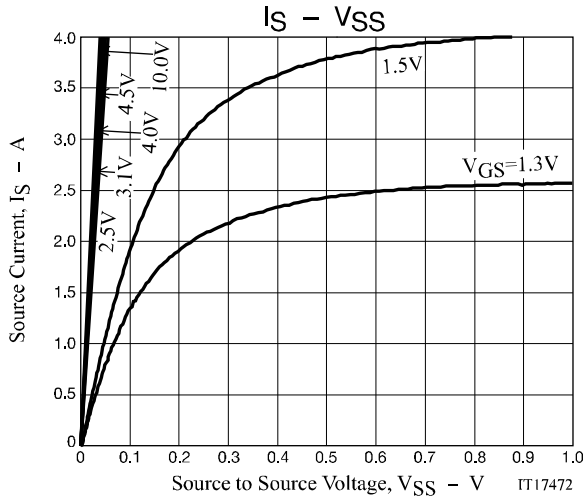
$I_G = 1\text{mA}$

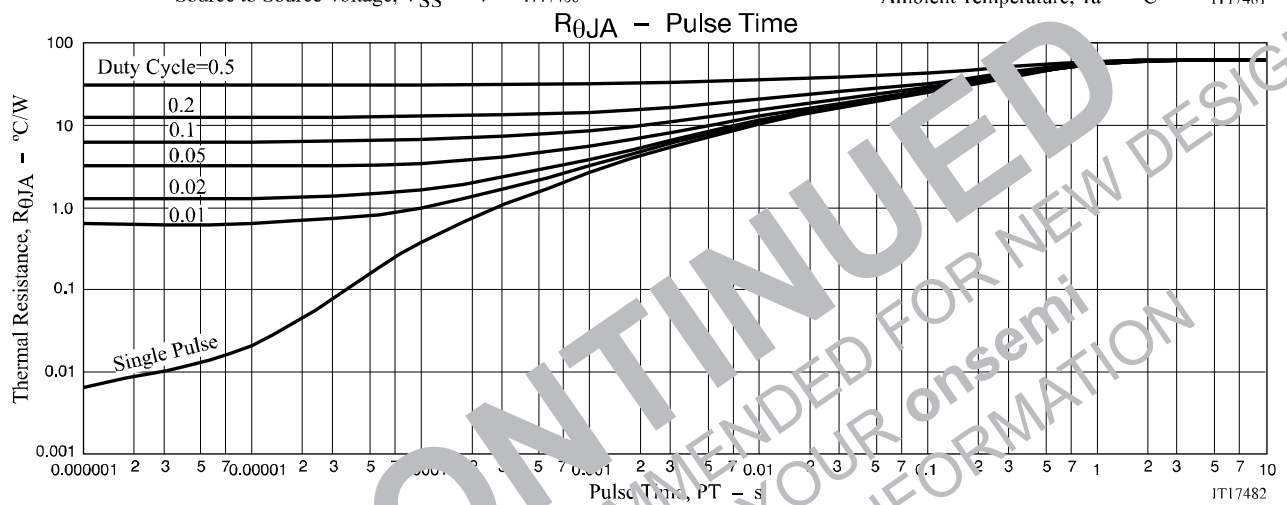
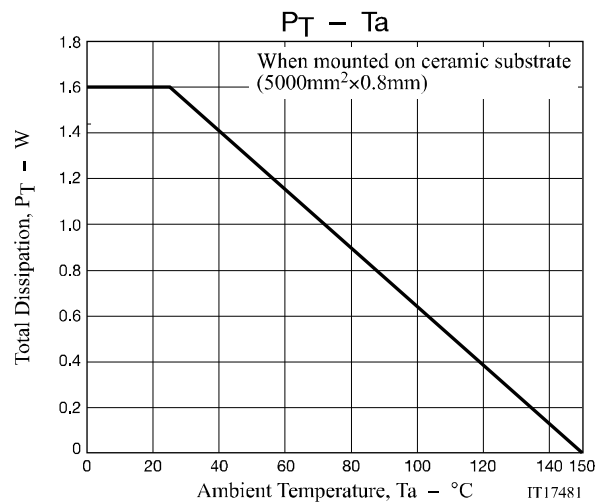
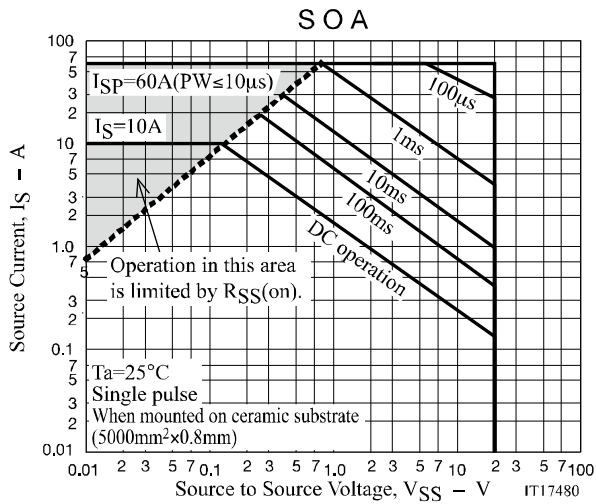
Test Circuit 8  
VF(S-S)



When FET1 is  
measured, +4.5V is added to  
Vgs of FET2.

When FET2 is measured, the position of FET1 and FET2 is switched.







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Authorized Distributor

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