

Dual NPN Bias Resistor Transistors

R1 = 1 kΩ, R2 = 1 kΩ

NPN Transistors with Monolithic Bias Resistor Network

MUN5230DW1, NSBC113EDXV6

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

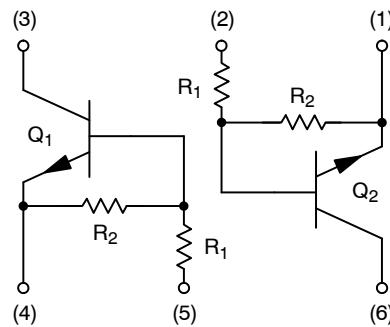
MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$, common for Q_1 and Q_2 , unless otherwise noted)

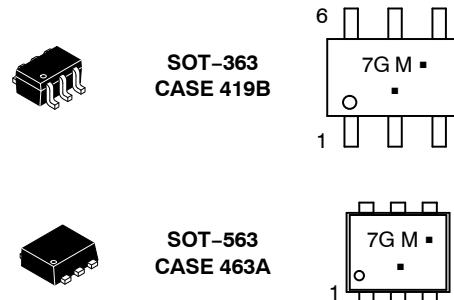
Rating	Symbol	Max	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current – Continuous	I_C	100	mAdc
Input Forward Voltage	$V_{IN(fwd)}$	10	Vdc
Input Reverse Voltage	$V_{IN(rev)}$	10	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PIN CONNECTIONS



MARKING DIAGRAMS



7G = Specific Device Code
M = Date Code*
□ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

See detailed ordering, marking, and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been DISCONTINUED. Please refer to the table on page 2.

MUN5230DW1, NSBC113EDXV6

ORDERING INFORMATION

Device	Package	Shipping [†]
MUN5230DW1T1G, SMUN5230DW1T1G	SOT-363	3,000 / Tape & Reel

DISCONTINUED (Note 1)

NSBC113EDXV6T1G	SOT-563	4,000 / Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
MUN5230DW1 (SOT-363) ONE JUNCTION HEATED			
Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 2) (Note 3)	P_D	187 256 1.5 2.0	mW mW/ $^\circ\text{C}$
Derate above 25°C (Note 2) (Note 3)			
Thermal Resistance, Junction to Ambient (Note 2) (Note 3)	$R_{\theta JA}$	670 490	$^\circ\text{C}/\text{W}$

NSBC113EDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 4)

Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 2) (Note 3)	P_D	250 385 2.0 3.0	mW mW/ $^\circ\text{C}$
Derate above 25°C (Note 2) (Note 3)			
Thermal Resistance, Junction to Ambient (Note 2) (Note 3)	$R_{\theta JA}$	493 325	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Lead (Note 2) (Note 3)	$R_{\theta JL}$	188 208	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

NSBC113EDXV6 (SOT-563) ONE JUNCTION HEATED

Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 2) Derate above 25°C (Note 2)	P_D	357 2.9	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 2)	$R_{\theta JA}$	350	$^\circ\text{C}/\text{W}$

NSBC113EDXV6 (SOT-563) BOTH JUNCTION HEATED (Note 4)

Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 2) Derate above 25°C (Note 2)	P_D	500 4.0	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient (Note 2)	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

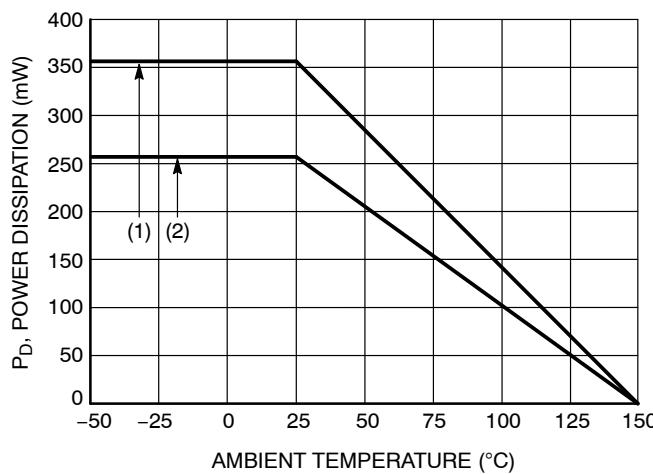
2. FR-4 @ Minimum Pad.
3. FR-4 @ 1.0×1.0 Inch Pad.
4. Both junction heated values assume total power is sum of two equally powered channels.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, common for Q_1 and Q_2 , unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current ($V_{CB} = 50\text{ V}$, $I_E = 0$)	I_{CBO}	—	—	100	nAdc
Collector-Emitter Cutoff Current ($V_{CE} = 50\text{ V}$, $I_B = 0$)	I_{CEO}	—	—	500	nAdc
Emitter-Base Cutoff Current ($V_{EB} = 6.0\text{ V}$, $I_C = 0$)	I_{EBO}	—	—	4.3	mAdc
Collector-Base Breakdown Voltage ($I_C = 10\text{ }\mu\text{A}$, $I_E = 0$)	$V_{(BR)CBO}$	50	—	—	Vdc
Collector-Emitter Breakdown Voltage (Note 5) ($I_C = 2.0\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	50	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 5) ($I_C = 5.0\text{ mA}$, $V_{CE} = 10\text{ V}$)	h_{FE}	3.0	5.0	—	
Collector-Emitter Saturation Voltage (Note 5) ($I_C = 10\text{ mA}$, $I_B = 5.0\text{ mA}$)	$V_{CE(\text{sat})}$	—	—	0.25	V
Input Voltage (Off) ($V_{CE} = 5.0\text{ V}$, $I_C = 100\text{ }\mu\text{A}$)	$V_{i(\text{off})}$	—	1.2	—	Vdc
Input Voltage (On) ($V_{CE} = 0.2\text{ V}$, $I_C = 20\text{ mA}$)	$V_{i(\text{on})}$	—	1.7	—	Vdc
Output Voltage (On) ($V_{CC} = 5.0\text{ V}$, $V_B = 2.5\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OL}	—	—	0.2	Vdc
Output Voltage (Off) ($V_{CC} = 5.0\text{ V}$, $V_B = 0.05\text{ V}$, $R_L = 1.0\text{ k}\Omega$)	V_{OH}	4.9	—	—	Vdc
Input Resistor	R_1	0.7	1.0	1.3	k Ω
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle $\leq 2\%$.



(1) SOT-363; 1.0 x 1.0 Inch Pad
(2) SOT-563; Minimum Pad

Figure 1. Derating Curve

MUN5230DW1, NSBC113EDXV6

TYPICAL CHARACTERISTICS MUN5230DW1, NSBC113EDXV6

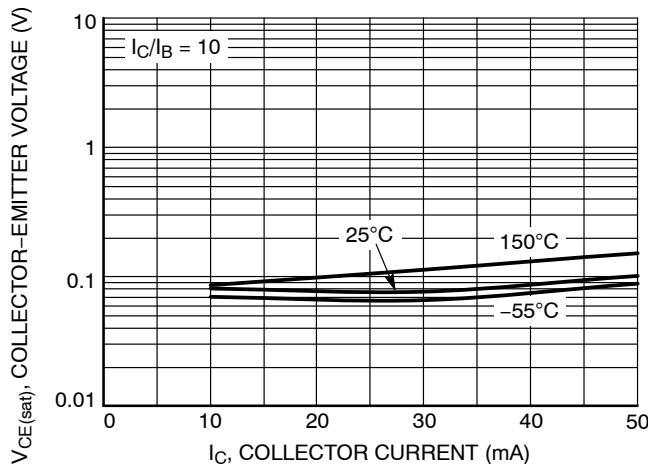


Figure 2. $V_{CE(sat)}$ vs. I_C

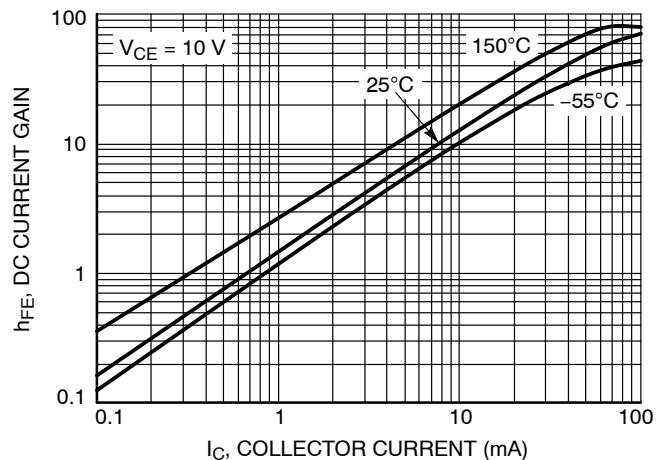


Figure 3. DC Current Gain

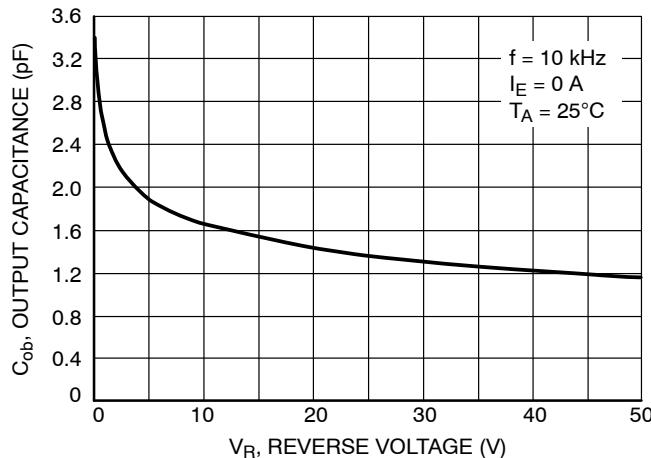


Figure 4. Output Capacitance

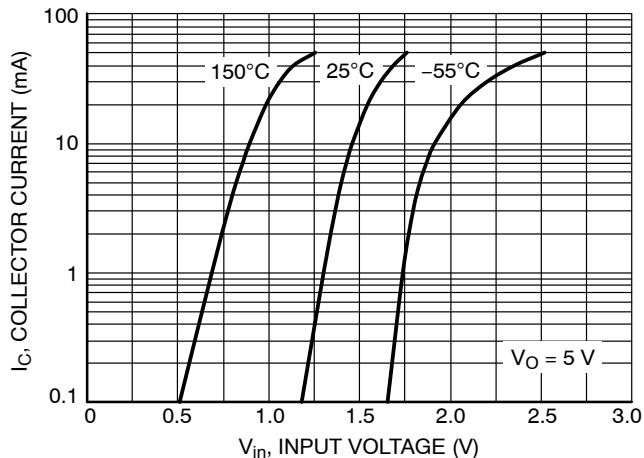


Figure 5. Output Current vs. Input Voltage

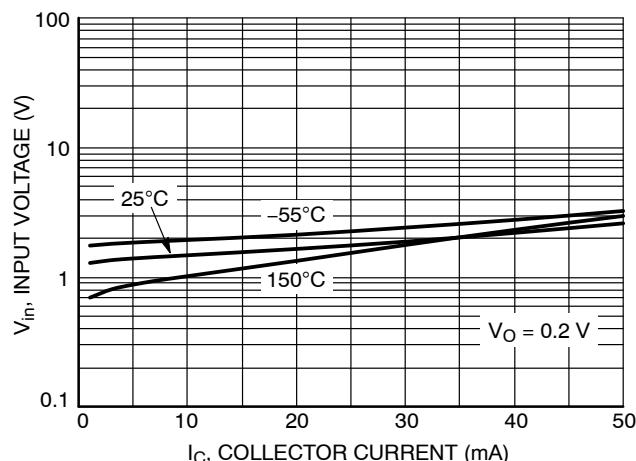


Figure 6. Input Voltage vs. Output Current

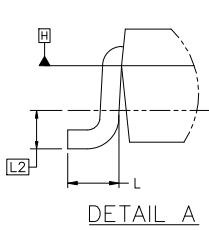
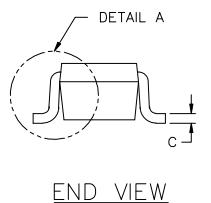
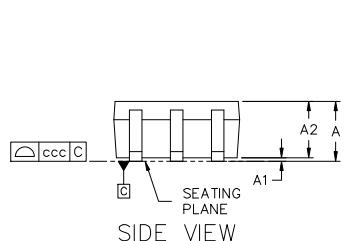
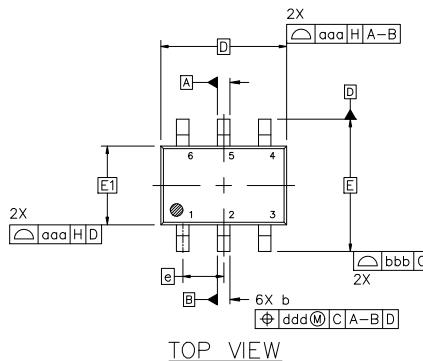


SC-88 2.00x1.25x0.90, 0.65P
CASE 419B-02
ISSUE Z

DATE 18 APR 2024

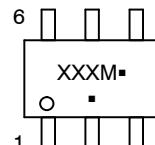
NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUM A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00	BSC	
E	2.10	BSC	
E1	1.25	BSC	
e	0.65	BSC	
L	0.26	0.36	0.46
L2	0.15	BSC	
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

XXX = Specific Dev.

■ = Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL. SOI DFRM/PD.

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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CASE 419B-02
ISSUE Z

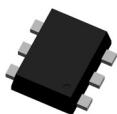
DATE 18 APR 2024

STYLE 1: PIN 1. Emitter 2 2. Base 2 3. Collector 1 4. Emitter 1 5. Base 1 6. Collector 2	STYLE 2: Cancelled	STYLE 3: Cancelled	STYLE 4: PIN 1. Cathode 2. Cathode 3. Collector 4. Emitter 5. Base 6. Anode	STYLE 5: PIN 1. Anode 2. Anode 3. Collector 4. Emitter 5. Base 6. Cathode	STYLE 6: PIN 1. Anode 2 2. N/C 3. Cathode 1 4. Anode 1 5. N/C 6. Cathode 2
STYLE 7: PIN 1. Source 2 2. Drain 2 3. Gate 1 4. Source 1 5. Drain 1 6. Gate 2	STYLE 8: Cancelled	STYLE 9: PIN 1. Emitter 2 2. Emitter 1 3. Collector 1 4. Base 1 5. Base 2 6. Collector 2	STYLE 10: PIN 1. Source 2 2. Source 1 3. Collector 1 4. Drain 1 5. Drain 2 6. Gate 2	STYLE 11: PIN 1. Cathode 2 2. Cathode 2 3. Anode 1 4. Cathode 1 5. Cathode 1 6. Anode 2	STYLE 12: PIN 1. Anode 2 2. Anode 2 3. Cathode 1 4. Anode 1 5. Anode 1 6. Cathode 2
STYLE 13: PIN 1. Anode 2. N/C 3. Collector 4. Emitter 5. Base 6. Cathode	STYLE 14: PIN 1. Vref 2. GND 3. GND 4. Iout 5. Ven 6. Vcc	STYLE 15: PIN 1. Anode 1 2. Anode 2 3. Anode 3 4. Cathode 3 5. Cathode 2 6. Cathode 1	STYLE 16: PIN 1. Base 1 2. Emitter 2 3. Collector 2 4. Base 2 5. Emitter 1 6. Collector 1	STYLE 17: PIN 1. Base 1 2. Emitter 1 3. Collector 2 4. Base 2 5. Emitter 2 6. Collector 1	STYLE 18: PIN 1. Vin1 2. Vcc 3. Vout2 4. Vin2 5. Gnd 6. Vout1
STYLE 19: PIN 1. Iout 2. Gnd 3. Gnd 4. Vcc 5. Ven 6. Vref	STYLE 20: PIN 1. Collector 2. Collector 3. Base 4. Emitter 5. Collector 6. Collector	STYLE 21: PIN 1. Anode 1 2. N/C 3. Anode 2 4. Cathode 2 5. N/C 6. Cathode 1	STYLE 22: PIN 1. D1 (l) 2. Gnd 3. D2 (l) 4. D2 (c) 5. Vbus 6. D1 (c)	STYLE 23: PIN 1. Vn 2. Ch1 3. Vp 4. N/C 5. Ch2 6. N/C	STYLE 24: PIN 1. Cathode 2. Anode 3. Cathode 4. Cathode 5. Cathode 6. Cathode
STYLE 25: PIN 1. Base 1 2. Cathode 3. Collector 2 4. Base 2 5. Emitter 6. Collector 1	STYLE 26: PIN 1. Source 1 2. Gate 1 3. Drain 2 4. Source 2 5. Gate 2 6. Drain 1	STYLE 27: PIN 1. Base 2 2. Base 1 3. Collector 1 4. Emitter 1 5. Emitter 2 6. Collector 2	STYLE 28: PIN 1. Drain 2. Drain 3. Gate 4. Source 5. Drain 6. Drain	STYLE 29: PIN 1. Anode 2. Anode 3. Collector 4. Emitter 5. Base/Anode 6. Cathode	STYLE 30: PIN 1. Source 1 2. Drain 2 3. Drain 2 4. Source 2 5. Gate 1 6. Drain 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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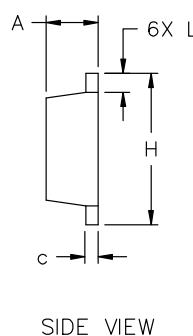
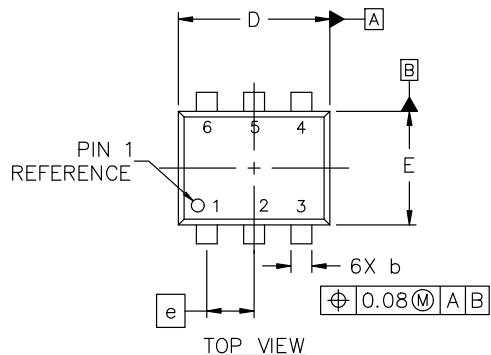
SOT-563-6 1.60x1.20x0.55, 0.50P

CASE 463A
ISSUE J

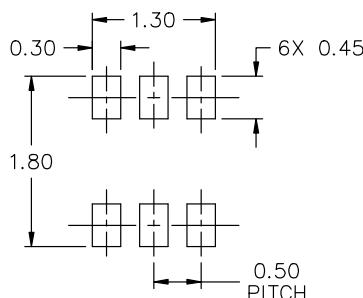
DATE 15 FEB 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e 0.50 BSC			
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

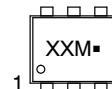
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2. Base 1	2. Emitter 2	2. Cathode 1
3. Collector 2	3. Base 2	3. Anode/Anode 2
4. Emitter 2	4. Collector 2	4. Cathode 2
5. Base 2	5. Base 1	5. Cathode 2
6. Collector 1	6. Collector 1	6. Anode/Anode 1

STYLE 4: PIN 1. Collector	STYLE 5: PIN 1. Cathode	STYLE 6: PIN 1. Cathode
2. Collector	2. Cathode	2. Anode
3. Base	3. Anode	3. Cathode
4. Emitter	4. Anode	4. Cathode
5. Collector	5. Cathode	5. Cathode
6. Collector	6. Cathode	6. Cathode

STYLE 7: PIN 1. Cathode	STYLE 8: PIN 1. Drain	STYLE 9: PIN 1. Source 1
2. Anode	2. Drain	2. Gate 1
3. Cathode	3. Gate	3. Drain 2
4. Cathode	4. Source	4. Source 2
5. Anode	5. Drain	5. Gate 2
6. Cathode	6. Drain	6. Drain 1

STYLE 10: PIN 1. Cathode 1	STYLE 11: PIN 1. Emitter 2
2. N/C	2. Base 2
3. Cathode 2	3. Collector 1
4. Anode 2	4. Emitter 1
5. N/C	5. Base 1
6. Anode 1	6. Collector 2

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XX = Specific Device Code

M = Month Code

■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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