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BELASIGNA 250

High-Performance Programmable Audio Processing System

Introduction

BELASIGNA® 250 is a complete programmable audio processing system, designed specifically for ultra−low−power embedded and portable digital audio systems. This high−performance chip builds on the architecture and design of BELASIGNA 200 to deliver exceptional sound quality along with unmatched flexibility.

BELASIGNA 250 incorporates a full audio signal chain, from stereo 16−bit A/D converters or digital interfaces to accept the signal, through the fully flexible digital processing architecture, to stereo analog line−level or direct digital power outputs that can connect directly to speakers.

BELASIGNA 250 features flexible clocking options and smart power management features including a soft power−down mode. Two DSP subsystems operate concurrently: the RCore, which is a fully software programmable DSP core, and the weighted overlap−add (WOLA) filterbank coprocessor, which is a dedicated, configurable processor that executes time−frequency domain transforms and other vector− based computations. A full range of other hardware−assisted features, such as audio−targeted DMA complete the system.

A comprehensive and easy−to−use suite of development tools, hands−on training and full technical support are available to enable rapid development and introduction of highly differentiated products in record time.

Key Features

- **Unique Parallel−processing Architecture:** A Complete DSP−based, Mixed−signal Audio System Consisting of a 16−bit Fully Programmable Dual−Harvard 16−bit DSP Core, a Patented, High−resolution Block Floating−point WOLA Filterbank Coprocessor, and an Input/Output Processor (IOP) along with Several Peripherals and Interfaces which Optimize the Architecture for Audio Processing
- **Integrated Converters and Powered Output:** Minimize Need for External Components
- **Ultra−low Power Consumption:** Under 5 mA at 20 MHz to Support Advanced Operations; 1.8 V Supply Voltage
- **“Smart” Power Management:** Including Low Current Standby Mode Requiring Only 0.05 mA
- **Flexible Clocking Architecture:** Supports Speeds up to 50 MHz
- **Full Range of Configurable Interfaces:** Including: I^2S, PCM, UART, SPI, I^2C, TWSS, GPIO
- **Excellent Fidelity:** 88 dB System Dynamic Range, Exceptionally Low System Noise and Low Group Delay
- **Support for IP Protection:** to Prevent Unauthorized Access to Algorithms and Data
- These Devices are Pb−Free, BFR Free and are RoHS Compliant

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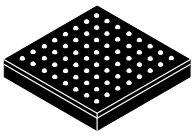


LFBGA−64
7x7
CASE 566AF

MARKING DIAGRAM

0W888−002 = Device Code
XXXX = Date Code
Y = Assembly Plant Identifier
ZZ = Traceability Code
AAAA = Country of Assembly

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 23 of this data sheet.

Figures and Data

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Voltage at any input pin	−0.3	2.2	V
Operating supply voltage (Note 1)	0.9	2.0	V
Operating temperature range (Note 2)	−40	85	°C
Storage temperature range	−40	125	°C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V)			

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Below 1.05 V audio performance will be degraded.
2. Parameters may exceed listed tolerances when out of the temperature range 0 to 50°C.

Electrical Performance Specifications

The parameters in Table 2 do not vary with WOLA filterbank configuration. The tests were performed at 20°C with a clean 1.8 V supply voltage. BELASIGNA 250 was running in high voltage mode (VDDC = 1.8 V). The system clock (SYS_CLK) was set to 5.12 MHz and a sampling frequency of 16 kHz was used with MCLK was set to 1.28 MHz.

Parameters marked as screened are tested on each chip. Other parameters are qualified but not tested on every part.

Table 2. ELECTRICAL SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
OVERALL							
Supply voltage	V_{BAT}		0.9 (Note 3)	1.8	2.0	V	
Current consumption	I_{BAT}	SYS_CLK = 1.28 MHz, sample rate = 16 kHz	−	650	−	μA	
		5.12 MHz, 16 kHz	−	1	−	mA	
		19.2 MHz, 16 kHz	−	5	−	mA	
		49.152 MHz, 16 kHz	−	10	−	mA	
		49.152 MHz, 48 kHz	−	13	−	mA	
VREG (1 μF External Capacitor)							
Regulated voltage output	V_{REG}		0.95	1.00	1.05	V	√
Regulator PSRR	V_{REG_PSRR}	1 kHz	50	55		dB	
Load current	I_{LOAD}		−	−	2	mA	
Load regulation	$LOAD_{REG}$		−	11	20	mV/mA	
Line regulation	$LINE_{REG}$		−	2	5	mV/V	
VDBL (1 μF External Capacitor)							
Regulated doubled voltage output	VDBL		1.9	2.0	2.1	V	√
Regulator PSRR	$VDBL_{PSRR}$	1 kHz	45	50		dB	
Load current	I_{LOAD}		−	−	2	mA	
Load regulation	$LOAD_{REG}$		−	120	200	mV/mA	√
Line regulation	$LINE_{REG}$		−	5	10	mV/V	
VDDC (1 μF External Capacitor)							
Digital supply voltage output	VDDC	LV mode (VREG)	0.9	1.0	1.1	V	√
		DV mode (VDBL)	1.8	2.0	2.2	V	√

3. Audio performance will be degraded below 1.05 V.
4. Measured with a = 12 dB input signal.
5. Input stage delay is inversely proportional to sampling frequency.
6. Max voltage should be limited to 2.2 V peak regardless of VDDC. Protection diodes will be enabled above this voltage.

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
VDDC (1 μF External Capacitor)							
Regulator PSRR	$VDDC_{PSRR}$	LV mode; 1 kHz	20	28	–	dB	
		DV mode; 1 kHz	40	48	–	dB	
Load current	I_{LOAD}	All modes	–	–	3.5	mA	
VDDC (1 μF External Capacitor)							
Load regulation	$LOAD_{REG}$	LV mode	–	5	10	mV/mA	√
		DV mode	–	150	250	mV/mA	√
Line regulation	$LINE_{REG}$	LV mode	–	1.5	10	mV/V	
		DV mode	–	5	10	mV/V	
POWER−ON−RESET (POR)							
POR startup voltage	$VDDC_{STARTUP}$		0.78	0.83	0.88	V	
POR shutdown voltage	$VDDC_{SHUTDOWN}$		0.76	0.81	0.86	V	
POR hysteresis	$POR_{HYSTERESIS}$		10	16	22	mV	
POR duration	T_{POR}		5	10	15	ms	
INPUT STAGE							
Analog input voltage	V_{IN}		0	–	2	V	
Preamplifier gain tolerance	PAG	1 kHz	−1.5	–	1.5	dB	√
Preamplifier gain mismatch between channels		1 kHz	−1	–	1	dB	
Input impedance	R_{IN}	0 dB preamplifer gain	–	250	–	kΩ	
		Non−zero preamplifier gains	400	550	700	kΩ	√
Input referred noise	IN_{IRN}	Unweighted, 20 Hz to 8 kHz BW				μVrms	
		Preamplifier setting:					
		0 dB	–	40	55		
		12 dB	–	12	14		
		15 dB	–	8	11		
		18 dB	–	6	8		
		21 dB	–	4.5	5.5		
		24 dB	–	4	5		
		27 dB	–	3.5	4.5		
		30 dB	–	3	4		
Input dynamic range	IN_{DR}	1 kHz, 20 Hz to 8 kHz BW				dB	
		Preamplifier setting:					
		0 dB	85	88	–		
		12 dB	84	87	–		
		15 dB	84	87	–		
		18 dB	83	86	–		
		21 dB	82	85	–		
		24 dB	81	84	–		
		27 dB	80	83	–		
		30 dB	78	81	–		
Input peak THD+N (Note 4)	IN_{THDN}	Any valid preamplifier gain, 1 kHz	–	−63	−60	dB	√
Input stage delay (Note 5)			–	200	–	μs	

3. Audio performance will be degraded below 1.05 V.
4. Measured with a = 12 dB input signal.
5. Input stage delay is inversely proportional to sampling frequency.
6. Max voltage should be limited to 2.2 V peak regardless of VDDC. Protection diodes will be enabled above this voltage.

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
DIRECT DIGITAL OUTPUT							
Maximum load current	I_{DO}	Normal mode	−	−	13	mA	
		High power mode	−	−	25	mA	
Output impedance	R_{DO}	Normal mode	−	9	11	Ω	
		High power mode	−	5	6	Ω	
Output dynamic range	DO_{DR}	Unweighted, 100 Hz to 8 kHz BW, mono	90	93	−	dB	
Output THD+N	DO_{THDN}	Unweighted, 100 Hz to 22 kHz BW, mono		−79	−76	dB	
Output voltage	DO_{VOUT}		−Vbat		Vbat	V	
ANALOG OUTPUT STAGE							
Analog output voltage	V_{OUT}		0	−	2	V	
Attenuator gain tolerance	ATG	Input is –6 dB re: full scale @ 1 kHz (all preamplifier gains)	−1	−	1	dB	√
Output impedance	R_{OUT}	Attenuator settings: 0 dB 12 dB 15 dB 18 dB 21 dB 24 dB 27 dB 30 dB	 1 9 7 4 3 2 1 1	 2 13 10 8 6 4 3 2	 5 17 14 12 9 7 6 5	kΩ	√
Output noise	OUT_N	0 dB attenuation	−	33	40	μV	
Output dynamic range	OUT_{DR}	Unweighted, 100 Hz to 8 kHz BW, mono	85	87	−	dB	
Output THD+N	OUT_{THDN}	Unweighted, 100 Hz to 22 kHz BW, mono	−	−70	−67	dB	
ANTI−ALIASING FILTERS (Input and Output)							
Preamplifier filter cut−off frequency		Preamp not bypassed	−	25	−	kHz	
Digital anti−aliasing filter cut−off frequency			−	$f_S/2$	−		
Analog output cut−off frequency		25 kHz	15	25	35	kHz	
		12 kHz (only output filter)	9	12	15	kHz	
Passband flatness			−1	−	1	dB	
Stopband attenuation		60 kHz (12 kHz cut−off)	−	60	−	dB	
LOW−SPEED A/D							
Input voltage		Peak input voltage	0	−	2.0	V	√
INL		From GND to 2*VREG	−	−	10	LSB	
DNL		From GND to 2*VREG	−	−	2	LSB	
Maximum variation over temperature (0°C to 50°C)			−	−	5	LSB	
Sampling frequency		All channels sequentially	−	12.8	−	kHz	
Channel sampling frequency		8 channels	−	1.6	−	kHz	

3. Audio performance will be degraded below 1.05 V.
4. Measured with a = 12 dB input signal.
5. Input stage delay is inversely proportional to sampling frequency.
6. Max voltage should be limited to 2.2 V peak regardless of VDDC. Protection diodes will be enabled above this voltage.

Table 2. ELECTRICAL SPECIFICATIONS (continued)

Description	Symbol	Conditions	Min	Typ	Max	Units	Screened
DIGITAL PADS							
Voltage level for high input	V_{IH}		VDDC * 0.8	−	VDDC + 0.5 (Note 6)	V	
Voltage level for low input	V_{IL}		−0.3	−	VDDC * 0.2	V	
Input capacitance for digital pads	C_{IN}		−	2	−	pF	
Pull−up resistance for digital input pads	R_{UP_IN}		−	260	−	kΩ	√
Pull−down resistance to VDDC for digital input pads	R_{DOWN_IN}	VDDC = 1.0 V	−	430	−	kΩ	
		VDDC = 1.25 V	−	260	−	kΩ	√
		VDDC = 2.0 V	−	140	−	kΩ	
Pull−up resistance for digital input pads	R_{UP_IN}		−	260	−	kΩ	√
Rise and fall time	Tr, Tf	Digital output pad	−	−	100	ns	
ESD		Human Body Model	2	−	−	kV	
Latch−up		V < GNDO, V > VDDO	200	−	−	mA	
OSCILLATION CIRCUITRY							
Internal oscillator frequency	SYS_CLK		0.5	−	10.24	MHz	
Calibrated clock frequency	SYS_CLK		−1	±0	+1	%	√
Internal oscillator jitter		System clock: 1.28 MHz	−	0.4	1	ns	
External oscillator tolerances		Duty cycle	45	50	55	%	
		System clock: 50 MHz	−	−	300	ps	
Maximum working frequency	CLK_{MAX}	External clock; VBAT: 1.25 V	−	−	10	MHz	
		External clock; VBAT: 1.8 V	−	−	50	MHz	
IR INTERFACE							
Carrier frequency			39	40	41	kHz	
Data rate			1150	1200	1250	bit/s	
Input current			0.1	−	15	μA	
DIGITAL INTERFACES							
TWSS baud rate		PCLK ≤ 1.92 MHz	−	−	100	kbps	
		PCLK > 1.92 MHz	−	−	400	kbps	
General−purpose UART baud rate		PCLK = 3.81 MHz	−	−	762	kbps	
		PCLK = 7.62 MHz	−	−	1.524	Mbps	
Debug port baud rate			−	−	115.2	kbps	

3. Audio performance will be degraded below 1.05 V.
4. Measured with a = 12 dB input signal.
5. Input stage delay is inversely proportional to sampling frequency.
6. Max voltage should be limited to 2.2 V peak regardless of VDDC. Protection diodes will be enabled above this voltage.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Mechanical Information and Circuit Design Guidelines

A total of 51 active pins are present on BELASIGNA 250. This package contains a total of 64 balls, organized in an 8−by−8 array. A description of these pins is given in Table 3.

Table 3. LFBGA PIN DESCRIPTIONS

Pad Index	BELASIGNA 250 Pin Name	Description	I/O	A/D
F2	VBAT	Power supply	I	A
B3, E2	AGND	Analog ground	N/A	A
E4	RCVRBAT	Digital output power supply	I	A
H4	RCVRGND	Digital output ground	N/A	A
D6	VDDC	Digital core power supply	O	D
F7	GNDC	Digital core ground	N/A	D
H6, C5	VDDO	Digital pads power supply	I	D
A6, F6	GNDO	Digital pads ground	N/A	D
E1	VREG	Microphone power supply	O	A
A1	VDBL	Doubled voltage output	O	A
B2	CAP0	Charge pump capacitor connection	N/A	A
A2	CAP1	Charge pump capacitor connection	N/A	A
B1	AI0	Microphone input	I	A
C1	AI1/LOUT	Microphone input / direct audio input	I	A
C2	AI2	Microphone input	I	A
D1	AI3	Microphone input	I	A
F1	AI_RC	Remote control input	I	A
D3	AIR	Audio input reference	N/A	A
G3	RCVR0+	Digital output 0 positive output	O	A
H3	RCVR0−	Digital output 0 negative output	O	A
H2	AO0/RCVR1+	Analog output 0 / digital output 1 positive output	O	A
H1	AO1/RCVR1−	Analog output 1 / digital output 1 negative output	O	A
F3	AOR	Analog output reference	N/A	A
H8	DEBUG_RX	RS−232 serial input	I	D
G8	DEBUG_TX	RS−232 serial output	O	D
H7	EXT_CLK	External clock input / output	I/O	D
C3	SPI_CLK	SPI clock	O	D
A3	SPI_CS	SPI chip select	O	D
B4	SPI_SERO	SPI serial output	O	D
A4	SPI_SERI	SPI serial input	I	D
E6	TWSS_CLK	Two−wire synchronous serial clock	I/O	D
F8	TWSS_DATA	Two−wire synchronous serial data	I/O	D
G5	GPIO[0] / I2S_FD	General−purpose input or output / I2S digital frame	I/O	D
H5	GPIO[1] / I2S_IND	General−purpose input or output / I2S digital input	I/O	D
G4	GPIO[2] / I2S_INA	General−purpose input or output / I2S analog input	I/O	D
F5	GPIO[3] / NCLK_DIV_RESET / I2S_FA	General−purpose input or output / I2S analog frame	I/O	D
B5	GPIO[4] / LSAD [0] / I2S_OUTD	General−purpose input or output / low−speed A/D input / I2S digital output	I/O	D/A
A5	GPIO[5] / LSAD[1] / I2S_OUTA	General−purpose input or output / low−speed A/D input / I2S analog output	I/O	D/A

Table 3. LFBGA PIN DESCRIPTIONS (continued)

Pad Index	BELASIGNA 250 Pin Name	Description	I/O	A/D
B6	GPIO[6] / LSAD[2]	General−purpose input or output / low−speed A/D input	I/O	D/A
A7	GPIO[7] / LSAD[3]	General−purpose input or output / low−speed A/D input	I/O	D/A
A8	GPIO[8] / LSAD[4] / UART_TX	General−purpose input or output / low−speed A/D input / UART output	I/O	D/A
B7	GPIO[9] / LSAD[5] / UART_RX	General−purpose input or output / low−speed A/D input / UART input	I/O	D/A
B8	GPIO[10] / UCLK	General−purpose input or output / user clock	I/O	D
C7	GPIO[11] / PCM_CLK	General−purpose input or output / PCM clock	I/O	D
C8	GPIO[12] / PCM_SERI	General−purpose input or output / PCM serial input	I/O	D
D7	GPIO[13] / PCM_SERO	General−purpose input or output / PCM serial output	I/O	D
D8	GPIO[14] / PCM_FRAME	General−purpose input or output / PCM frame	I/O	D
E7	GPIO[15]	General−purpose input or output	I/O	D

NOTE: Unlisted pads must be left unconnected.

Weight

BELASIGNA 250 has an average weight of 0.1275 grams.

Recommended Design Guidelines

BELASIGNA 250 is designed to allow both digital and analog processing in a single system. Due to the mixed−signal nature of this system, the careful design of the printed circuit board (PCB) layout is critical to maintain the high audio fidelity of BELASIGNA 250. To avoid coupling noise into the audio signal path, keep the digital traces away from the analog traces. To avoid electrical feedback coupling, isolate the input traces from the output traces.

Recommended Ground Design Strategy

The ground plane should be partitioned into two: the analog ground plane (AGND) and the digital ground plane (DGND). These two planes should be connected together at a single point, known as the star point. The star point should be located at the ground terminal of a capacitor on the output of the power regulator as illustrated in Figure 1.

The DGND plane is used as the ground return for digital circuits and should be placed under digital circuits. The AGND plane should be kept as noise−free as possible. It is used as the ground return for analog circuits and it should surround analog components and pins. It should not be connected to or placed under any noisy circuits such as RF chips, switching supplies or digital pads of BELASIGNA 250 itself. Analog ground returns associated with the audio output stage should connect back to the star point on separate individual traces.

For more information on the recommended ground design strategy, see Table 4 and Table 5.

In some designs, space constraints may make separate ground planes impractical. In this case a star configuration strategy should be used. Each analog ground return should connect to the star point with separate traces.

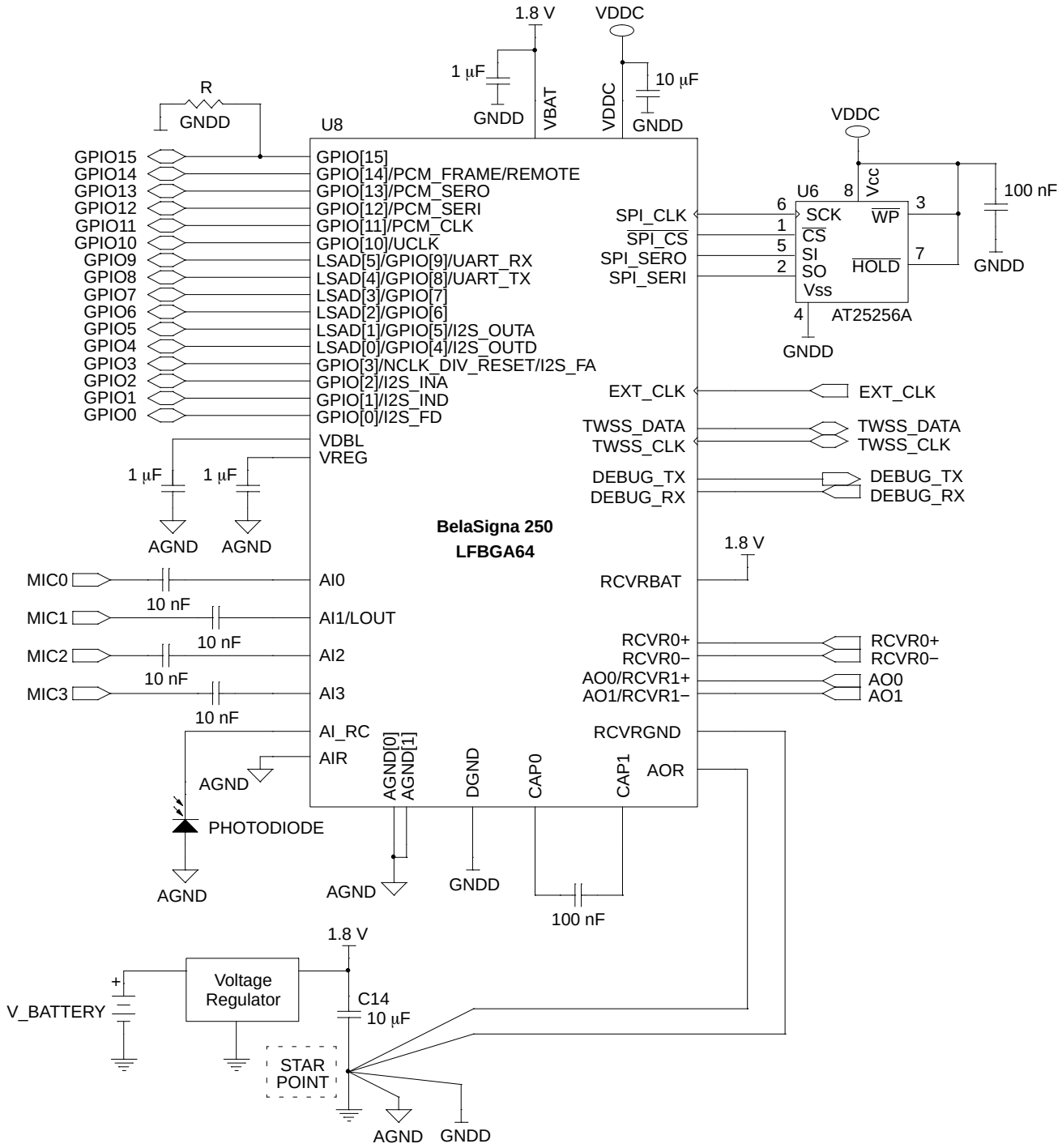


Figure 1. Schematic of Ground Scheme

Internal Power Supplies

Power management circuitry in BELASIGNA 250 generates separate digital (VDDC) and analog (VREG, VDBL) regulated supplies. Each supply requires an external decoupling capacitor, even if the supply is not used externally. Decoupling capacitors should be placed as close as possible to the power pads. Further details on these critical signals are provided in Table 4. Non−critical signals are outlined in Table 5.

Table 4. CRITICAL SIGNALS

Pin Name	Description	Routing Guideline
VBAT	Power supply	Place 1 μF (min) decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND plane.
VREG, VDBL	Internal regulator for analog sections	Place separate 1 μF decoupling capacitors close to each pin. Connect negative capacitor terminal to AGND. Keep away from digital traces and output traces. VREG may be used to generate microphone bias. VDBL shall not be used to supply external circuitry.
AGND	Analog ground return	Connect to AGND plane.
VDDO / VDDC	Internal regulator for digital sections (pads and core)	Place 10 μF decoupling capacitor close to pin. Connect negative terminal of capacitor to DGND.
GNDO / GNDC	Digital ground return (pads and core)	Connect to digital ground.
AI0, AI1 / LOUT, AI2, AI3	Microphone inputs	Keep as short as possible. Keep away from all digital traces and audio outputs. Avoid routing in parallel with other traces. Connect unused inputs to AGND.
AIR	Input stage reference voltage	Connect to AGND. If no analog ground plane, should share trace with microphone grounds to star point.
AO0, AO1	Analog audio output	Keep away from microphone inputs.
RCVR0+, RCVR0−, RCVR1+, RCVR1−	Direct digital audio output	Keep away from analog traces, particularly microphone inputs. Route corresponding traces as differential pair; route parallel to each other and approximately the same length.
AOR	Output stage reference voltage	Connect to star point. Share trace with power amplifier (if present).
RCVRGND	Output stage ground return	Connect to star point. Keep away from analog inputs.
EXT_CLK	External clock input / internal clock output	Minimize trace length. Keep away from analog signals. If possible, surround with digital ground.
AI_RC	Infrared receiver input	If used, minimize trace length to photodiode.

Table 5. NON−CRITICAL SIGNALS

Pin Name	Description	Routing Guideline
CAP0, CAP1	Internal charge pump − capacitor connection	Place 100 nF capacitor close to pins
DEBUG_TX, DEBUG_RX	Debug port	Not critical − Connect to test points
TWSS_SDA, TWSS_CLK	TWSS port	Not critical
GPIO[14..0]	General−purpose I/O	Not critical
GPIO[15]	General−purpose I/O Determines voltage mode during boot. For 1.8 V operation, should be connected to DGND.	Not critical
UART_RX, UART_TX	General−purpose UART	Not critical
PCM_FRAME, PCM_CLK, PCM_OUT, PCM_IN	Pulse code modulation port	Not critical − Keep away from analog signals.
I2S_INA, I2S_IND, I2S_FA, I2S_FD, I2S_OUTA, I2S_OUTD	I^2S compatible port	Not critical
UCLK	Programmable clock output	Not critical − If used, keep away from analog inputs/outputs
LSAD[5..0]	Low−speed A/D converters	Not critical
SPI_CLK, SPI_CS, SPI_SERI, SPI_SERO	Serial peripheral interface port Connect to EEPROM	Not critical

Audio Inputs

The audio input traces should be as short as possible. The input impedance of each audio input pad (e.g., AI0, AI1, etc.,) is high (approximately 500 kΩ); therefore a 10 nF capacitor is sufficient to decouple the DC bias. This capacitor and the internal resistance form a first−order analog high pass filter whose cutoff frequency can be calculated by f_{3dB} (Hz) = 1/(R x C x 2π), which results with ~30 Hz for 10 nF capacitor. This 10 nF capacitor value applies when the preamplifier is being used, in other words, when a non−unity gain is applied to the signals. When the preamplifier is by−passed, the impedance is reduced; hence, the cut−off frequency of the resulting high−pass filter could be too high. In such a case, the use of a 30−40 nF serial capacitor is recommended.

Keep audio input traces strictly away from output traces. Microphone ground terminals should be connected to the AGND plane (if present) or share a trace with the input ground reference voltage pin (AIR) to the star point. Analog and digital outputs MUST be kept away from microphone inputs to ensure low noise performance.

Audio Outputs

The audio output traces should be as short as possible. If the direct digital output is used, the trace length of RCVRx+ and RCVRx− should be approximately the same to provide matched impedances. If the analog audio output is used, the ground return for the external power amplifier should share a trace with the output ground reference voltage pin (AOR) to the star point.

Architecture Overview

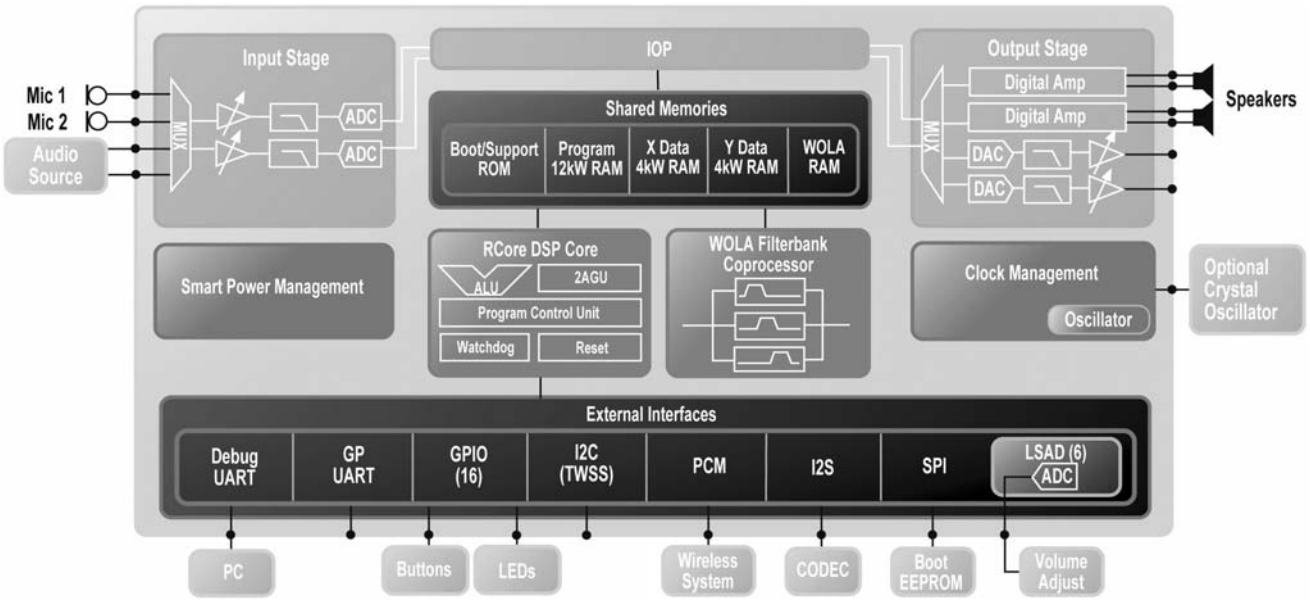


Figure 2. BELASIGNA 250 Architecture: A Complete Audio Processing System

RCore DSP

The RCore is a 16−bit fixed−point, dual−Harvard architecture DSP. It includes efficient normalize and de−normalize instructions, and support for double precision operations to provide the additional dynamic range needed for many applications. All memory locations in the system are accessible by the RCore using several addressing modes including indirect and circular modes. The RCore assumes master functionality of the system.

RCore DSP Architecture

Figure 3 illustrates the architecture of the RCore.

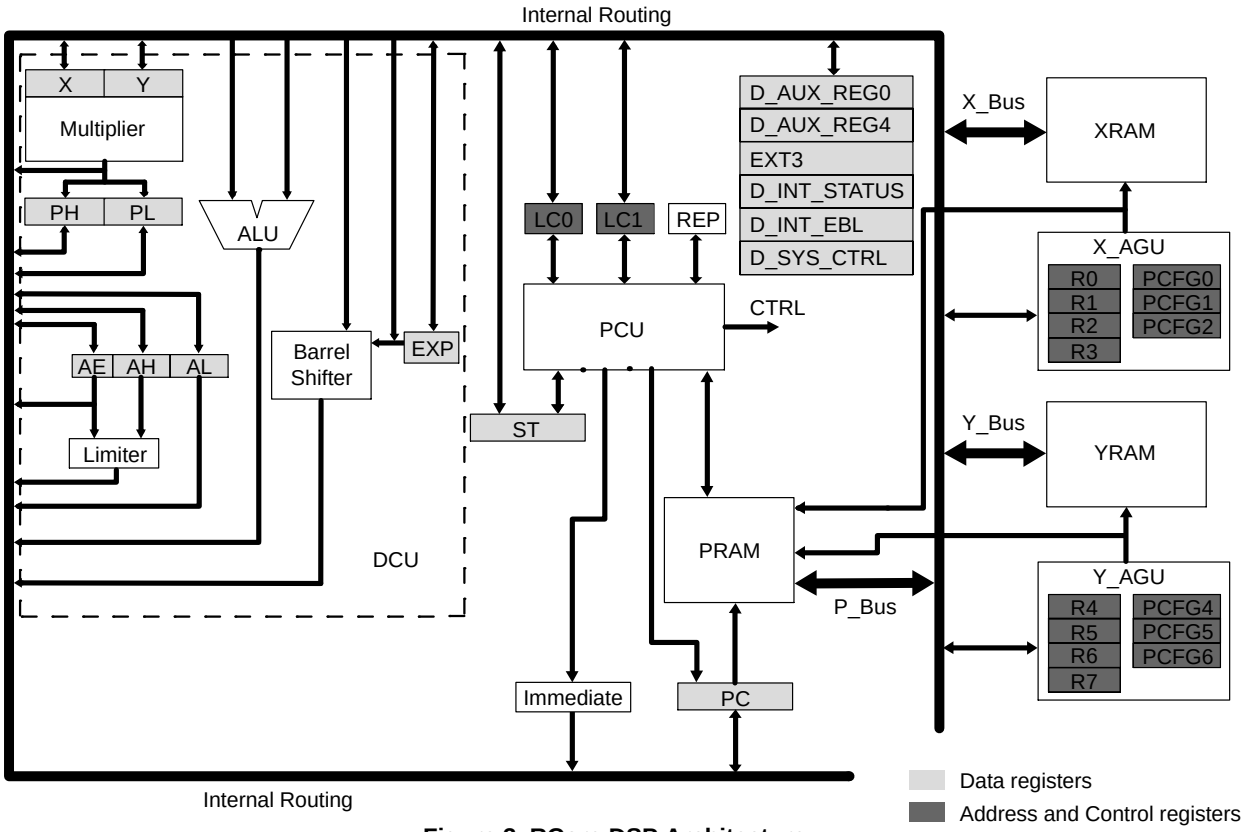


Figure 3. RCore DSP Architecture

The RCore is a single−cycle pipelined multiply−accumulate (MAC) architecture that feeds into a 40−bit accumulator complete with barrel shifter for fast normalization and de−normalization operations. Program execution is controlled by a sequencer that employs a three−stage pipeline (FETCH, DECODE, EXECUTE). Furthermore, the RCore incorporates pointer configuration registers for low cycle−count address generation when accessing the three memories: program memory (PRAM), X data memory (XRAM) and Y data memory (YRAM).

Instruction Set

The RCore instruction set can be divided into the following three classes:

1. Arithmetic and Logic Instructions

The RCore uses two's−complement fractional as a native data format. Thus, the range of valid numbers is [−1; 1), which is represented by 0x8000 to 0x7FFF. Other formats can be utilized by applying appropriate shifts to the data.

The multiplier takes 16−bit values and performs a multiplication every time an operand is loaded into either the X or Y registers. A number of instructions that allow loading of X and Y simultaneously and addition of the new product to the previous product (a MAC operation) are available. Single−cycle MAC with data pointer update and fetch is supported.

The arithmetic logic unit (ALU) receives its input from either the accumulator (AE|AH|AL) or the product register (PH|PL). Although the RCore is a 16−bit system, 32−bit additions or subtractions are also supported. Bit manipulation is also available on the accumulator, as are operations to perform arithmetic or logic shifting, toggling of specific bits, limiting, and other functions.

2. Data Movement Instructions

Data movement instructions transfer data between RAM, control registers and the RCore's internal registers (accumulator, PH, PL, etc.).

Two address generators are available to simultaneously generate two addresses in a single cycle. The address pointers R0..2 and R4..6 can be configured to support increment, decrement, add−by−offset, and two types of modulo−N circular buffer operations. Single−cycle access to low−X memory or low−Y memory as well as two−cycle instructions for immediate access to any address, are also available.

3. Program Flow Control Instructions

The RCore supports repeating of both single−word instructions and larger segments of code using dedicated repeat instructions or hardware loop counters. Furthermore, instructions to manipulate the program counter (PC) register such as calls to subroutines, conditional branches and unconditional branches are also provided.

The full instruction set may be seen in Table 6.

Table 6. INSTRUCTION SET

Instruction	Description
ABS A [,Cond] [,DW]	Calculate absolute value of A on condition
ADD A, Reg [,C]	Add register to A
ADD A, (Rij) [,C]	Add memory to A
ADD A, DRAM [,B]	Add (DRAM) to A
ADD A, (Rij)p [,C]	Add program memory to A
ADD A, Rc [,C]	Add Rc register to A
ADDI A, IMM [,C]	Add IMM to A
ADSI A, SIMM	Add signed SIMM to A
AND A, Reg	AND register with AH to AH
AND A, (Rij)	AND memory with AH to AH
AND A, DRAM [,B]	AND (DRAM) with AH to AH
AND A, (Rij)p	AND program memory with AH to AH
AND A, Rc	AND Rc register with AH to AH
ANDI A, IMM	AND IMM with AH to AH
ANSI A, SIMM	AND unsigned SIMM with AH to AH
BRA PRAM [,Cond]	Branch to new address on condition
BREAK	Stop the DSP for debugging purposes
CALL PRAM [,Cond] [,B]	Push PC and branch to new address on condition
CLB A	Calculate the leading bits on A
CLR A [,DW]	Clear accumulator
CLR Reg	Clear register
CMP A, Reg [,C]	Compare register to A
CMP A, (Rij) [,C]	Compare memory to A
CMP A, DRAM [,B]	Compare (DRAM) to A
CMP A, (Rij)p [,C]	Compare program memory to A
CMP A, Rc [,C]	Compare Rc register to A
CMPI A, IMM [,C]	Compare IMM to A
CMSI A, SIMM	Compare signed SIMM to A
CMPL A [,Cond] [,DW]	Calculate logical inverse of A on condition
DADD [Cond] [,P]	Add PH | PL to A, update PH | PL on condition
DBNZ0/1 PRAM	Branch to new address if LC0/1 <> 0
DCMP	Compare PH | PL to A
DEC A [,Cond] [,DW]	Decrement A on condition
DEC Reg [Cond]	Decrement register on condition
DEC (Rij) [,Cond]	Decrement memory on condition
DSUB [Cond] [,P]	Subtract PH | PL from A, update PH | PL on condition
EOR A, Reg	Exclusive−OR register with AH to AH
EOR A, (Rij)	Exclusive−OR memory with AH to AH
EOR A, DRAM [,B]	Exclusive−OR (DRAM) with AH to AH
EOR A, (Rij)p	Exclusive−OR program memory with AH to AH
EOR A, Rc	Exclusive−OR Rc register with AH to AH
EORI A, IMM	Exclusive−OR IMM with AH to AH
EOSI A, SIMM	Exclusive−OR unsigned SIMM with AH to AH
INC A [,Cond] [,DW]	Increment A on condition
INC Reg [,Cond]	Increment register on condition
INC (Rij) [,Cond]	Increment memory on condition
LD Rc, Rc	Load Rc register with Rc register
LD Reg, Reg	Load register with register
LD Reg, (Rij)	Load register with memory
LD (Rij), Reg	Load memory with register
LD (Ri), (Rj)	Transfer Y mem data to X mem
LD (Rj), (Ri)	Transfer X mem data to Y mem
LD A, DRAM [,B]	Load A with (DRAM)
LD DRAM, A [,B]	Load (DRAM) with A
LD Rc, (Rij)	Load Rc register with memory
LD (Rij), Rc	Load memory with Rc register
LD Reg, (Rij)p	Load register with program memory
LD (Rij)p, Reg	Load program memory with register
LD Reg, (Reg)p	Load register with program memory via register
LD Reg, Rc	Load register with Rc register
LD Rc, Reg	Load Rc register with register
LDI Reg, IMM	Load register with IMM
LDI Rc, IMM	Load Rc register with IMM
LDI (Rij), IMM	Load memory with IMM
LDSI LC0/1 SIMM	Load loop counter with 16−bit unsigned SIMM
LDSI A, SIMM	Load A with signed SIMM
LDSI Rij, SIMM	Load pointer register with unsigned SIMM
MLD (Rj), (Ri) [,SQ]	Multiplier load and clear A
MLD Reg, (Ri) [,SQ]	Multiplier load and clear A
MODR Rj, Ri	Pointer register modification
MPYA (Rj), (Ri) [,SQ]	Multiplier load and accumulate
MPYA Reg, (Ri) [,SQ]	Multiplier load and accumulate
MPYS (Rj), (Ri) [,SQ]	Multiplier load and accumulate negative
MPYS Reg, (Ri) [,SQ]	Multiplier load and accumulate negative
MSET (Rj), (Ri) [,SQ]	Multiplier load

Instruction	Description
MSET Reg, (Ri) [,SQ]	Multiplier load
MUL [Cond] [,A] [,P]	Update A and/or PH | PL with X*Y on condition
NEG A [,Cond] [,DW]	Calculate negative value of A on condition
NOP	No operation
OR A, Reg	OR register with AH to AH
OR A, (Rij)	OR memory with AH to AH
OR A, DRAM [,B]	OR (DRAM) with AH to AH
OR A, (Rij)p	OR program memory with AH to AH
OR A, Rc	OR Rc register with AH to AH
ORI A, IMM	OR IMM with AH to AH
ORSI A, SIMM	OR unsigned SIMM with AH to AH
POP Reg [,B]	Pop register from stack
POP Rc [,B]	Pop Rc register from stack
PUSH Reg [,B]	Push register on stack
PUSH Rc [,B]	Push Rc register on stack
PUSH IMM [,B]	Push IMM on stack
REP n	Repeat next instruction n+1 times (9−bit unsigned)
REP Reg	Repeat next instruction Reg+1 times
REP (Rij)	Repeat next instruction (Rij)+1 times
RES Reg, Bit	Clear bit in register
RES (Rij), Bit	Clear bit in memory
RET [B]	Return from subroutine
RND A	Round A with AL
SET Reg, Bit	Set bit in register
SET (Rij), Bit	Set bit in memory
SET_IE	Set interrupt enable flag
SHFT n	Shift A by ± n bits (6−bit signed)
SHFT A [,Cond] [,INV]	Shift A by EXP bits on condition
SLEEP [IE]	Sleep
SUB A, Reg [,C]	Subtract register from A
SUB A, (Rij) [,C]	Subtract memory from A
SUB A, DRAM [,B]	Subtract (DRAM) from A
SUB A, (Rij)p [,C]	Subtract program memory from A
SUB A, Rc [,C]	Subtract Rc register from A
SUBI A, IMM [,C]	Subtract IMM from A
SUSI A, SIMM	Subtract signed SIMM from A
SWAP A [,Cond]	Swap AH, AL on condition
TGL Reg, Bit	Toggle bit in register
TGL (Rij), Bit	Toggle bit in memory
TST Reg, Bit	Test bit in register
TST (Rij), Bit	Test bit in memory

Table 7. NOTATION

Symbol	Meaning
A	Accumulator update
B	Memory bank selection (X or Y)
C	Carry bit
Cond	Condition in status register
DRAM	Low data (X or Y) memory address (8−bits)
DW	Double word
IE	Interrupt enable flag
IMM	Immediate data (16−bits)
INV	Inverse shift
P	PH | PL update
PRAM	Program memory address (16−bits)
Rc	Rc register (R0..7, PCFG0..2, PCFG4..6, LC0/1)
Reg	Data register (AL, AH, X, Y, ST, PC, PL, PH, EXT0, EXP, AE, EXT3..EXT7)
Ri / Rj / Rij	Pointer to X / Y / either data memory
SIMM	Short immediate data (10−bits)
SQ	Square

Weighted Overlap−Add (WOLA) Filterbank Coprocessor

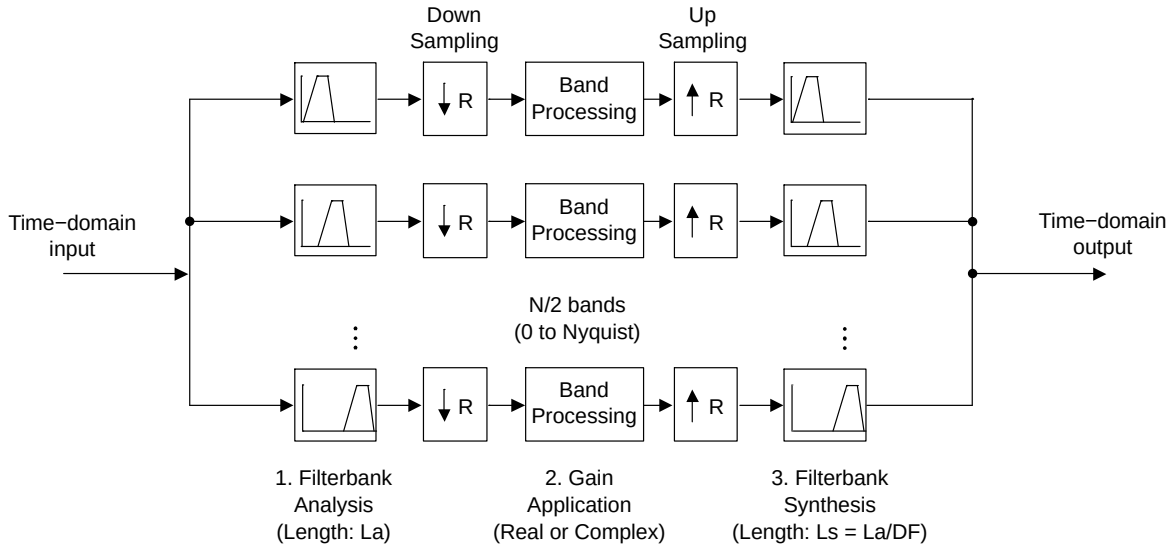


Figure 4. WOLA Filterbank Coprocessor Architecture

The WOLA coprocessor performs low−delay, high−fidelity filterbank processing to provide efficient time−frequency processing and alias−free gain adjustments. The WOLA coprocessor stores intermediate data values as well as program code and window coefficients in its own memory space. Audio data are accessed directly from the input and output FIFOs where they are automatically managed by the IOP.

The WOLA coprocessor can be configured to provide different sizes and types of transforms, such as mono, simple stereo or full stereo configurations. The number of bands, the stacking mode (even or odd), the oversampling factor and the shape of the analysis and synthesis windows used are all configurable. The selected set of parameters affects both the frequency resolution, the group delay through the WOLA coprocessor and the number of cycles needed for complete execution.

The WOLA coprocessor can generate both real and complex data or energy values that represent the energy in each band. Either real or complex gains can be applied to the data. Complex gains provide means for phase adjustments, which is useful in sub−band directional hearing aid applications. The RCore always has access to these values through shared memories. All parameters are configurable with microcode, which is used to control the WOLA coprocessor during execution.

The RCore initiates all WOLA functions (analysis, gain application, synthesis) through dedicated control registers. A dedicated interrupt is used to signal completion of a WOLA function.

A large number of standard WOLA microcode configurations are delivered with the BELASIGNA 250 Evaluation and Development Kit (EDK). These configurations have been specially designed for low group delay and high fidelity.

Input/Output Processor (IOP)

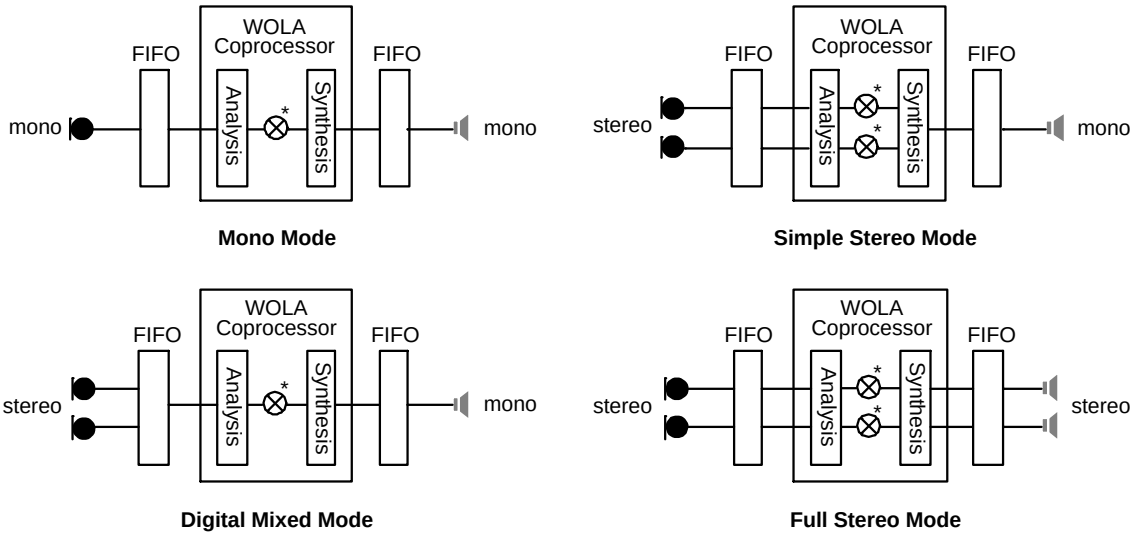
The IOP is an audio−optimized configurable DMA unit for audio data samples. It manages the collection of data from the A/D converters to the input FIFO and feeds digital data to the audio output stage from the output FIFO.

The IOP places and retrieves FIFO data in memories shared with the RCore. Each FIFO (input and output) has two memory interfaces. The first corresponds with the normal FIFO. Here the address of the most recent input block changes as new blocks of samples arrive. The second corresponds with the Smart FIFO. In this scheme the address of the most recent input block is fixed. The Smart FIFO interface is especially useful for time−domain filters.

In the case where the WOLA coprocessor and the IOP no longer work together as a result of a low battery condition, an IOP end−of−battery−life auto−mute feature is available.

The IOP can be configured to access data in the FIFOs in four different audio modes that are shown in Figure 8.

- **Mono mode:** Input samples are stored sequentially in the input FIFO. Output samples are stored sequentially in the output FIFO.
- **Simple stereo mode:** Input samples from the two channels are interleaved in the input FIFO. Output samples for the single output channel are stored in the lower part of the output FIFO.
- **Digital mixed mode:** Input samples from the two channels are stored in each half of the input FIFO. Output samples for the single output channel are stored in the lower half of the output FIFO.
- **Full stereo mode:** Input samples from the two channels are interleaved in the input FIFO. Output samples for the two output channels are also interleaved in the output FIFO.



* Real & Complex Gain Application

Figure 5. Audio Modes

Other Digital Blocks and Functions

RAM and ROM

There are 20−Kwords of on−chip program and data RAM on BELASIGNA 250. These are divided into three entities: a 12−Kword program memory, and two 4−Kword data memories (“X” and “Y”, as are common in a dual−Harvard architecture).

There are also three RAM banks that are shared between the RCore and WOLA coprocessor. These memory banks contain the input and output FIFOs, gain tables for the WOLA coprocessor, temporary memory for WOLA calculations, WOLA coprocessor results, and the WOLA coprocessor microcode.

There is a 128−word lookup table (LUT) ROM that contains $\log_2(x)$, 2^x, 1/x and sqrt(x) values, and a 1−Kword program ROM that is used during booting and configuration of the system.

Memory Maps

Complete memory maps for BELASIGNA 250 are shown in Figure 6.

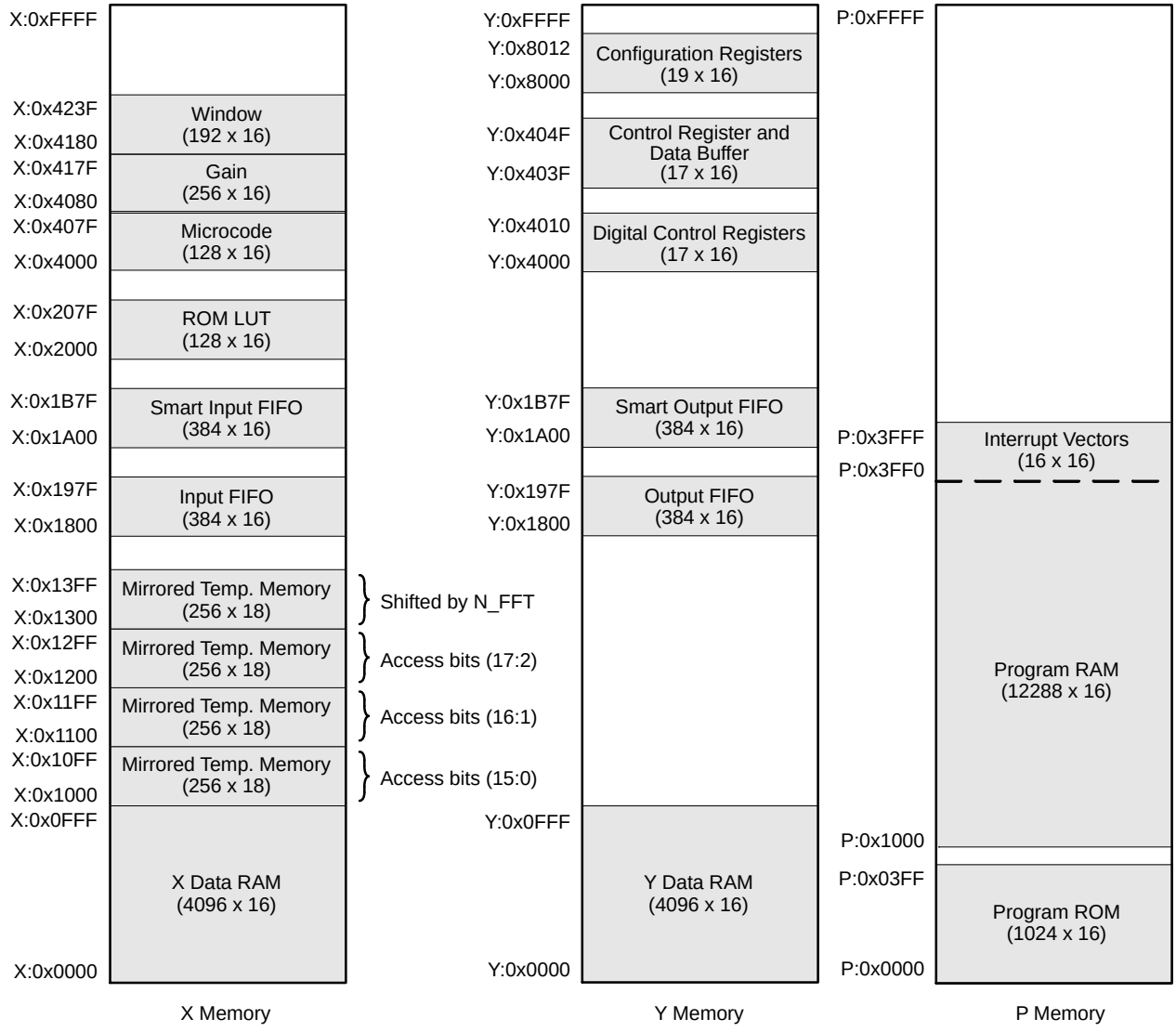


Figure 6. Memory Maps

General−Purpose Timer

The general−purpose timer is a 12−bit countdown timer with a 3−bit prescaler that interrupts the RCore when it reaches zero. It can operate in two modes, single−shot or continuous. In single−shot mode, the timer counts down only once and then generates an interrupt. It will then have to be restarted from the RCore. In continuous mode, the timer “wraps around” every time it hits zero and interrupts are generated continuously. This unit is often useful in scheduling tasks that are not part of the sample−based signal−processing scheme, such as checking a battery voltage or reading the value of a volume control.

Watchdog Timer

The watchdog timer is a programmable hardware timer that operates from the system clock and is used to ensure system sanity. It is always active and must be periodically acknowledged as a check that an application is still running. Once the watchdog times out, it generates an interrupt. If left to time out a second consecutive time without acknowledgement, BELASIGNA 250 will fully reset itself.

Interrupts

The RCore has a single interrupt channel that serves 13 interrupt sources in a prioritized manner. The interrupt controller also handles interrupt acknowledge flags. Every interrupt source has its own interrupt vector. Furthermore, the priority scheme of the interrupt sources can be modified. Refer to Table 8 for a description of all interrupts.

Table 8. INTERRUPT DESCRIPTIONS

Interrupt	Description
WOLA_DONE	WOLA function done
IO_BLOCK_FULL	IOP interrupt
GP_TIMER	General−purpose timer interrupt
WATCHDOG_TIMER	Watchdog timer interrupt
SPI_INTERFACE	SPI interface interrupt
IR	IR remote interrupt
EXT3_RX	EXT3 register receive interrupt
EXT3_TX	EXT3 register transmit interrupt
GPIO	User configurable GPIO interrupt
TWSS_INTERFACE	Two−wire synchronous serial interface interrupt
UART_RX	General−purpose UART receive interrupt
UART_TX	General−purpose UART transmit interrupt
PCM	PCM interface interrupt

Analog Blocks

Input Stage

The analog audio input stage is comprised of two individual channels. For each channel, the selected one out of the four possible inputs is routed to the input of the programmable preamplifier that can be configured for bypass or gain values of 12 to 30 dB (3 dB steps).

The analog signal is filtered to remove frequencies above 20 kHz before it is passed into the high−fidelity 16−bit oversampling ΣΔ A/D converter. Subsequently, any necessary sample rate decimation is performed to downsample the signal to the desired sampling rate. During decimation the level of the signal can be adjusted digitally for optimal gain matching between the two input channels. Any undesired DC component can be removed by a configurable DC−removal filter that is part of the decimation circuitry. The DC removal filter can be configured for bypass or cut−off frequencies at 5, 10 and 20 Hz.

A built−in feature allows a sampling delay to be configured between channel zero and channel one (or vice versa). This is useful in beam−forming applications.

Note: Both preamplifiers can be daisy−chained to increase the potential gain, but the signal has to be routed externally to the chip.

For power consumption savings either of the input channels can be disabled via software. A different input must be selected for each channel. The input stage is shown in Figure 7.

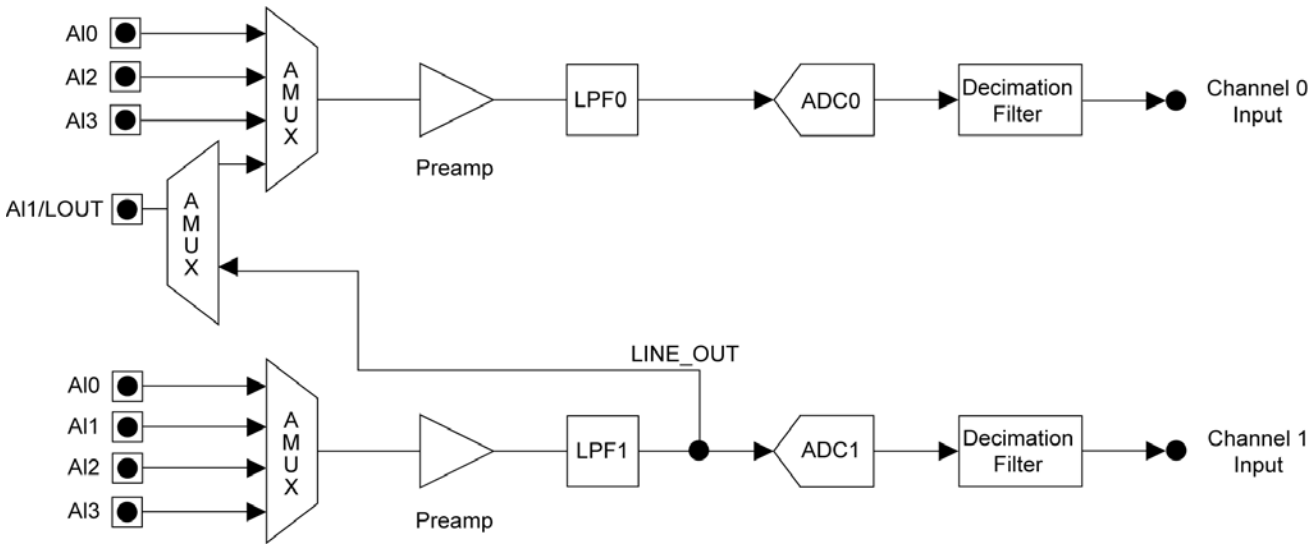


Figure 7. Input Stage

Output Stage

The analog audio output and the digital output are composed of two individual channels. The first part of the output stage interpolates the signal for highly oversampled D/A conversion and automatically configures itself for the desired over−sampling rate. Here, the signal is routed to the ΣΔ D/A converter and the direct digital outputs.

The D/A converter translates the signal into a high−fidelity analog signal and passes it into a third order analog reconstruction filter to smooth out the effects of sampling. The reconstruction filter has a cut−off frequency configurable at 10 or 20 kHz.

From the reconstruction filter, the signal passes through the programmable output attenuator, which can adjust the signal for various line level outputs or mute the signal altogether. The attenuator can be configured to a value in the interval 12 to 30 dB (3 dB steps) or it can be bypassed.

The direct digital outputs provide two H−bridges driven by pulse−density modulated outputs that can be used to directly drive an output transducer without the need for a separate power amplifier. The output driver has a dedicated power−supply pin, which allows for separation (through RC−filtering) between the supply for the analog blocks on the chip and the supply for the output driver.

The output stage is shown in Figure 8.

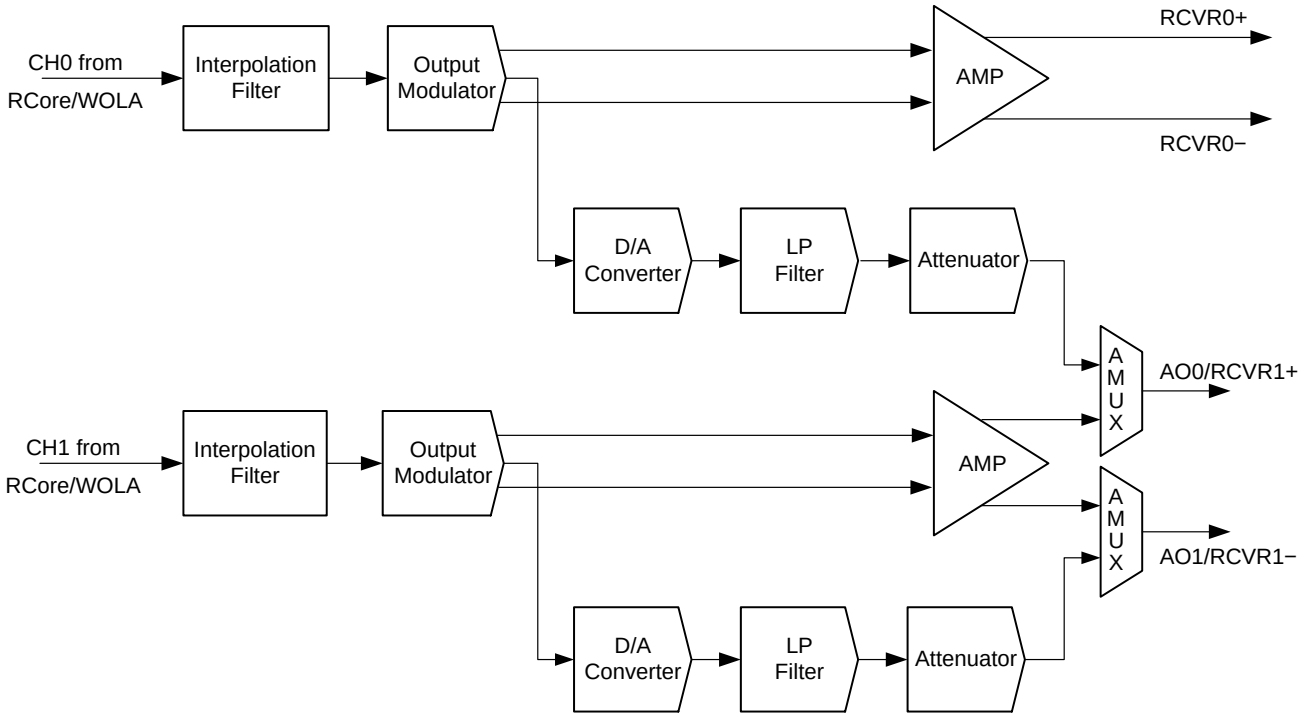


Figure 8. Output Stage

Clock−Generation Circuitry

The chip operates with five clock domains to provide flexibility in the control of peripherals, the selection of sampling frequencies and the configuration of interface communication speeds. The five clock domains are as follows in Table 9. The base clock for all operations on the BELASIGNA 250 chip is the system clock (SYS_CLK). This clock may be acquired from one of three sources: the main on−chip oscillator, the system standby clock or an external clock signal.

Table 9. CLOCK DOMAINS

Clock Name	Description	Used For
SYS_CLK	System clock	All on−chip processors such as RCore, WOLA, IOP
MCLK	Main clock	All A/D and D/A converters
PCLK	Peripheral clock	Debug port, remote control, watchdog timer
WOLACLK	WOLA clock	WOLA module computations
UCLK	User clock	Can be programmed to provide a dedicated clock for an external device

The internal RC oscillator is characterized to operate up to a frequency of 5.12 MHz. To operate properly using this internal clock, BELASIGNA 250 has to be calibrated, and the calibration values are to be stored within a non−volatile memory (usually an SPI EEPROM). When calibration isn't possible, BELASIGNA 250 can operate with an externally supplied SYS_CLK, in this case, it is qualified for operation up to 50 MHz.

The sampling frequency for all A/D and D/A converters depends on MCLK. When MCLK is 1.28 MHz, sampling frequencies up to 20 kHz can be selected. When MCLK is 1.92 MHz sampling frequencies up to 30 kHz can be selected. For MCLK equal to 2.56 MHz sampling frequencies up to 40 kHz can be selected. For MCLK equal to 3.84 MHz, sampling frequencies up to 60 kHz can be selected.

The WOLA clock (WCLK) feature allows WOLA operations to be performed at a frequency slower than SYS_CLK. This feature allows the dynamic current consumption related to the digital blocks to be "spread" over a longer period of time, smoothing the system's dynamic current draw, which can affect the audio signal.

The user clock (UCLK) can be used to provide a clock signal to an external component, independently from the EXT_CLK pin functionality. It can be derived from SYS_CLK with a variety of derivation factors, or can be connected to MCLK or even PCLK. One instance in which it is beneficial to use this feature is when a continuous external clock output is required but when EXT_CLK is already being used to provide SYS_CLK to BELASIGNA 250.

Power Supply Unit

Voltage Modes

BELASIGNA 250 can operate in three different power supply modes: high, low and double voltage. These modes allow BELASIGNA 250 to integrate into a wider variety of devices with a range of voltage supplies and communications levels. The power supply modes are described below:

- **High voltage (HV) power supply mode:** BELASIGNA 250 operates from a nominal supply of 1.8 V on VBAT, but this can scale depending on available supply. All digital sections of the system, including digital I/O pads, run from the same voltage as supplied on VBAT. This mode is preferable in designs where a very stable supply is available and BELASIGNA 250 will be interfacing to other digital systems at the same voltage. This mode is also necessary for higher than 5.12 MHz system clocks.
- **Low voltage (LV) power supply mode:** BELASIGNA 250 operates from a nominal supply of 1.25 V. The WOLA, the RCore and all digital I/O pads run from a 1 V regulated supply. The low voltage operation of the processing cores is very power−efficient, but the system clock should be kept under 5.12 MHz to ensure proper operation.
- **Double voltage (DV) power supply mode:** BELASIGNA 250 operates from a nominal supply of 1.25 V. The WOLA, the RCore and all digital I/O pads run from the on−chip charge pump which regulates internal voltage up to 2 V. This allows BELASIGNA 250 to communicate with higher voltage systems like a 1.8 V EEPROM when running on a lower supply voltage. However, a specific level translation mechanism has been designed to allow BELASIGNA 250 to communicate with an SPI EEPROM in low voltage mode as well. This voltage mode is not suitable for normal operation, processing in this mode may result in audible audio artifacts. Most BELASIGNA 250 applications run in high voltage mode.

Power−on−Reset (POR) and Booting Sequence

At POR, all control registers and RCore registers are put into known default states. During the power−on procedure, all audio outputs are muted; all RCore registers and all control registers (analog and digital) are set to default values. (Please contact ON Semiconductor for more

information on default values associated with each control register.)

BELASIGNA 250 boots in a two−stage boot sequence. The program ROM begins loading the bootloader from an external EEPROM 200 ms after power is applied to the chip. In this process the program ROM checks the bootloader for validity, which in turn ensures the file system validity. If the file structure is validated, the bootloader is written to PRAM. In case of an error while reading the external EEPROM, all outputs are muted. The system restarts approximately every second and attempts to reboot.

Once the bootloader is loaded into PRAM the program counter is set to point to the beginning of the bootloader code. Subsequently, the signal−processing application that is stored in the EEPROM is downloaded to PRAM by the bootloader. The boot process generally takes less than one second. ON Semiconductor provides a standard full−feature bootloader. A graphical representation of this booting sequence can be seen in Figure 9.

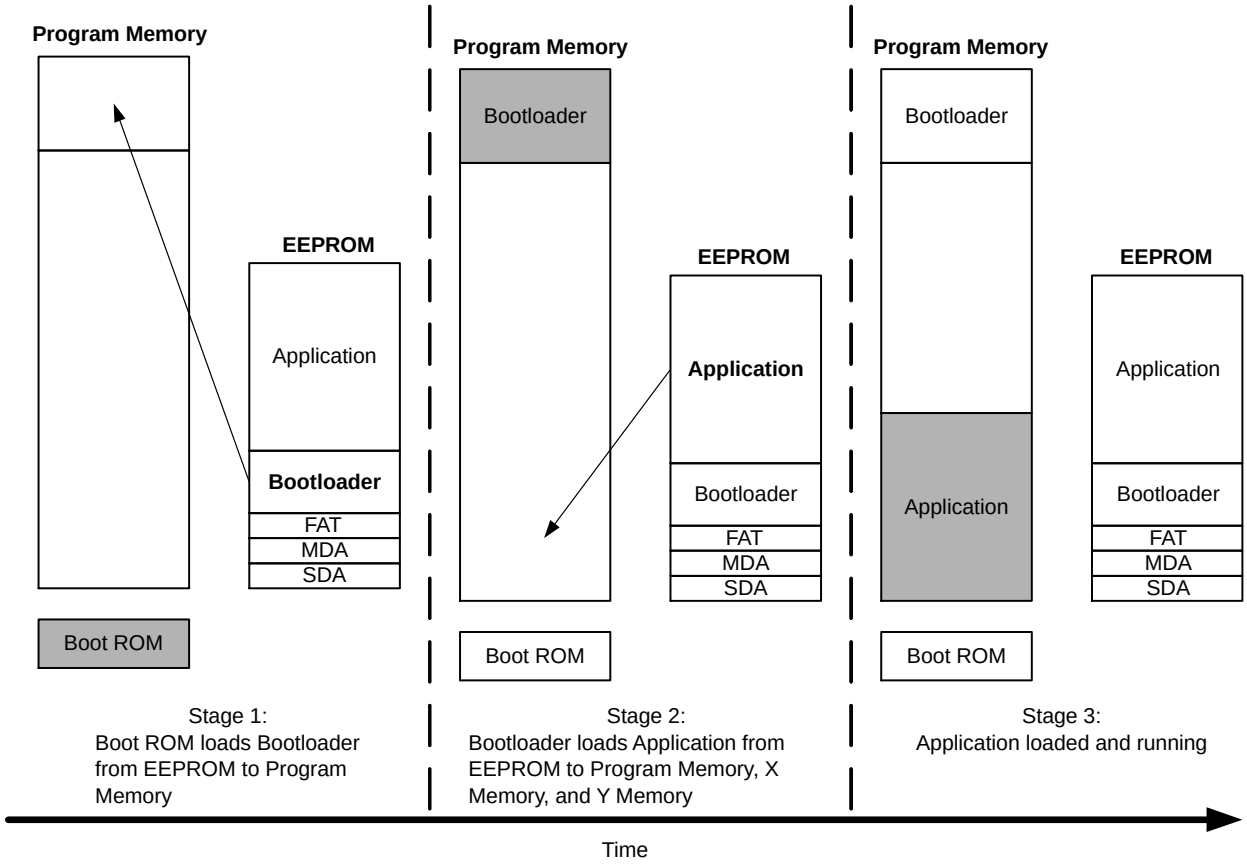


Figure 9. Booting Sequence

Power Management Strategy

BELASIGNA 250 has a built−in power management unit that guarantees valid system operation under any voltage supply condition to prevent any unexpected audio output as the result of any supply irregularity. The unit constantly monitors the power supply and shuts down all functional units (including all units in the audio path) when the power supply voltage goes below a level at which point valid operation can no longer be guaranteed.

The power supply operation can be seen in Figure 10. Once the supply voltage rises above the startup voltage of the internal regulator that supplies the digital subsystems ($VDDC_{STARTUP}$) and remains there for the length of time T_{POR}, a POR will occur. If the supply is consistent, the internal system voltage will then remain at a fixed nominal voltage ($VDDC_{NOMINAL}$). If a spike occurs that causes the voltage to drop below the shutdown internal system voltage ($VDDC_{SHUTDOWN}$), the system will shut down. If the voltage rises again above the startup voltage and remains there for the length of time T_{POR}, a POR will occur. If operating directly off a battery, the system will not power down until the voltage drops below the $VDDC_{SHUTDOWN}$ voltage as the battery dies. This prevents unwanted resets when the voltage is just on the edge of being too low for the system to operate properly because the difference between $VDDC_{STARTUP}$ and $VDDC_{SHUTDOWN}$ prevents oscillation around the $VDDC_{SHUTDOWN}$ point.

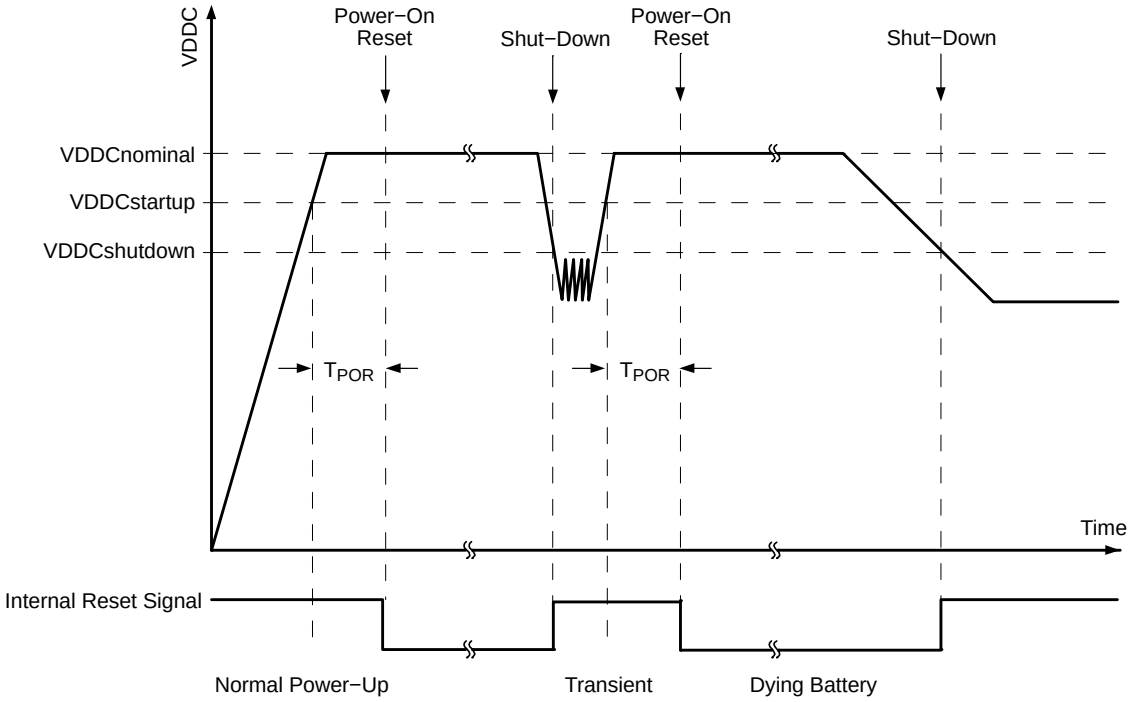


Figure 10. Power Management

Other Analog Support Blocks and Functions

Multi−Chip Sample Clock (MCLK) Synchronization

BELASIGNA 250 allows MCLK synchronization between two or more BELASIGNA 250 devices connected in a multi−chip configuration. Samples on multiple chips will synchronize to occur at the same instant in time. This is useful in applications using microphone arrays where synchronous sampling is required. The sample clock synchronization is enabled using a control bit and a GPIO assignment that brings all MCLKs across chips to zero phase at the same instant in time.

Low−Speed A/D Converters (LSAD)

Six LSAD inputs are available on BELASIGNA 250. Combined with two internal LSAD inputs (supply and ground), there are a total of eight multiplexed inputs to the LSAD converter. The multiplexed inputs are sampled sequentially at 1.6 kHz per channel when operating at MCLK of 1.28 MHz (proportionally). The native data format for the LSAD is 10−bit two's−complement. However, a total of eight operation modes are provided that allow a configurable input dynamic range in cases where certain minimum and maximum values for the converted inputs are desired, such as in the case of a volume control where only input values up to a certain magnitude are allowed. The six LSAD pads are multiplexed with other functionality.

Battery Monitor

A programmable on−chip battery monitor is available for power management. The battery monitor works by incrementing a counter value every time the battery voltage goes below a desired, configurable threshold value. This counter value can be used in an application−specific power−management algorithm running on the RCore. The RCore can initiate any desired actions in case the battery hits a predetermined value. This function is realized with an internal LSAD tied directly to the power supply.

Infrared (IR) Remote Control

A switched−carrier IR remote control receiver interface is provided, which can receive commands wirelessly with the attachment of a photovoltaic diode or similar component. Data transfer from a remote unit is initiated by first transmitting a burst sequence followed by the data to be transferred. The data must be RS−232 formatted (8N1) and must be modulated using a 40 kHz switched−carrier modulation scheme. Data are received at 1200 bps by a dedicated UART. The remote control receiver interacts with the RCore through memory mapped control registers and interrupts.

Digital Interfaces

BELASIGNA 250 has the following digital interfaces:

- 16−pin general−purpose I/O (GPIO) interface.
- Serial peripheral interface (SPI) communications port with interface speeds up to 640 kbps at 1.28 MHz system clock. The SPI port on BELASIGNA 250 only supports master mode, so it will only communicate with SPI slave devices. When connecting to an SPI slave device other than a boot EEPROM, the SPI_CS pin should be left unconnected and the slave device CS line should be driven from a GPIO to avoid BELASIGNA 250 boot malfunction. When connecting to an SPI EEPROM for boot, the designer can choose to connect the SPI_CS pin to the EEPROM or use a GPIO

(high at boot) for a design with several daisy−chained SPI devices.

- PCM interface for high−bandwidth digital audio I/O. This interface comes with configurable input and output buffers for reduced interrupt handling overhead when BELASIGNA 250 is used in an audio streaming application.
- Configurable high−speed RS−232 universal asynchronous receiver/transmitter (UART).
- RS−232−based communications port for debugging and in−circuit emulation. This interface can also be used to send analog audio data to the input stage.
- Two−wire synchronous serial (TWSS) interface compatible with the I^2C protocol and with speeds up to 100 kbps at 1.28 MHz MCLK and up to 400 kbps at MCLKs higher than 1.92 MHz. Supports master and slave operation.

Assembly Information

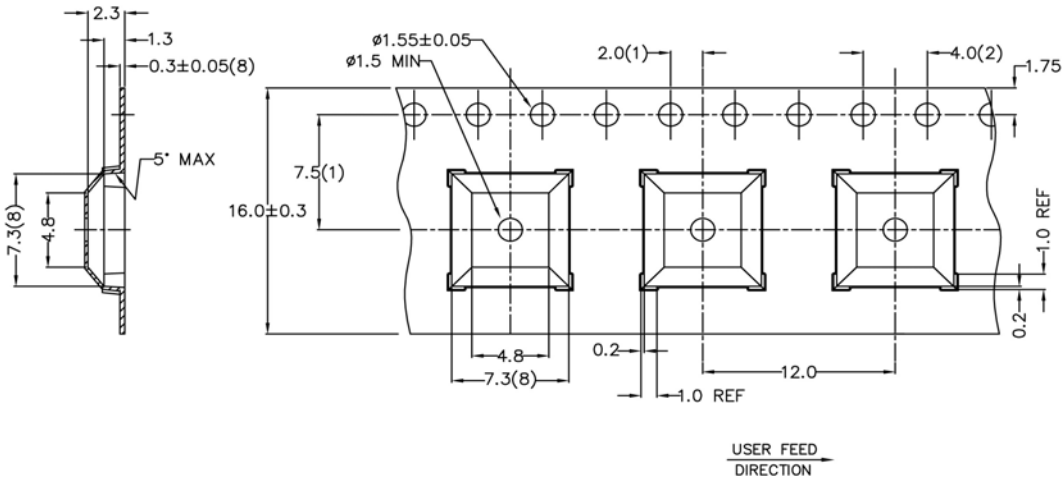
Carrier Details
7 x 7 mm LFBGA

ON Semiconductor offers tape and reel packing for BELASIGNA 250 LFBGA packages. The packing consists of a pocketed carrier tape, a cover tape, and a molded anti−static polystyrene reel. The carrier and cover tape create an ESD safe environment, protecting the components from physical and electrostatic damage during shipping and handling.

Quantity per Reel: 1500 units
Pin 1 Orientation: Upper Left
Each complete reel contains 1500 parts.
Brand: PEAK
P/N: CP3−BG0707−16−12.0B4

A = 13 inches
B = 16 mm
C = 4 inches
D = 14 mm

Figure 11. Package Orientation on Tape



1. Measured from the centerline of sprocket hole to centerline of the pocket hole and from the centerline of sprocket hole to centerline of the pocket.
2. Cumulative tolerance of 10 sprocket holes is ±0.20.
3. This thickness is applicable as measured at the edge of the tape.
4. Material: conductive polystyrene.
5. Dimensions in mm.
6. Allowable camber to be 1 mm per 100 mm in length, non−cumulative over 250 mm.
7. Unless otherwise specified, tolerance ±0.10.
8. Measurement point to be 0.3 from bottom pocket.
9. Surface resistivity less than or equal to 1.0X10E9 Ω^2.

Figure 12. Carrier Tape Drawing

Moisture Sensitivity Level

BELASIGNA 250 is MSL JEDEC Level 3.

Re−flow Information

The re−flow profile depends on the equipment that is used for the re−flow and the assembly that is being re−flowed. Use the following table from the JEDEC Standard 22−A113D and J−STD−020D.01 as a guideline:

Electrostatic Discharge (ESD) Sensitive Device

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality. Device is 2 kV HBM ESD qualified.

Miscellaneous

Chip Identification

The Evaluation and Development Tools include a method for verifying the chip version. A BELASIGNA 250 chip will respond as follows:

Family: 0x01 or 0x02

Version: 0x0B

ROM Version: 0x0206

Support Software

A full suite of comprehensive tools is available to assist software developers from the initial concept and technology assessment through to prototyping and product launch. Simulation, application development and communication tools as well as an Evaluation and Development Kit (EDK) facilitate the development of advanced algorithms on BELASIGNA 250.

Training

To facilitate development on the BELASIGNA 250 platform, training is available upon request. Contact your account manager for more information.

Company or Product Inquiries

For more information about ON Semiconductor products or services visit our Web site at http://onsemi.com.

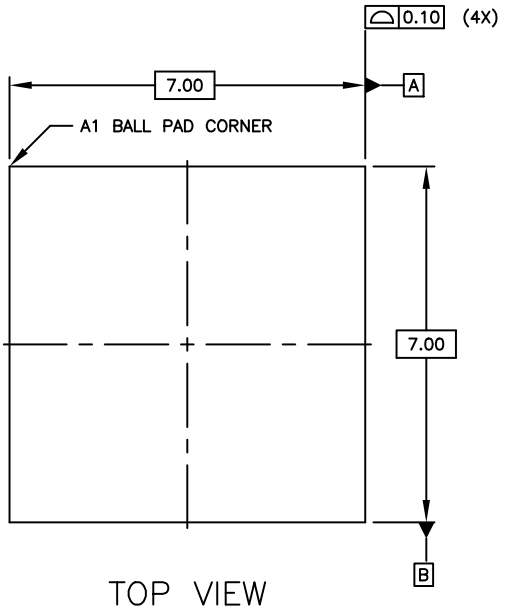
Table 10. ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Shipping†
0W888−002−XTP	−85 to 40°C	7 x 7 mm LFBGA (Pb−Free)	1500 / Tape & Reel

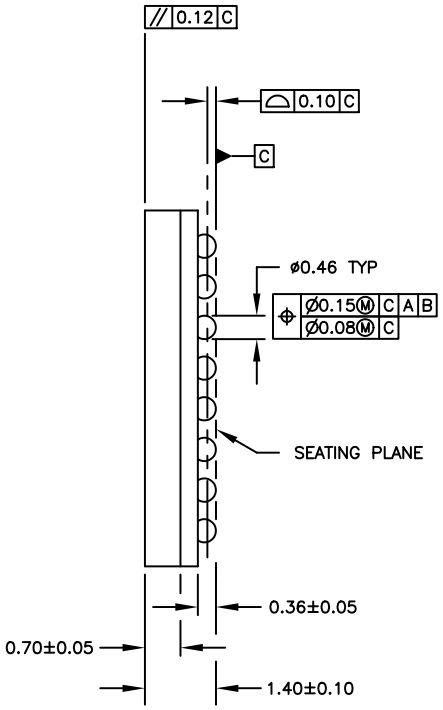
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

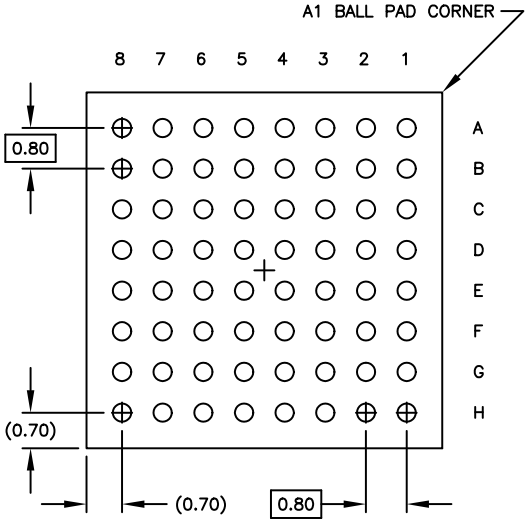
LFBGA 64, 7x7
CASE 566AF
ISSUE O



TOP VIEW



SIDE VIEW



BOTTOM VIEW
64 SOLDER BALLS

W/B No.	BALL No.	W/B No.	BALL No.	W/B No.	BALL No.	W/B No.	BALL No.
1	B1	17	H2	33	G8	49	A7
2	D4	18	E4	34	E5	50	D5
3	C1	19	H3	35	F8	51	A6
4	D3	20	F4	36	E6	52	C5
5	C2	21	G3	37	F7	53	B6
6	D1	22	H4	38	E8	54	A5
7	E3	23	F5	39	D6	55	C4
8	D2	24	G4	40	E7	56	B5
9	E1	25	H5	41	D8	57	A4
10	E2	26	G5	42	D7	58	B4
11	F1	27	H6	43	C8	59	A3
12	F3	28	F6	44	C6	60	C3
13	F2	29	G6	45	C7	61	B3
14	G1	30	H7	46	B8	62	A2
15	G2	31	G7	47	B7	63	B2
16	H1	32	H8	48	A8	64	A1

BELASIGNA 250

PUBLICATION ORDERING INFORMATION

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