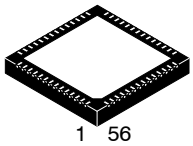
8+2 Phase Output Controller with SVID Interface for Desktop Computer CPU Applications

ASP2100, ASP2100R



QFN56
CASE 485BT

The ASP2100 and ASP2100R are dual rail, eight plus two phase buck solutions optimized for Intel®'s IMVP9.1 Rev0.9 and Rev0.95 CPU's respectively. The multi−phase rail control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing or smart power stage current sensing. These features provide an ultra−fast initial response to dynamic load events and reduced system cost. The ASP2100 has an ultra−low offset current monitor amplifier with programmable offset compensation for high accuracy current monitoring.

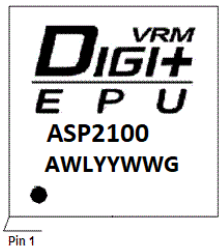
Features

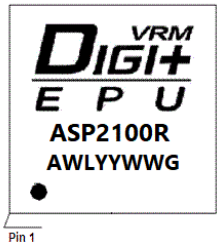
- Vin Range 4.5 V to 21 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Digital Soft Start Ramp
- Adjustable V_{BOOT}
- High Impedance Differential Amplifier for Accurate Output Voltage Sensing
- Dual VID Table Support to be Compatible with IMVP9.1
- Support for High Current Extensions
- Auto Phase Shedding
- Dynamic Reference Injection
- Programmable Output Voltage Slew Rates
- Dynamic VID Feed−Forward
- Differential Current Sense Amplifiers for Each Phase
- Programmable Adaptive Voltage Positioning (AVP)
- Current Mode Dual Edge Modulation for Fastest Initial Response to Transient Loading
- High Performance Operational Error Amplifier
- Accurate Total Summing Current Amplifier
- Thermal Monitor
- Adjustable Switching Frequency Range
- Digitally Stabilized Switching Frequency
- Ultrasonic Operation
- Support Acoustic Noise Mitigation Function
- PSYS Input Monitor (SVID address 0x0D)
- Support for VCCIN_AUX IMON Input
- Meets Intel's IMVP9.1 Specifications
- I^2C Control Interface

Typical Applications

- Desktop Computers

MARKING DIAGRAMS





A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free

ORDERING INFORMATION

Device	Package	Shipping†
ASP2100MNTXG	QFN56 (Pb−Free)	2500 / Tape & Reel
ASP2100RMNTXG	QFN56 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

BLOCK DIAGRAM

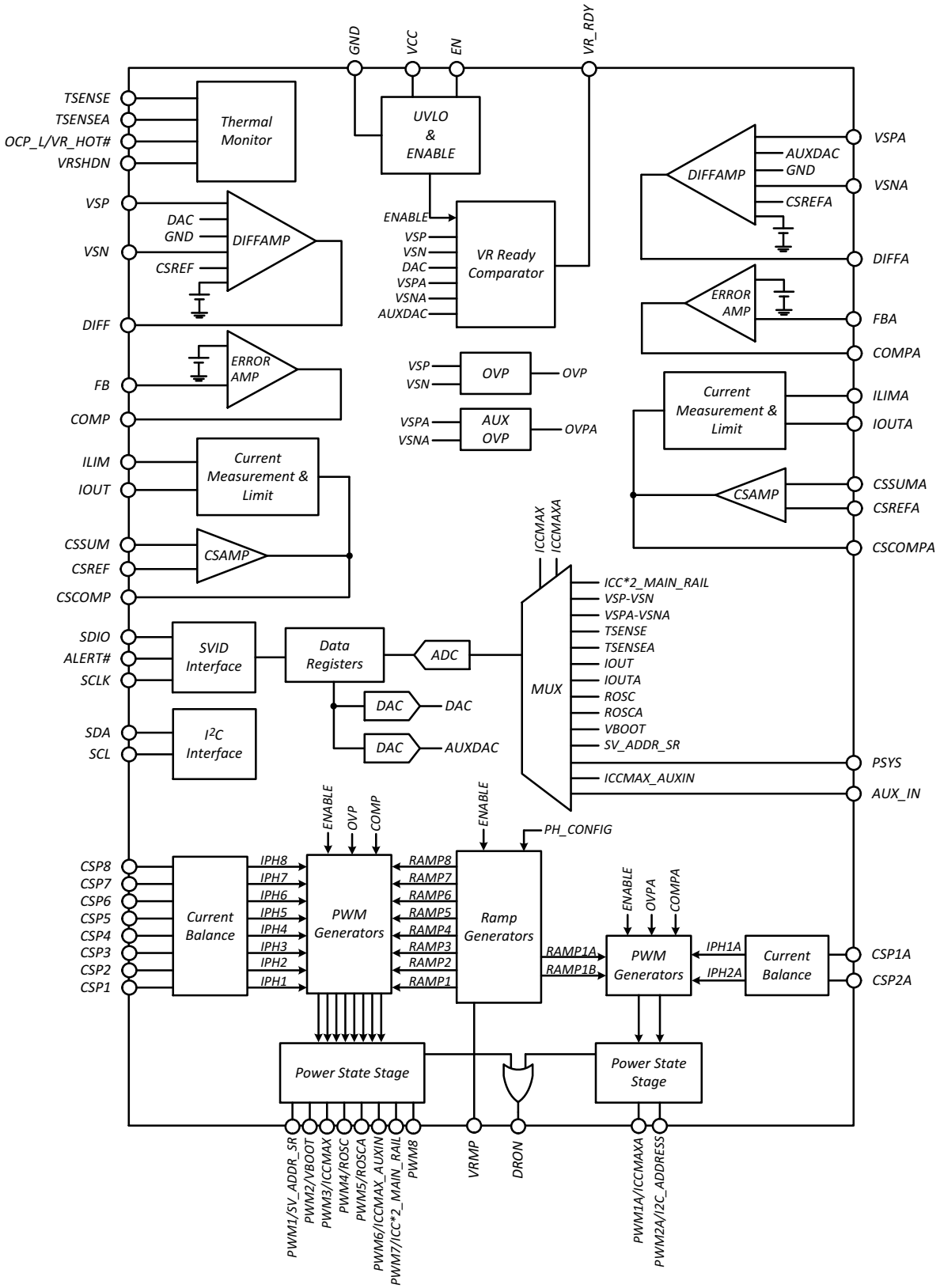


Figure 1. Internal Block Diagram

APPLICATION INFORMATION

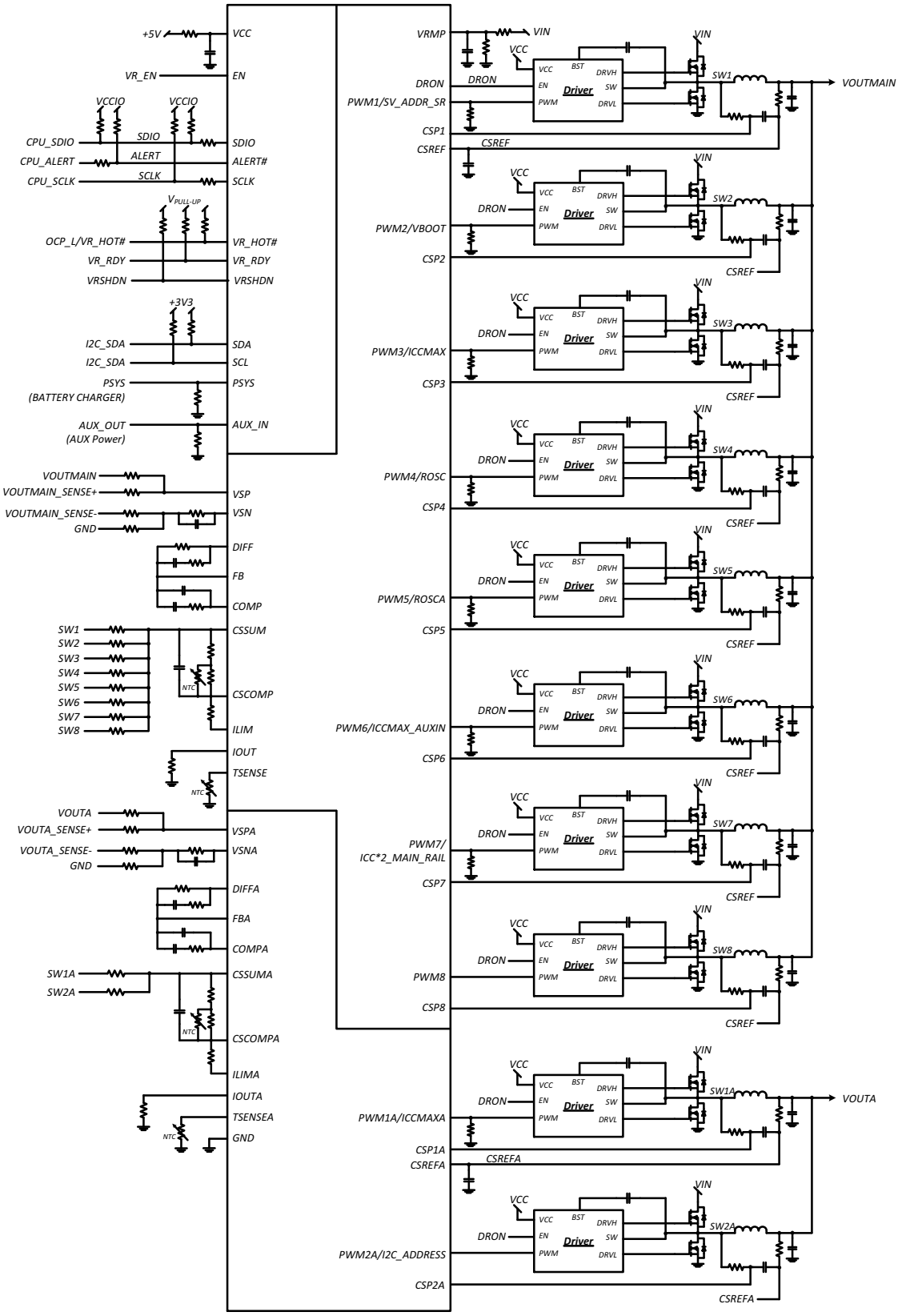


Figure 2. Typical Application Circuit

PIN ASSIGNMENT

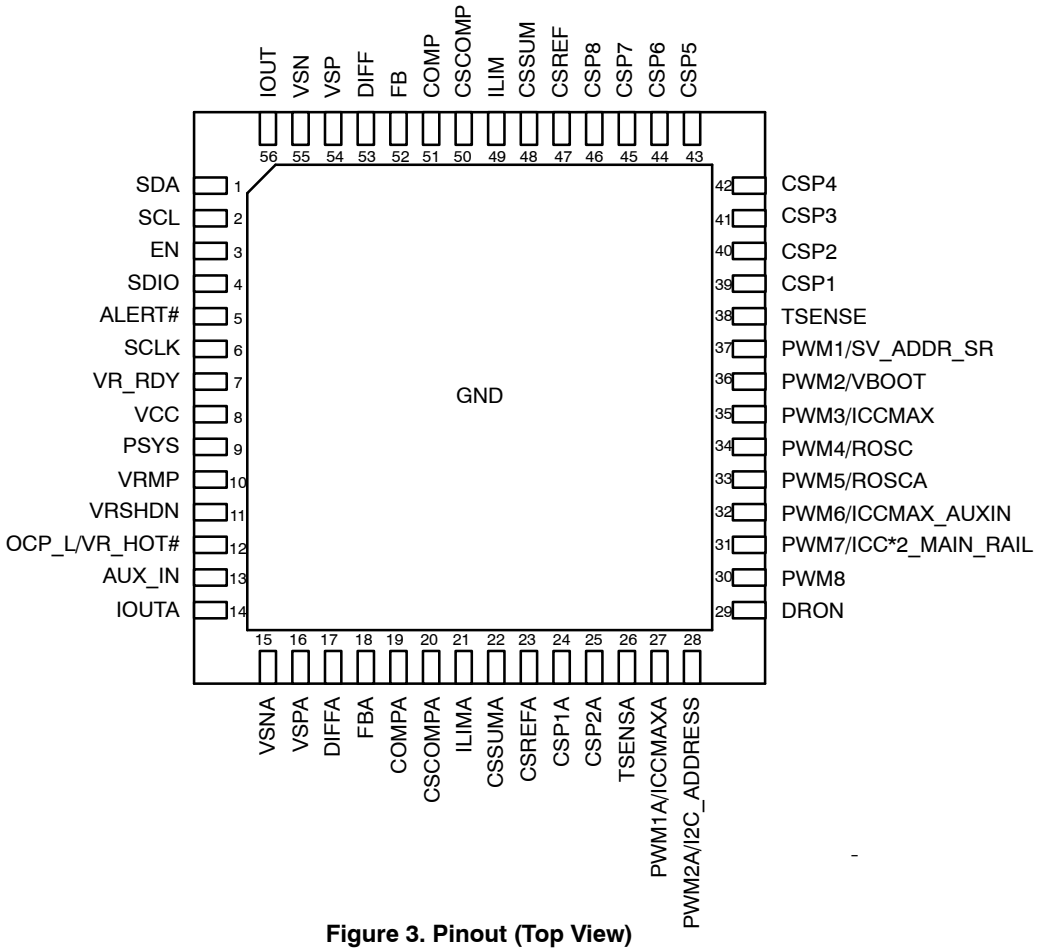


Figure 3. Pinout (Top View)

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	SDA	I^2C bus serial data interface
2	SCL	I^2C bus clock
3	EN	Enable. High enables both rails
4	SDIO	Serial VID data interface
5	ALERT#	Serial VID ALERT#
6	SCLK	Serial VID clock
7	VR_RDY	VR_RDY indicates both rails are ready to accept SVID commands
8	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
9	PSYS	System power signal input. A resistor to ground scales this signal
10	VRMP	Feed−forward input of Vin for the ramp−slope compensation. The current fed into this pin is used to control the ramp of the PWM slopes
11	VRSHDN	VRSHDN output, pulled and latched low until power off if VR temp reaches programmed level
12	OCP_L/VR_HOT#	OD output. Indicates high VR temperature, or OCP_L threshold crossed. OCP_L need to enable by I^2C
13	AUX_IN	AUX IMON Input on 0x0Dh SVID domain. A resistor to ground scales this signal.
14	IOUTA	Total output current monitor
15	VSNA	Differential output voltage negative sense for regulator 2
16	VSPA	Differential output voltage positive sense for regulator 2

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Pin Name	Description
17	DIFFA	Output of the regulator 2 differential remote sense amplifier
18	FBA	Error amplifier voltage feedback for regulator 2
19	COMPA	Output of the error amplifier and the inverting inputs of the PWM comparators for regulator 2
20	CSCOMPA	Output of total−current−sense amplifier for regulator 2
21	ILIMA	Over−current threshold setting − programmed with a resistor to CSCOMPA for regulator 2
22	CSSUMA	Inverting input of total−current−sense amplifier for regulator 2
23	CSREFA	Total−current−sense amplifier reference voltage input for regulator 2
24	CSP1A	Non−inverting input to current−balance amplifier for Phase 1 of regulator 2
25	CSP2A	Non−inverting input to current−balance amplifier for Phase 2 of regulator 2
26	TSENSEA	Temperature sense input for regulator 2
27	PWM1A/ICCMAXA	PWM1 output for regulator 2. Pulldown on this pin programs ICCMAX for regulator 2 during startup
28	PWM2A/ I2C_ADDRESS	PWM2 output for regulator 2. Pulldown on this pin programs I^2C address during startup
29	DRON	External FET driver enable for discrete driver or ONSemi DrMOS
30	PWM8	PWM8 output for regulator 1.
31	PWM7/ ICC*2_MAIN_RAIL	PWM7 output for regulator 1/Pulldown resistor on this pin can be used to enable ICC*2_MAIN_RAIL function.
32	PWM6/ ICCMAX_AUXIN	PWM6 output for regulator 1/Pulldown resistor on this pin programs ICCMAX for the AUX_IN monitoring rail
33	PWM5/ROSCA	PWM5 output for regulator 1/Pulldown on this pin programs RoscA value for regulator 2
34	PWM4/ROSC	PWM4 output for regulator 1/Pulldown on this pin programs Rosc value for regulator 1
35	PWM3/ICCMAX	PWM3 output for regulator 1/Pulldown on this pin programs ICCMAX for regulator 1 during startup
36	PWM2/VBOOT	PWM2 output for regulator 1/Pin−program for regulator 1 and regulator 2 Vboot
37	PWM1/ SV_ADDR_SR	ASP2100: PWM1 output for regulator 1/Pulldown on this pin configures SVID address and slew rate. ASP2100R: PWM1 output for regulator 1 / Pulldown on this pin configures SVID address, slew rate and VR_Hot control for Fast V−Mode.
38	TSENSE	Temperature sense input for regulator 1
39	CSP1	Differential current sense positive for Phase 1 of regulator 1
40	CSP2	Differential current sense positive for Phase 2 of regulator 1
41	CSP3	Differential current sense positive for Phase 3 of regulator 1
42	CSP4	Differential current sense positive for Phase 4 of regulator 1
43	CSP5	Differential current sense positive for Phase 5 of regulator 1
44	CSP6	Differential current sense positive for Phase 6 of regulator 1
45	CSP7	Differential current sense positive for Phase 7 of regulator 1
46	CSP8	Differential current sense positive for Phase 8 of regulator 1
47	CSREF	Total−current−sense amplifier reference voltage input for regulator 1
48	CSSUM	Inverting input of total−current−sense amplifier for regulator 1
49	ILIM	Over−current threshold setting − programmed with a resistor to CSCOMP for regulator 1
50	CSCOMP	Output of total−current−sense amplifier for regulator 1
51	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators for regulator 1
52	FB	Error amplifier voltage feedback for regulator 1
53	DIFF	Output of the regulator 1 differential remote sense amplifier
54	VSP	Differential output voltage sense positive for regulator 1
55	VSN	Differential output voltage sense negative for regulator 1
56	IOUT	Total output current monitor for regulator 1
	Flag	GND

1. “Regulator 1” is referred to as “Main” rail throughout the datasheet. “Main” is the primary rail with the highest phase count.
2. “Regulator 2” is referred to as “A” rail throughout the datasheet.

MAXIMUM RATINGS (Note 3)

Pin Symbol	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
COMP, COMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP, CSCOMPA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWMX	VCC + 0.3 V	−0.3 V	–	1 mA
VSN, VSNA	GND + 0.3 V	GND − 0.3 V	1 mA	2 mA
DIFF, DIFFA	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VR_RDY	VCC + 0.3 V	−0.3 V	2 mA	–
VCC	6.0 V	−0.3 V	–	–
VRMP	VCC + 0.3 V	−0.3 V	–	–
SCLK, SDIO	3.6 V	−0.3 V	–	–
All Other Pins	VCC + 0.3 V	−0.3 V	–	–

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. All signals referenced to GND unless noted otherwise

ESD CAPABILITY

Description	Symbol	Typ	Unit
ESD Capability, Human Body Model (Note 4)	ESDHBM	2,000	V
ESD Capability, Charged Device Model (Note 4)	ESDCDM	750	V

4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charge Device Model tested per AEC−Q100−011 (EIA/JESD22−C101)
   Latch−up Current Maximum Rating: ≤ 200 mA per JEDEC standard: JESD78.

RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Min	Max	Unit
VCC Voltage Range	VCC	4.75	5.25	V
Operating Junction Temperature Range (Note 5)	TJ	−10	125	°C
Operating Ambient Temperature Range	TA	−10	100	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. JEDEC JESD 51−7 with 0 LFM.

THERMAL CHARACTERISTICS

Description	Symbol	Value	Unit
Thermal Characteristic QFN Package	R_{JA}	65	°C/W
Maximum Storage Temperature Range	T_{STG}	−40 to +150	°C
Soldering Temperature		260	°C
Junction−to−Ambient, Thermal Resistance (Note 6)	θ_{JA}	30	°C/W
Junction−to−Case (Top), Thermal Resistance (Note 6)	$\theta_{JC(TOP)}$	18	°C/W
Junction−to−Board Heat Spreader, Thermal Resistance (Note 6)	θ_{JB}	1.0	°C/W
Junction−to−Case (Top), Measurement Reference (Note 6)	Ψ_{J-CT}	1.1	°C/W
Moisture Sensitivity Level QFN Package	MSL	1	

6. JEDEC JESD 51−7 with 0 LFM

ELECTRICAL CHARACTERISTICS ($-10°C < T_A < 100°C$; $4.75\ V < V_{CC} < 5.25\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Voltage Range		4.75	–	5.25	V
Quiescent Current	PS0	–	31	–	mA
	PS1	–	26	–	mA
	PS2	–	21	–	mA
	PS3	–	17	–	mA
	PS4	–	–	79	μA
	Enable Low	–	–	64	μA
UVLO Threshold	VCC Rising	–	–	4.5	V
	VCC Falling	4.1	–	–	V
	VCC UVLO Hysteresis	–	100	–	mV
VRMP					
VIN Supply Range	VRMP range prior to external voltage divider resistor network with 1/12 ratio	4.5	–	21	V
UVLO Threshold	VRMP Rising	–	–	0.355	V
	VRMP Falling	0.250	–	–	V
ENABLE INPUT					
Upper Threshold	Activation Level	0.8	–	–	V
Lower Threshold	Deactivation Level	–	–	0.3	V
PHASE DETECTION					
CSP Pin Threshold Voltage		VCC – 0.4	–	–	V
Phase Detect Timer		–	1.5	–	ms
IMVP9.1 DAC (PROTOCOL 0Eh)					
System Voltage Accuracy	0 V < DAC < 0.495 V (25°C only)	–10	–	10	mV
	0.5 V < DAC < 0.745 V (25°C only)	–8	–	8	mV
	0.75 V < DAC (25°C only)	–0.5	–	0.5	%
DAC SLEW RATE					
Soft Start Slew Rate		–	1/4 fast	–	mV/μs
Slew Rate Slow		–	1/4 fast	–	mV/μs
Slew Rate Fast	Resistor Selectable (See Table 4)	–	>10	–	mV/μs
VOFS Slew Rate		–	1/4 fast	–	mV/μs
DRON					
Output High Voltage	Sourcing 1 mA	3	–	–	V
Output Low Voltage	Sinking 1 mA	–	–	0.1	V
TSENSE					
TSENSE Bias Current		115.5	120	124.5	μA
Alert#	Assert Threshold	–	486	–	mV
	De–Assert Threshold	–	548	–	mV
VR_HOT	Assert Threshold	–	448	–	mV
	De–Assert Threshold	–	511	–	mV
VRSHDN	Assert Threshold	–	185	–	mV
VR_RDY OUTPUT					
VR_RDY Rise Time	1 kΩ pull–up to 3.3 V CTOT = 45 pF	–	110	150	ns
VR_RDY Fall Time		–	20	150	ns

ELECTRICAL CHARACTERISTICS ($-10°C < T_A < 100°C$; $4.75\ V < V_{CC} < 5.25\ V$; $C_{VCC} = 0.1\ \mu F$ unless otherwise noted) (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
VR_RDY Output Voltage Low	$I_{VR\_RDY} = -4$ mA	–	–	0.3	V
SVID (SDIO and SCLK)					
SVID Voltage Low Level	VIL (Note 7)	–	–	0.45	V
SVID Voltage High Level	VIH (Note 7)	0.65	–	–	V
SVID Pull Down Resistance	(Note 8)	–	4	–	Ω
SDIO Output Low Voltage	VOL	–	–	0.3	V
SVID Clock to Data Delay	TCO (Note 8)	–	–	12	ns
SVID Setup Time	(Note 8)	7	–	–	ns
SVID Hold Time	(Note 8)	14	–	–	ns
Input Capacitance	(Note 8)	–	5	–	pF
ALERT#					
VOL (Output Low)		–	–	0.3	V
OVP AND UVP					
Absolute Over Voltage Threshold	10 mV DAC step During Soft Start – CSREF Rising	3.3	3.44	3.6	V
	5 mV DAC step During Soft Start – CSREF Rising	2.4	2.5	2.6	V
Over Voltage Threshold Above DAC	VSP–VSN–VID Rising	350	400	475	mV
Over Voltage Delay	VSP–VSN Rising to PWM Low		50		ns
Under Voltage Threshold Below DAC–DROOP (VUVM)	VSP–VSN–VID Falling	–440	–400	–360	mV
Under Voltage Delay		–	5	–	μs
PWM OUTPUT					
Output High Voltage	Sourcing 500 μA	$V_{CC} - 0.2$	–	–	V
Output Mid Voltage	No Load, Power State 2	1.7	1.8	1.9	V
Output Low Voltage	Sinking 500 μA	–	–	0.7	V
DIFFERENTIAL AMPLIFIER					
Input Bias Current	VSP = 1.3 V	200	–	500	nA
–3 dB Bandwidth	CL = 20 pF, RL = 10 kΩ	–	22.5	–	MHz
Closed Loop DC Gain	VSP – VSN = 0.5 V to 1.3 V	–	1	–	V/V
ERROR AMPLIFIER					
Input Bias Current	Input = 1.3 V	–400	–	400	nA
DC Gain	CL = 20 pF, RL = 10 kΩ	–	80	–	dB
–3 dB Bandwidth	CL = 20 pF, RL = 10 kΩ	–	20	–	MHz
Slew Rate	ΔVin = 100 mV, G = –10 V/V, ΔVout = 1.5 V to 2.5 V, CL = 20 pF, RL = 10 kΩ	–	5	–	V/μs
OVER–CURRENT PROTECTION (ILIM)					
ILim Threshold Current Immediately, OCP_L/VRHOT# Asserts	ICL0 – PS0 Operation	8	9	10	μA
	ICL1 – PS1, PS2, PS3 Operation (Note 9)	–	9/N	–	μA
ILim Threshold Current (Delayed OCP shutdown)	ICLM0 – PS0 Operation	11	13	15	μA
	ICLM1 – PS1, PS2, PS3 Operation (Note 9)	–	13/N	–	μA
Shutdown Delay	Immediate	–	650	–	ns
	Delayed	–	20	–	μs

ELECTRICAL CHARACTERISTICS (–10°C < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF unless otherwise noted) (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
IOUT OUTPUT					
Current Gain	IOUT/ILIM (RLIM = 20 kΩ, RIOUT = 5 kΩ, Vout = 0.8 V, 1.25 V, 1.52 V)	9.5	10	10.5	A/A
PWM GENERATOR					
PWM Minimum Pulse Width		–	40	–	ns
0% Duty Cycle	Comp Voltage for PWM Held Low	–	1.3	–	V
100% Duty Cycle	Comp Voltage for PWM Held High VIN at 4.5 V	–	1.75	–	V
	Comp Voltage for PWM Held High VIN at 21 V	–	3.4	–	
CURRENT SUMMING AMPLIFIER (CSAMP)					
Offset Voltage		–500	–	500	μV
Input Bias Current	CSSUM = CSREF = 1.0 V	–10	–	10	μA
Open Loop Gain		–	80	–	dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF to GND, R_L = 10 kΩ to GND	–	10	–	MHz
CURRENT BALANCE AMPLIFIER					
Differential Mode Input Voltage Range	CSREF = 1.2 V	–100	–	100	mV
PSYS					
Full Scale Input Voltage		–	2.5	–	V
Disable Threshold		–	VCC – 0.4	–	V
I^2C (SDA AND SCL)					
High Input Voltage (V_{IH})	V_{TT_I2C} is the I^2C (SDA & SCL) Termination Voltage, 1.71 V ≤ V_{TT_I2C} ≤ 5.25 V (Note 10)	0.65 * V_{TT_I2C}	–	–	V
Low Input Voltage (V_{IL})		–	–	0.35 * V_{TT_I2C}	V
Hysteresis	(Note 10)	–	120	–	mV
Output Low Voltage	I_{PULLUP} = 3 mA	–	–	0.4	V
Input Current		–10	–	–	μA
Input Capacitance	SDA and SCL	–	5	–	pF
Clock Frequency		–	–	400	kHz
SCL Falling Edge to SDA Valid Timing	(Note 8)	–	–	1	μs

7. Tested at 25°C / 5 V VCC only.
8. Guaranteed by characterization, not production tested.
9. N is the phase configuration number in PS0.
10. Guaranteed by design, not production tested.

Start Up

Following the rise of VCC above the UVLO threshold, externally programmed configuration data is collected, and all PWM outputs are set to Mid−level to prepare the gate drivers of the power stages for activation. When the controller is enabled, DRON is asserted (high) to activate the external gate drivers. A digital counter steps the DAC up from zero to the target boot voltage based on the Soft Start Slew Rate in the spec table. As the DAC ramps, the PWM outputs of each rail will change from Mid−level to high when the first PWM pulse for that rail is produced. When the controller is disabled, the PWM signals return to Mid−level. The VR_RDY signal is asserted when the controller is ready to accept the first SVID command.

TIMING DIAGRAMS

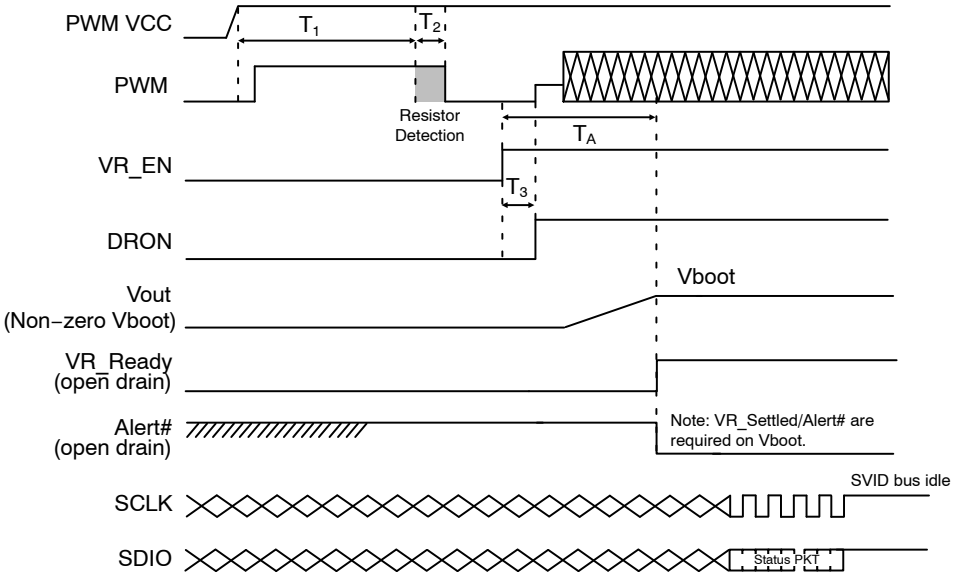


Figure 4. IMVP9.1 Start−Up Timing Diagram (With PWM resistor detection and DRON)

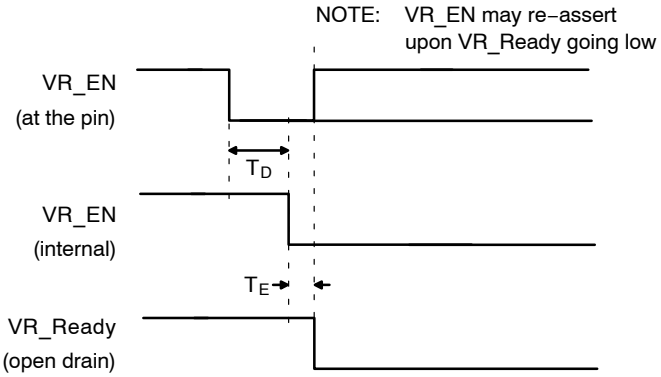


Figure 5. Shut−Down Timing Diagram

Table 1. START−UP AND SHUT−DOWN TIMING

Description		Min	Typ	Max	Unit
TA	VR_EN to VR_Ready. Controller ready to accept SVID command	−	−	2.5	ms
TD	External de−assertion of VR_EN to the internal recognition of VR_EN de−assertion (glitch filter)	0	−	1	μs
TE	VR_EN internal de−assertion to VR_Ready de−assertion	−	−	500	ns
T1	VCC rise over UVLO to configured resistor detection begin	−	1.5	−	ms
T2	Configured resistor detection time	−	100	−	μs
T3	VR_EN to DRON	−	117	−	μs

DEVICE CONFIGURATION

Phase and Rail Configuration

During start−up, the number of operational phases of the multiphase rail is determined by the internal circuitry monitoring the CSP inputs. If a reduced phase count is required, the appropriate CSP pins should be externally pulled to VCC with a resistor during startup. Also, whether or not the PSYS function is active and responds to an address call on the SVID bus is determined by the internal circuitry monitoring the PSYS input. Tying the PSYS input to VCC will cause the PSYS rail to not respond to any calls to address 0Dh on the SVID bus.

Basic Configuration

The controller has four basic configuration features. On power up a 10 μA current is sourced from these pins through a resistor connected to this pin and the resulting voltage is measured. The following features will be programmed:

- SVID Address
- Slew Rate
- V_{BOOT}
- Output Voltage Step

SVID address and slew rate options are shown in Table 4.

V_{BOOT} and output voltage step options are shown in Table 6.

ASP2100R Fast V−Mode

VR_HOT assertion for Fast V−Mode on/off selection as shown in Table 5. Fast V−Mode is only supported on the ASP2100R.

Switching Frequency

Switching frequencies between 180 kHz and 1.17 MHz are programmed on power up with pulldown resistors on the Rosc and RoscA pins. Switching frequency options are shown in Table 9. The Main Rail follows the configuration number in PS0. The A rail follows 1−phase switching frequency setting.

ICCMAX

The SVID interface provides the platform ICCMAX values for each rail, at register 21h. Resistors to ground on the PWM3/ICCMAX, PWM1A/ICCMAXA and PWM6/ICCMAX_AUXIN pins program these registers. On power up, 10 μA is sourced from these pins to generate voltages on the program resistors. The values of the registers are set by the equation below. The resistor values should be no less than 10 kΩ.

$$ICC_{MAX_{21h}} = \frac{R \times 10\ \mu A \times 255}{2.5\ V} \qquad \text{(eq. 1)}$$

ICCMAX Additional Capability

IMVP9.1 adds an option to extend the current range of the main rail by scaling the LSB size of register $ICCMAX_{21h}$ by $2^{ICCMAX\_ADD_{50h}[1:0]}$ amps (See Table 2). On the ASP2100 and ASP2100R, these register bits can be configured to 2 A per bit by enabling ICC*2_MAIN_RAIL mode. See Table 6 for details on how to enable this mode.

Table 2. ICCMAX CAPABILITY SCALING

$ICCMAX\_ADD_{50h}[4:0]$		ICC Scaling	Power Scaling
Power [4:2]	Current [1:0]		
010	00	1 A / bit	4 W /bit
011	01	2 A / bit	8 W / bit

When ICC*2_MAIN_RAIL mode is enabled, the bits ICCMAX_ADD50h[1:0] are set to 01b to indicate a scaling of 2 A per bit. This scaling applies to both the ICCMAX21h and the IOUT_H15h SVID registers. The bits ICCMAX_ADD50h[4:2] are also set to 011b to indicate that the POUT_H18h register value is scaled to 8 W per bit. See SVID register ICCMAX_ADD50h description in Table 19 for more details. Table 3 shows the rail configurations when ICC*2_MAIN_RAIL mode is enabled or disabled.

Table 3. RAIL SETTINGS FOR ICC*2_MAIN_RAIL MODE

		ICC*2_MAIN_RAIL	
		Disabled	Enabled
Main Rail	$ICCMAX_{21h}$ LSB Size	1 A	2 A
	$IOUT_{15h}$ LSB Size	1 A	2 A
	$POUT_{18h}$ LSB Size	4 W	8 W
	$HIGHPOWER\_ICCMAX\_ADD_{50h}[1:0]$	00	01
	$HIGHPOWER\_ICCMAX\_ADD_{50h}[4:2]$	010	011
	Default Loadline Weighting	50%	100%
A Rail	$ICCMAX_{21h}$ LSB Size	1 A	
	$IOUT_{15h}$ LSB Size	1 A	
	$POUT_{18h}$ LSB Size	4 W	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}[1:0]$	00	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}[4:2]$	010	
	Default Loadline Weighting	50%	
VCCIN_AUX	$ICCMAX_{21h}$ LSB Size	1 A	
	$IOUT_{15h}$ LSB Size	1 A	
	$POUT_{18h}$ LSB Size	4 W	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}[1:0]$	00	
	$HIGHPOWER\_ICCMAX\_ADD_{50h}[4:2]$	010	

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

CCM/DCM Operation

In PS0, all rails operate in Continuous Conduction Mode (CCM) which uses the dual−edge control methodology. However, if PS0 is configured as one−phase instead of multi−phase, the control methodology changes to RPM operation. RPM has great transient performance in one−phase CCM operation. The RPM frequency average DC value is targeted to be similar to the PS0 Dual Edge frequency. However, the switching frequency of RPM depends on input voltage, output voltage, load current, inductor value, and output capacitor value.

In PS2 and PS3, all rails will operate in either Continuous Conduction Mode (CCM) or discontinuous Conduction Mode (DCM) depending on load current in order to prevent loss of efficiency from negative inductor current.

Table 4. ASP2100 SVID ADDRESS AND SLEW RATE

Resistor (kΩ)	SR (mV/μs)	Main Rail SVID Address	A Rail SVID Address
10	10	00	01
14	30	00	01
18.7	48	00	01
24.3	10	01	00
30.9	30	01	00
38.3	48	01	00
47.5	10	00	02
59	30	00	02
71.5	48	00	02
86.6	10	01	02
105	30	01	02
127	48	01	02

Table 5. ASP2100R SVID ADDRESS, SLEW RATE AND FAST V−MODE

Resistor (kΩ)	SR (mV/μs)	Main Rail SVID Address	A Rail SVID Address	VR_HOT Assertion Fast V−Mode
10	10	0	1	ON
14	30	0	1	ON
18.7	48	0	1	ON
24.3	10	0	1	OFF
30.9	30	0	1	OFF
38.3	48	0	1	OFF
47.5	10	0	2	ON
59	30	0	2	ON
71.5	48	0	2	ON
86.6	10	0	2	OFF
105	30	0	2	OFF
127	48	0	2	OFF

Table 6. V_{BOOT} AND OUTPUT VOLTAGE STEP

Resistor (kΩ)	V_{BOOT} (V) Main Rail	V_{BOOT} (V) A Rail	Output Voltage Step
10	0 V	0 V	Both rails 5 mV/step
14	0 V	1.05 V	
18.7	1.05 V	0 V	
24.3	1.05 V	1.05 V	
30.9	0 V	0 V	Both rails 10 mV/step
38.3	0 V	1.8 V	
47.5	1.8 V	0 V	
59	1.8 V	1.8 V	
71.5	0 V	0 V	Main rail 5 mV/step. A rail 10 mV/step.
86.6	0 V	1.8 V	
105	1.05 V	0 V	
127	1.05 V	1.8 V	
154	0 V	0 V	Main rail 10 mV/step. A rail 5 mV/step.
187	1.8 V	0 V	
221	0 V	1.05 V	
280	1.8 V	1.05 V	

Table 7. POWER STATES

SVID Power State	Typical Operating Mode
PS0	Multiphase rail dual edge
PS1	One−phase CCM RPM
PS2	One−phase DCM RPM
PS3	One−phase DCM RPM
PS4	Standby

PSYS

The PSYS pin is an analog input to the VR controller. PSYS is a system input power monitor that facilitates the monitoring of the total platform system power. The system power is sensed at the platform charging device, the VR controller facilitates reporting back current and through the SVID interface at address 0Dh.

AUX_IN

The AUX_IMON current monitor input is a means of measuring the VCCIN_AUX platform VR output current using the IMVP9.1 ADC. This input is used to digitize the VCCIN_AUX output current information, which is sent to the IMVP9.1 PWM controller as an analog current mode signal proportional to the VCCIN_AUX output current. The signal is converted to a voltage at the IMVP9.1 controller input pin by a termination resistor, located at the controller. A resistor with high input impedance should be selected to avoid loading effects on the signal. The AUX Current reading is scaled by ICCMAX_AUXIN and can be read back on Register 0x15 of Rail 0x0D of the controller SVID bus.

Programming Pin

This is a multifunction select pin used to set the operation of multiple features and the combination of these features enabled/disabled. Items programmed on this pin are ICC*2_MAIN_RAIL which allows the user to select if the ICCMAX and IOUT reporting for the main rail is a 1 A or 2 A LSB step size. When off, the resolution is 1 A per LSB. When on, the resolution is set to 2 A per LSB which allows reporting of over 255 A on the main rail only.

Auto phase shedding can be enabled in PS0 mode in order to minimize power dissipation. Auto phase shedding is determined by the I^2C settings described in the Phase Shedding (Enable by I^2C) section and the I^2C register maps.

The other options include spread spectrum and acoustic noise solution. These programming pin functions must be enabled by the resistor setting shown in Table 8 before they can be enabled/disabled in I^2C.

Table 8. PIN OF ICC*2_MAIN_RAIL CONFIGURATION

Resistor (kΩ)	ICC*2 Main Rail	Acoustic Noise Solution	Spread Spectrum	Auto Phase Shedding
10	OFF	OFF	OFF	OFF
14	OFF	OFF	OFF	ON
18.7	OFF	OFF	ON	OFF
24.3	OFF	OFF	ON	ON
30.9	OFF	ON	OFF	OFF
38.3	OFF	ON	OFF	ON
47.5	OFF	ON	ON	OFF
59	OFF	ON	ON	ON
71.5	ON	OFF	OFF	OFF
86.6	ON	OFF	OFF	ON
105	ON	OFF	ON	OFF
127	ON	OFF	ON	ON
154	ON	ON	OFF	OFF
187	ON	ON	OFF	ON
221	ON	ON	ON	OFF
280	ON	ON	ON	ON

Table 9. SWITCHING FREQUENCY

Control by I^2C (Hex)	ROSC / ROSCA Control by Pin Resistor (kΩ)	Switching Frequency (kHz) (PS0 Number of Phases)		
		1 Phase~6 Phase	7 Phase	8 Phase
0000	10	180	180	180
0001	14	225	215	210
0010	18.7	270	250	240
0011	24.3	315	285	270
0100	30.9	360	320	300
0101	38.3	405	355	330
0110	47.5	450	390	360
0111	59	495	425	390
1000	71.5	540	460	420
1001	86.6	630	495	450
1010	105	720	530	480
1011	127	810	600	510
1100	154	900	700	540
1101	187	990	800	600
1110	221	1080	900	700
1111	280	1170	1000	800

THEORY OF OPERATION

Input Voltage Feed−Forward (VRMP Pin)

Ramp generator circuits are provided for the dual−edge modulator. The ramp generators implement input voltage feed−forward control by varying the ramp slopes proportional to the VRMP pin voltage. The VRMP pin also has a UVLO function, which is active only after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled. For multi−phase operation, the dual−edge PWM ramp amplitude is changed according to the following:

$$VRMP_{PP} = 0.1 \times V_{VRMP} \quad \text{(eq. 2)}$$

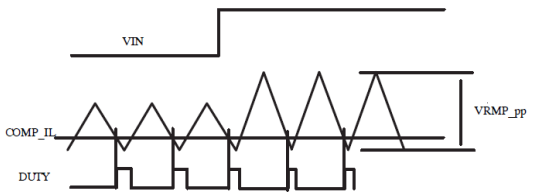


Figure 6. Ramp Feed Forward

An external voltage divider is required on this VRMP pin in order to scale the voltage seen on the VRMP pin the voltage divider on the pin needs to be setup to maintain a ratio of 1/12. Typical resistor values may include 1 MΩ Rup / 90.9 kΩ Rdown or 1.1 MΩ Rup / 100 kΩ Rdown. UVLO on VRMP is inactive in PS4 power state and PS3 when a VID to 0 V is received.

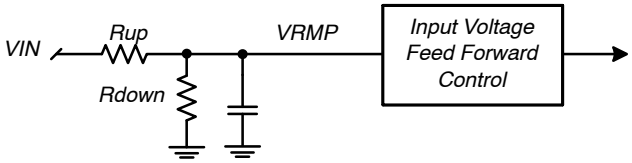


Figure 7. Ramp Feed Forward Circuit

Differential Current Feedback Amplifiers

Each phase of the rail has a low offset, differential amplifier to sense the current of that phase in order to balance current. The CSREF and CSPx pins are high impedance inputs, but it is recommended that any external filter resistor RCSN does not exceed 10 kΩ to avoid offset due to leakage current.

It is also recommended that the voltage sense element be no less than 0.5 mΩ for best current balance.

The external filter $RCSN_X$ and $CCSN_X$ time constant should match the inductor L/DCR time constant, but fine tuning of this time constant is generally not required. Phase current signals are summed with the COMP or ramp signals at their respective PWM comparator inputs in order to balance phase currents via a current mode control approach.

$$RCSN_X = \frac{L_{PHASE}}{CCSN_X \times DCR} \quad \text{(eq. 3)}$$

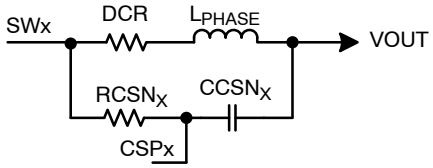


Figure 8. Per Phase Current Sense Network

Total Current Sense Amplifier

The multiphase rail uses a patented approach to sum the phase currents into a single, temperature compensated, total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The $RREF_X$ resistors average the voltages at the output terminals of the inductors to create a low impedance reference voltage at CSREF. The RPH_X resistors sum currents from the switch nodes to the virtual CSREF potential created at the CSSUM pin by the amplifier. The total current signal is the difference between the CSCOMP and CSREF voltages.

The amplifier filters, and amplifies, the voltage across the inductors in order to extract only the voltage across the inductor series resistances (DCR). An NTC thermistor (Rth) in the feedback network placed near the Phase 1 inductor senses the inductor temperature, and compensates both the DC gain and the filter time constant for the change in DCR with temperature. The Phase 1 inductor is chosen for the thermistor location so that the temperature of the inductor providing current in the PS1 power mode.

The DC gain equation for the DC total current signal is:

$$V_{CSCOMP} - V_{CSREF} = -\frac{R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}}{Rph} \times DCR \times I_{OUT} \quad \text{(eq. 4)}$$

Set the DC gain by adjusting the value of the Rph resistors in order to make the ratio of total current signal to output current equal the desired loadline. The values of Rcs1 and Rcs2 are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.

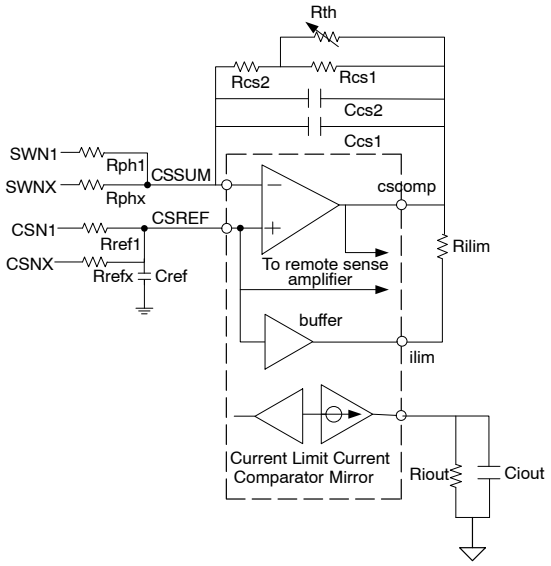


Figure 9. Total Current Sense Amplifier

The pole frequency of the CSCOMP filter should be set equal to the zero of the output inductor. This causes the total current signal to contain only the component of inductor voltage caused by the DCR voltage, and therefore to be proportional to inductor current. Connecting Ccs2 in parallel with Ccs1 allows fine tuning of the pole frequency using commonly available capacitor values. It is best to perform fine tuning during transient testing.

$$F_Z = \frac{DCR_{25°C}}{2\pi \times L_{Phase}} \quad \text{(eq. 5)}$$

$$F_P = \frac{1}{2\pi \times \left(R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}\right) \times (C_{CS1} + C_{CS2})} \quad \text{(eq. 6)}$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier.

The value of the CREF capacitor (in nF) on the CSREF pin should be:

$$Cref = \frac{0.02 \times Rph}{Rref} \quad \text{(eq. 7)}$$

High Performance Voltage Error Amplifier

The Remote Sense Amplifier output feeds a Type III compensation network formed by the Error Amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote Sense Amplifier output.

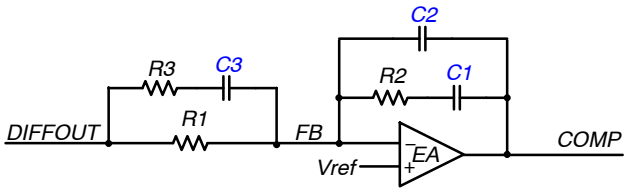


Figure 10. Error Amplifier

Loadline Programming (V_{DROOP})

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

A load line is produced by adding a signal proportional to output load current (V_{DROOP}) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. The load line is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.

$$V_{DROOP} = \frac{R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}}{Rph} \times DCR \times I_{OUT} \times \text{weighting} \quad \text{(eq. 8)}$$

Where the default weighting is 50% for A rail and Main rail when ICC*2_MAIN_RAIL = OFF and is 100% for Mail Rail when ICC*2_MAIN_RAIL = ON

Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense regulator output voltage. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage.

$$V_{DIFFOUT} = (V_{VSP} - V_{VSN}) + (1.3\ V - v_{DAC}) + (V_{DROOP} - V_{CSREF}) \quad \text{(eq. 9)}$$

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins for the main rail and ILIMA and CSCOMPA for the A−rail. For simplicity, only the main rail operation will be described. Refer to Table 10 for equivalent A−Rail parameters.

The multiphase rail generates a replica of the CSREF pin voltage at the ILIM pin, and compares the ILIM pin current

to ICL0 and ICLM0 (ICL1 and ICLM1 in PS1, PS2 and PS3). When enabled by setting I^{2}C register 0x1E[0]=1, if the ILIM pin current exceeds ICL0 (ICL1 for PS1, PS2, and PS3), the controller asserts OCP_L/VRHOT# immediately, but does not shut down. If the ILIM pin current exceeds ICLM0 (ICLM1 for PS1, PS2 and PS3), the rail latches off after a programmable delay (0x1B[7:5]). Set the value of the current limit resistor RILIM according to Equation 10 for the desired output current limit.

Table 10. OCP SETUP, CONTROL AND MONITORING

Description	Main Rail	A−Rail
R_{ILIM} resistor connection	CSCOMP to ILIM	CSCOMPA to ILIMA
OCP_L Current (PS0) [Default = 9 μA]	ICL0	ICL0A
OCP_L Current (PS1, PS2, PS3) [Default = 1.125 μA]	ICL1	ICL1A
Total OCP Enable	0x1D[3]	0x39[3]
OCP_L OCP Ratio I2C Register, [Default = 90%]	0x19[3:1]	0x37[3:1]
OCP_L Hysteresis Ratio Bit, ['0' = 10%, '1' = 20%]	0x19[0]	0x37[0]
OCP_L Enable Bits, ['0' = OFF, '1' = ON]	0x1E[0]	0x3A[0]
OCP Current (PS0) [Default = 13 μA]	ICLM0	ICLM0A
OCP Current (PS1, PS2, PS3) [Default = 1.625 μA]	ICLM1	ICLM1A
OCP Ratio I^{2}C Register, [Default = 130%]	0x19[7:4]	0x37[7:4]
Total OCP Delay, [Default = 20 μs]	0x1B[7:5]	
Total OCP Single Phase threshold, ['0' = 100%, '1' = 200%]	0x22[5]	0x3B[5]
Total OCP Indicator	0x18[7]	0x36[5]

The OCP_RATIO can be independently set for both the immediate (OCP_L) limit and the delayed OCP limit by modifying the respective I^{2}C 0x19[3:1] and 0x19[7:4] bit fields.

$$R_{ILIM} = \frac{R_{CS2} + \frac{R_{CS1} \times R_{TH}}{R_{CS1} + R_{TH}}}{R_{PH}} \times \frac{DCR \times I_{LIM}}{10\mu A \times OCP\_RATIO} \quad \text{(eq. 10)}$$

This equation sets the current limit when all phases are active. When the number of active phases is reduced, either by auto phase shedding or by entering the PS1, PS2, or PS3 power states, the OCP current limit is reduced according to Equation 11.

$$I_{LIM\ ACTIVE} = I_{LIM} \times \frac{\text{Active Phases}}{\text{Total Phase Count}} \quad \text{(eq. 11)}$$

For example:

OCP is set to 240 A on the 8 phase rail. If only a single phase is active, then the OCP limit automatically scales to 240 A x 1/8= 30 A. If 4 phases are active, then the OCP limit is 120 A.

Programming IOUT

The IOUT pin sources a current proportional to the ILIM current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2.5 V signal on IOUT.

$$R_{IOUT} = \frac{2.5\ V \times R_{LIMIT}}{10 \times \frac{R_{CS2} + \frac{R_{CS1} \times Rth}{R_{CS1} + Rth}}{Rph} \times DCR \times ICCMAX} \quad \text{(eq. 12)}$$

Programming DAC Feed−Forward Filter

The multiphase rail outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. This current is scaled with the load line setting from registers 0x0D and 0x0E for the main rail and 0x2E for the A rail.

A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, to compensate for the response of the DROOP function to the current flowing into the charging output capacitors. In the following equations, COUT is the total output capacitance of the system.

It is recommended that the highest load line weighting for the highest desired load line be used. This allows the DAC feed−forward current to optimally scale with the load line weight adjustments.

$$C_{FF} = 2.2\ nF \quad \text{(eq. 13)}$$

$$R_{FF} = Cout \times LL/C_{FF} \quad \text{(eq. 14)}$$

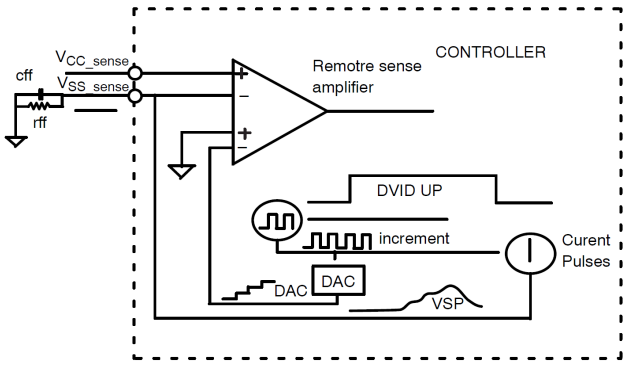


Figure 11. DAC Feed Forward

TSENSE Network

A temperature sense input is provided for each rail. A precision 120 μA current is sourced from the TSENSE & TSENSEA pins to generate a voltage on the temperature sense networks. The voltages on the temperature sense inputs are sampled by the internal A/D converter and compared to the threshold registers. A 100k NTC such as the Murata NCU18WF104F6SRB should be used and connected as shown in Figure 12. R_{COMP1} & R_{COMP2} are used to linearise the network response over the temperature range from 25°C to 106°C. Recommended values are 300 Ω and 13.7 kΩ respectively when the NCU18WF104F6SRB is used. A 100 nF filter cap, located near the controller, should also be used.

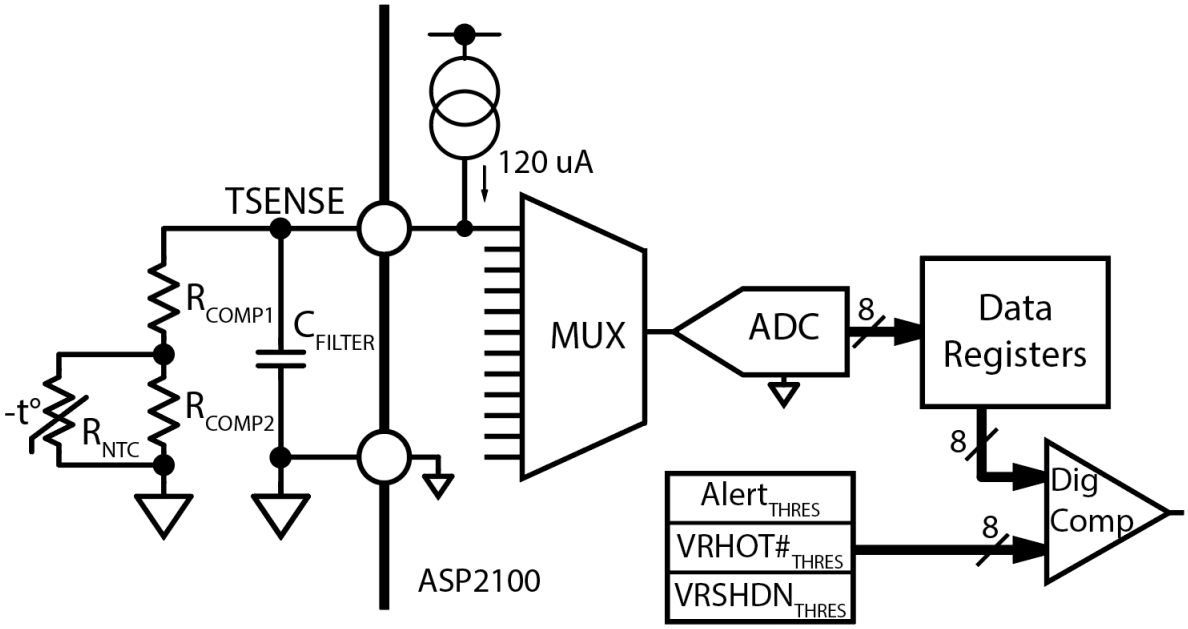


Figure 12. TSENSE Network

The Alert, VRHOT# and VRSHDN thresholds can be programmed over I^2C for the Main and A−rails using the following registers.

Table 11. TSENSE and TSENSEA I^2C REGISTERS

Threshold	Main Rail	A−Rail	Default Value
Alert	0x59[7:4]	0x59[3:0]	0x03
VRHOT#	0x22[3:0]	0x3B[3:0]	0x04
VRSHDN	0x20[7:4]	0x21[7:4]	0x07

The typical threshold values are shown in Table 12. The temperature values are related to the ideal response given in Equation 15.

$$T_{TH} = \left(1 - \frac{V\_TH}{1.8\ V}\right) \times 140^{\circ}C \qquad \text{(eq. 15)}$$

Table 12. TSENSE & TSENSEA THRESHOLD VOLTAGES

Register Value		VRSHDN		VRHOT#/Alert			
Dec	Hex	$V_{THASSERT}$ [mV]	Temp [°C] (Note 11)	$V_{THASSERT}$ [mV]	Temp [°C] (Note 11)	$V_{THDEASSERT}$ [mV]	Temp [°C] (Note 11)
0	0x00	365	112	603	93	666	88
1	0x01	340	114	564	96	627	91
2	0x02	315	116	526	99	589	94
3	0x03	290	118	487	102	548	97
4	0x04	260	120	448	105	511	100
5	0x05	235	122	408	108	471	103
6	0x06	210	124	368	111	433	106
7	0x07	185	126	329	114	394	109
8	0x08	159	128	292	117	355	112
9	0x09	129	130	251	120	316	115
10	0x0A	105	132	214	123	277	118
11	0x0B	80	134	175	126	238	121
12	0x0C	54	136	135	129	199	125
13	0x0D	24	138	97	132	160	128
14	0x0E	2	140	57	136	121	131
15	0x0F						

11. Temperatures shown relate to an ideal temperature characteristic.

$$T_{TRIP} = \left(1 - \frac{V_{TH}}{1.8\ V}\right) \times 140°C$$

These values match the recommended threshold values for temperatures up to 106°C to within ±3°C. For temperatures above 106°C, the NTC, R_{COMP1}, R_{COMP2}, and I^2C threshold values must be adjusted to achieve the desired trip point using Equation 16.

$$V_{TH} = \left(R_{COMP1} + \frac{R_{COMP2} \times R_{NTC}}{R_{COMP2} + R_{NTC}}\right) \times 120\ \mu A \quad \text{(eq. 16)}$$

Where R_{NTC} is the NTC resistance at the desired temperature.

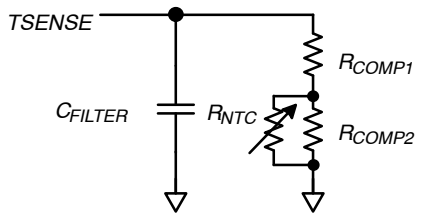


Figure 13. TSENSE Network

PWM Comparators

The noninverting input of each comparator (one for each phase) is connected to the summation of the error amplifier output (COMP) and each phase current (IL x DCR x Phase Balance Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output. During steady state PS0 operation, the main rail PWM pulses are centered on the valley of the triangle ramp waveforms and both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the error amp signal increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

I²C Address

In addition to the SVID interface between the CPU and VR, the controller also supports communication via I²C over the I²C. The I²C interface consists of SDA and SCL. Communication over I²C can occur once VCC is ready (even prior to enabling the controller), however, you should wait a minimum of 5 ms after VCC is ready before communicating. I²C address can be configured through hardware pin.

Table 13. I²C SLAVE ADDRESS CONFIGURATION

Resistor (kΩ)	Device I²C Slave Address
10	20h
14	21h
18.7	22h
24.3	23h
30.9	24h
38.3	25h
47.5	26h
59	27h
71.5	28h
86.6	29h
105	2Ah
127	2Bh
154	2Ch
187	2Dh
221	2Eh
280	2Fh

Output Voltage Offset (VOFS)

According to Intel definition, output voltage offset can be implemented through SVID. I²C also provides flexibility to change VOFS. There are four possibilities to change output voltage offset. For the default setting, VOFS is controlled by SVID. It can also be controlled by I²C register and ignored SVID setting. When phase shedding feature enable, VOFS can also be adjusted depend on output load.

Phase Shedding (Enable by I²C)

The phase shedding feature can be implement by I²C. The main rail it supports three adjustable current threshold, VM0~VM2. And four current stage, LCS0~LCS3, can set each phase number, offset voltage, load−line, and switching frequency. The A rail supports one adjustable current threshold, VM0. Two current stages, LCS0 and LCS1, can also separate their phase number, offset voltage, load−line, and switching frequency.

Phase shedding is enabled when the programming pin (see Table 8), the Power State Control bit and the Auto Phase Function Control bit are all enabled. For the main rail, the Power Stage Control bit is 0x1D[5] and the Auto Phase Function Control bit is 0x1E[4]. For the A rail, the Power Stage Control bit is 0x39[5] and the Auto Phase Function Control bit is 0x3A[4].

Table 14. OUTPUT VOLTAGE OFFSET (VOFS) OF MAIN RAIL

VOFS of Main Rail		0x1D[4] OFS Control	
		0 (Follow SVID)	1 (Ignore SVID)
0x1E[5] I²C VOFS	0 (Disable)	SVID 0x33	I²C 0x27
	1 (Enable)	SVID 0x33 + I²C 0x07~0x0A (Depend on phase shedding setting)	I²C 0x27 + I²C 0x07~0x0A (Depend on phase shedding setting)

Table 15. OUTPUT VOLTAGE OFFSET (VOFS) OF A RAIL

VOFS of A Rail		0x39[4] OFS Control	
		0 (Follow SVID)	1 (Ignore SVID)
0x3A[5] I²C VOFS	0 (Disable)	SVID 0x33	I²C 0x40
	1 (Enable)	SVID 0x33 + I²C 0x2B~0x2C (Depend on phase shedding setting)	I²C 0x40 + I²C 0x2B~0x2C (Depend on phase shedding setting)

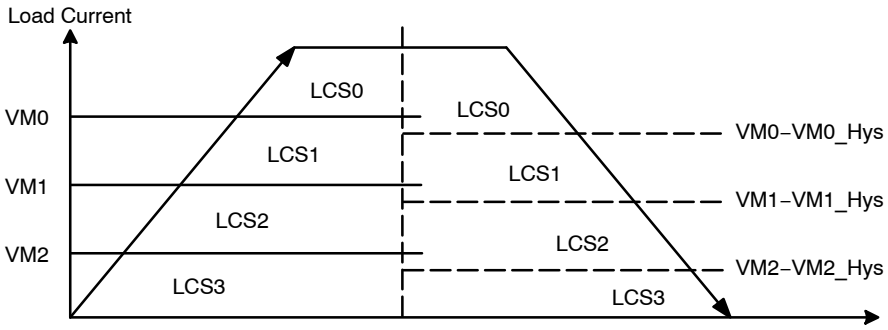


Figure 14. Phase Shedding for Main Rail

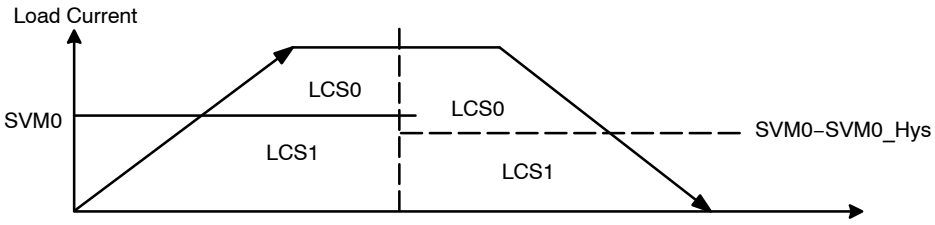


Figure 15. Phase Shedding for A Rail

Table 16. PHASE CONFIGURATION

Phase Configuration	Programming Pin in CSPx	Unused Pin
8 + 2	All CSP pins are connected normally	No unused Pin
7 + 2	CSP1 to CSP7 and CSP1A to CSP2A pins connected normally. CSP8 connected to VCC through a 2 kΩ resistor.	Float PWM8.
6 + 2	CSP1 to CSP6 and CSP1A to CSP2A pins connected normally. CSP7 connected to VCC through a 2 kΩ resistor.	Float PWM8 and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only.
5 + 2	CSP1 to CSP5 and CSP1A to CSP2A pins connected normally. CSP6 connected to VCC through a 2 kΩ resistor.	Float PWM8, CSP7, and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only. Use PWM6 for programming ICCMAX_AUXIN only.
4 + 2	CSP1 to CSP4 and CSP1A to CSP2A pins connected normally. CSP5 connected to VCC through a 2 kΩ resistor.	Float PWM8, CSP6, CSP7, and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only. Use PWM6 for programming ICCMAX_AUXIN only. Use PWM5 for programming ROSCA only.
3 + 2	CSP1 to CSP3 and CSP1A to CSP2A pins connected normally. CSP4 connected to VCC through a 2 kΩ resistor.	Float PWM8, CSP5, CSP6, CSP7, and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only. Use PWM6 for programming ICCMAX_AUXIN only. Use PWM5 for programming ROSCA only. Use PWM4 for programming ROSC only.
2 + 2	CSP1 to CSP2 and CSP1A to CSP2A pins connected normally. CSP3 connected to VCC through a 2 kΩ resistor.	Float PWM8, CSP4, CSP5, CSP6, CSP7, and CSP8. Use PWM7 for programming ICC*2_MAIN_RAIL only. Use PWM6 for programming ICCMAX_AUXIN only. Use PWM5 for programming ROSCA only. Use PWM4 for programming ROSC only. Use PWM3 for programming ICCMAX only.
8 + 1	CSP1 to CSP8 and CSP1A pins connected normally. CSP2A connected to VCC through a 2 kΩ resistor.	Use PWM2A for programming I2C_ADDRESS only.
8 + 0	CSP1 to CSP8 pins connected normally. CSP1A connected to VCC through a 2 kΩ resistor.	Float PWM1A and CSP2A. Use PWM2A for programming I2C_ADDRESS only.

Table 17. PHASE SHEDDING CONFIGURATION

Main Rail Phase Configuration in PS0	Main Rail Phase Configuration when Phase Shedding Enable (I^2C 0x06, IICP0~IICP3)			
	"00"	"01"	"10"	"11"
8	8	4	2	1
7	7	4	2	1
6	6	4	2	1
5	5	3	2	1
4	4	3	2	1

FAULT PROTECTION

Over Current Protection (OCP)

A programmable total phase current limit is provided which shuts down the controller when a programmable timer expires. See section ”Programming the Current Limit” on page 16 for more details on this feature. To recover from an OCP fault, the EN pin or VCC voltage must be cycled low.

Input Under−voltage Lockouts (UVLO)

The VR monitors the 5 V VCC supply as well as the VRMP pin voltage. Hysteresis is incorporated within these monitors.

Output Under Voltage Monitor

The multiphase phase rail output voltage is monitored for under voltage at the output of the differential amplifier. If the multiphase−phase rail output falls more than VUVM2 below the DAC−DROOP voltage, the UVM comparator will trip – sending the VR_RDY signal low.

Output Over Voltage Protection

The multiphase phase output voltage is monitored for OVP at the VSP pin. During normal operation, if an output voltage exceeds the DAC voltage by VOVP, the VR_RDY flag goes low, and the DAC voltage of the overvoltage rail will be slowly ramped down to 0 V to avoid producing a negative output voltage. At the same time, the PWM outputs of the overvoltage rail are sent low. The PWM output will pulse to mid−level during the DAC ramp down period if the output decreases below the DAC + OVP threshold as DAC decreases. When the DAC gets to zero, the PWMs will be held low, and the VR will stay in this mode until the VCC voltage or EN is toggled.

Absolute OVP

During start up, the OVP threshold is set to the absolute over voltage threshold. This allows the controller to start up without false triggering OVP.

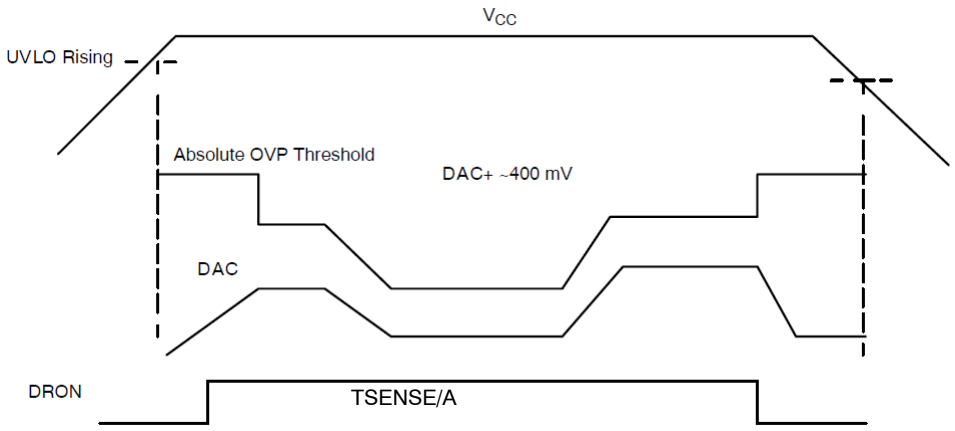


Figure 16. OVP Threshold Behavior

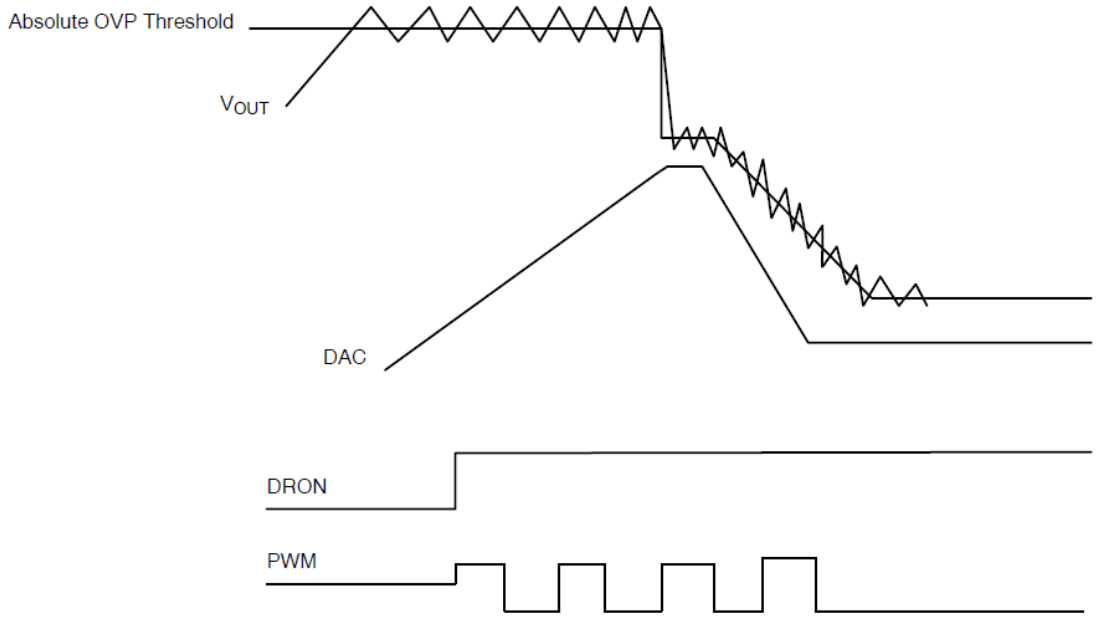


Figure 17. OVP Behavior at Start−up

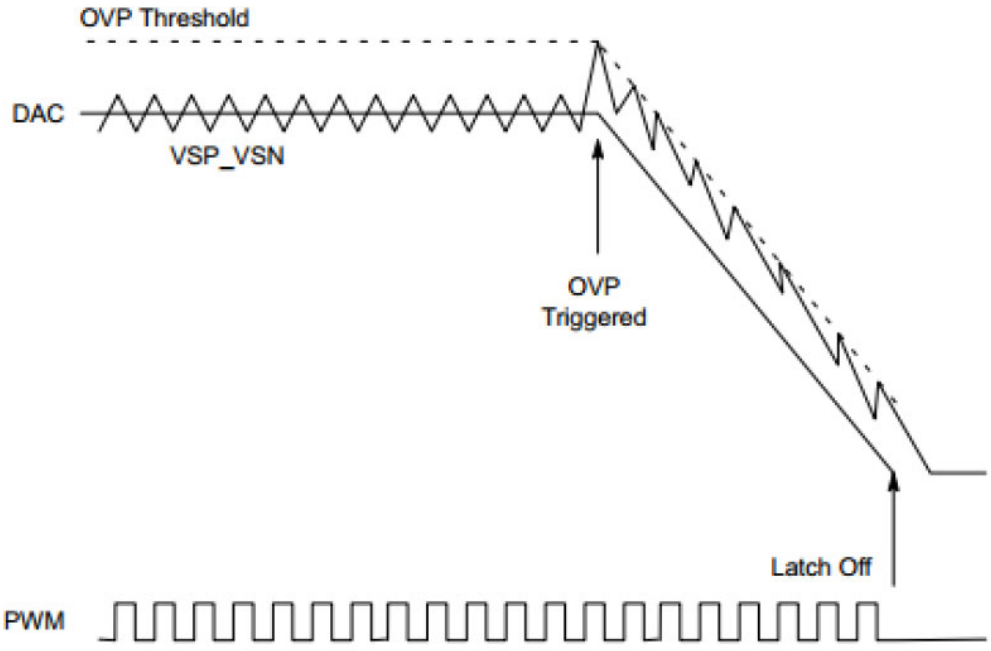


Figure 18. OVP During Normal Operation Mode

Serial VID Interface (SVID)

The Serial VID Interface (SVID Interface) is a 3 wire digital interface used to transfer power management information between the CPU (Master) and the VR controller (Slave). The 3 wires are clock (SCLK), data (SDIO) and ALERT#. The SCLK is unidirectional and generated by the master. The SDIO is bi−directional, used for transferring data from the microprocessor to the VR controller and from the VR controller to the CPU. The ALERT# is an open drain output from the VR controller to signal to the master that the Status Register should be read.

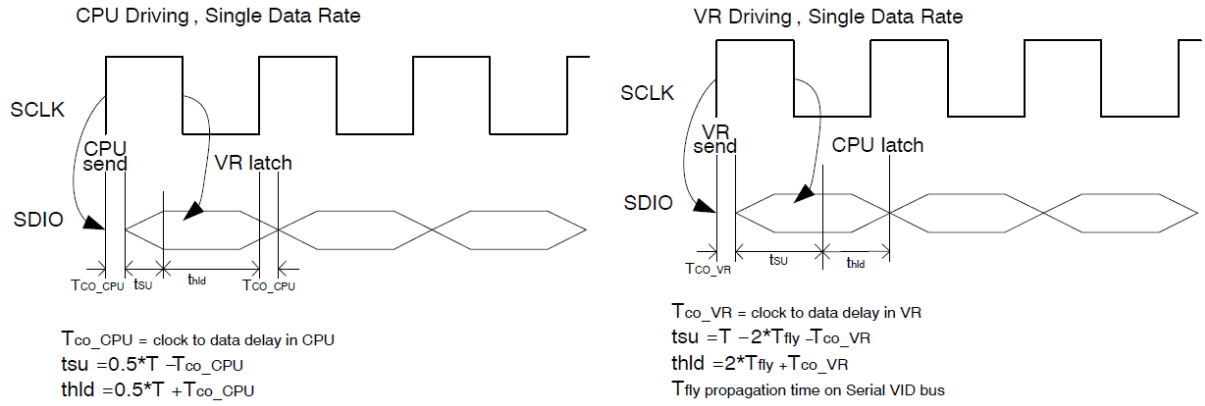


Figure 19. SVID Timing Diagram

Table 18. SLEW RATE

Option	SVID Command Code	Feature Description	Register Address (Indicating the Slew Rate of VID Code Change)
SetVID_Fast	01h	10 mV/μs, 30 mV/μs, or 48 mV/μs VID code change slew rate	24h
SetVID_Slow	02h	= 1/4 of SetVID_Fast VID code change slew rate	25h
SetVID_Decay	03h	No control, VID code down	N/A

Table 19. I²C REGISTERS FOR MAIN RAIL

Reg Addr	Register Name	Description	Access	Default
0x01	VM0[7:0]	Current threshold for LCS0 (highest current state) Resolution = (ICCMAX/255) A/bit	R/W	00h
0x02	VM1[7:0]	Current threshold for LCS1 Resolution = (ICCMAX/255) A/bit	R/W	00h
0x03	VM2[7:0]	Current threshold for LCS2 Resolution = (ICCMAX/255) A/bit	R/W	00h
0x04	VM0_HYST[5:3] VM1_HYST[2:0]	Bit[5:3]: Set VM0 Hysteresis, 8 steps VM0 Hys = (ICCMAX/100) x (2 + [5:3]) Bit[2:0]: Set VM1 Hysteresis, 8 steps VM1 Hys = (ICCMAX/100) x (2 + [2:0])	R/W	00h
0x05	VM2_HYST[5:3] SVM0_Hys_Arail[2:0]	Bit[5:3]: Set VM2 Hysteresis, 8 steps VM2 Hys = (ICCMAX/100) x (2 + [5:3]) Bit[2:0]: Set SVM0 Hysteresis, 8 steps SVM0 Hys = (ICCMAX/100) x (2 + [2:0])	R/W	00h
0x06	IICP3[7:6] IICP2[5:4] IICP1[3:2] IICP0[1:0]	*Number of phases active in each I²C state* Phase count while in I²C defined states Bit[7:6]: phases on in LCS3 Bit[5:4]: phases on in LCS2 Bit[3:2]: phases on in LCS1 Bit[1:0]: phases on in LCS0 00: 8 phases, 01: 4 phases, 10: 2 phases, 11: 1 phase 2 phases operate by PWM1 and PWM2. Note: 0x1D[5] & 0x1E[4] must be set to enable auto−phase shedding.	R/W	00h
0x07	VOFS0[7:0]	*Voltage Offset Adjustment* (Note 12) Offsets for I²C states LCS0 − LCS3 (5 mV/step). VOFS is 2's compliment, Bit 7 is sign bit. Voltage change slew rate is SLOW. Note: 0x1E[5] must be set to enable the voltage offset function	R/W	00h
0x08	VOFS1[7:0]		R/W	00h
0x09	VOFS2[7:0]		R/W	00h
0x0A	VOFS3[7:0]		R/W	00h
0x0B	IICF0[7:4] IICF1[3:0]	IICF0[7:4] = LCS0 operating frequency IICF1[3:0] = LCS1 operating frequency IICF2[7:4] = LCS2 operating frequency IICF3[3:0] = LCS3 operating frequency Refer to switching frequency configuration settings in Table 9. Note: 0x52[6] must be set to enable I²C frequency control	R/W	00h
0x0C	IICF2[7:4] IICF3[3:0]		R/W	00h
0x0D	IICLL0[7:4] IICLL1[3:0]	DC Load Line weighting in each I²C state LCS0 − LCS3 If ICC*2_MAIN_RAIL = OFF Range is 0% − 93.75% in 6.25% steps. (Default is 50%) If ICC*2_MAIN_RAIL = ON Range is 0% − 187.25% in 12.5% steps. (Default is 100%) Note: 0x1E[2] must be set to enable DC loadline adjustment	R/W	88h
0x0E	IICLL2[7:4] IICLL3[3:0]		R/W	88h
0x0F	CB_EN[7] PH1_IGAIN[6:4] PH2_IGAIN[2:0]	*Current Balance Gain* Adjustment CB_EN[7] = Enable/Disable current balance feature. Enable = 0 (Default), Disable = 1 PH1_IGAIN[6:4] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% PH2_IGAIN[2:0] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x10	PH3_IGAIN[6:4] PH4_IGAIN[2:0]	*Current Balance Gain* PH3_IGAIN[6:4] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% PH4_IGAIN[2:0] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h

Table 19. I²C REGISTERS FOR MAIN RAIL

Reg Addr	Register Name	Description	Access	Default
0x11	PH5_IGAIN[6:4] PH6_IGAIN[2:0]	*Current Balance Gain* PH5_IGAIN[6:4] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% PH6_IGAIN[2:0] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x12	PH7_IGAIN[6:4] PH8_IGAIN[2:0]	*Current Balance Gain* PH7_IGAIN[6:4] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% PH8_IGAIN[2:0] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x14	LCHVID[7:0]	Latch VID register – default = 1.1 V (ABh) Refer to IMVP9.1 SVID table. VDAC control by LCHVID when 0x1D[6] = “1”	R/W	ABh
0x15	IOUT[7:0]	8 bit ADC reading. Reads FFh when IOUT = ICCMAX	RO	–
0x16	VOUT_MSB[7:0]	Main Rail Voltage Reading, 8−bit MSB If 0x1E[6] = ”0”, VOUT = VDAC, 5mV/step If 0x1E[6] = ”1”, VOUT = Sense Voltage, 3.9 mV/step Note: Read this register before reading VOUT_LSB (0x17).	RO	–
0x17	VOUT_LSB[1:0]	Main Rail Voltage Reading, 2−bit LSB If 0x1E[6] = ”0”, VOUT = VDAC, 5 mV/step If 0x1E[6] = ”1”, VOUT = Sense Voltage, 3.9 mV/step. Note: Read VOUT_MSB (0x16) before reading this register.	RO	–

0x18	Protection Indicator[7:0]	*Protection Enable/Disable Indicator*
		Bit[7]: OCP Indicator
		0 = Not Active; 1 = Active
		Bit[6]: Per phase OCP Indicator
		0 = Not Active; 1 = Active
		Bit[5]: OVP Indicator
		0 = Not Active; 1 = Active
		Bit[4]: UVP Indicator
		0 = Not Active; 1 = Active
		Bit[3:0]: Per phase OCP indicator if Bit[6] = 1
		phase 1 = 0001; phase 2 = 0010;
		phase 3 = 0011; phase 4 = 0100;
		phase 5 = 0101; phase 6 = 0110;
		phase 7 = 0111; phase 8 = 1000;
		reserved = 1xxx
			RO	–

0x19	Total OCP[7:4] OCP_L[3:1] OCP_L Hys[0]	*Total OCP threshold, OCP_L flag assertion level and hysteresis setting* OCP[7:4]: Total Current OCP Ratio of ILIM (Over Current Protection) 0000: 50%; 0001: 60%; 0010: 70%; 0011: 80%; 0100: 90%; 0101: 100%; 0110: 110%; 0111: 120%; 1000: 130%(Default); 1001: 140%; 1010: 150%; 1011: 160%; 1100: 170%; 1101: 180%; 1110: 190%; 1111: 200% OCP_L[3:1]: OCP_L Ratio of ILIM (Over Current Protection) 000: 65%; 001: 70%; 010: 75%; 011: 80%; 100: 85%; 101: 90%(Default); 110: 95%; 111: 100% OCP_L Hys[0]: OCP_L Hysteresis Ratio of ILIM (Over Current Protection) 0: 10% (Default); 1: 20% Note: 0x1D[3] must be set to enable Total OCP threshold I²C setting	R/W	8Ah

Table 19. I²C REGISTERS FOR MAIN RAIL

Reg Addr	Register Name	Description	Access	Default
0x1A	IMONOvR[7:6] OC[5:4] UV[3:2] OV[1:0]	IMONOvR[7]: Overwrite SVID 0x15h (IMON) “1” = Enable; “0” = Disable IMONOvR[6]: Overwrite SVID 0x15h (IMON) “1” = 1/2; “0” = 1/4 OCP[5:4]: Per Phase OCP 00 = 400 mV; 01 = 500 mV (Default); 10 = 600 mV; 11 = 700 mV The lowest threshold for each phase is 400mV/amp gain. The default gain is 6 so this corresponds to 83 mV across CSPx/CSREF. Bit[3:2]: UVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV Bit[1:0]: OVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV	R/W	50h
0x1B	OCP_delay[7:0]	*OCP Delay Setting – Main & A share the same setting* OCP_delay[7:5]: Total OCP delay 000 = 5 μs; 001 = 10 μs; 010 = 15 μs; 011 = 20 μs (Default); 100 = 25 μs; 101 = 30 μs; 110 = 35 μs; 111 = 40 μs OCP_delay[4:2]: Per Phase OCP delay 000 = 2 μs; 001 = 4 μs; 010 = 6 μs (Default); 011 = 8 μs; 100 = 10 μs; 101 = 12 μs; 110 = 14 μs; 111 = 16 μs OCP_delay[1:0]: RESERVED	R/W	68h
0x1C	VR_SR[3:0] SVR_SR[7:4]	DVID slew rate. Range is from 8 mV/μs to 48 mV/μs. 0x0~0x5, 8 mV/μs~18 mV/μs, 2 mV/μs per step 0x6~0xF, 21 mV/μs~48 mV/μs, 3 mV/μs per step Note: 0x1D[7] must be set to enable I²C slew rate control using this register	R/W	33h
0x1D	Misc1[7:0]	Bit[7]: Slew Rate Control 0 = Select from pin 1 = Select from register Bit[6]: VDAC Control 0 = SVID 0x31 VDAC follow SVID 1 = SVID 0x31 VDAC ignore SVID. VDAC control by LCHVID Bit[5]: PWR State Control 0 = SVID 0x32 PWR state follow SVID 1 = SVID 0x32 PWR state ignore SVID. Phase control by I²C Bit[4]: OFS control 0 = SVID 0x33 Offset follow SVID 1 = SVID 0x33 Offset ignore SVID. Offset control by I²C (Note 12) Bit[3]: Total OCP Control 0 = Disable Total OCP function (OCPL# = H) 1 = Enable Total OCP function Bit[2]: Per−phase OCP Control 0 = Disable Per−phase OCP function 1 = Enable Per−phase OCP function Bit[1]: OVP Control 0 = Disable OVP function (VR_OVP# = H) 1 = Enable OVP function Bit[0]: UVP Control 0 = Disable UVP function 1 = Enable UVP function	R/W	0Fh
0x1E	Misc2[7:0]	Bit[7]: Spread Spectrum (Note 13) “0” to disable; “1” to enable Bit[6]: VOUT Voltage value select “0” for SVID register; “1” actual A/D Bit[5]: Output voltage offset control (Note 12) “0” to disable; “1” to enable Bit[4]: Auto phase function control (Note 13) “0” disable; “1” to enable If Bit[4] is 0, follow IICP0 if 1D[5] = 1; or follow SVID PS if 1D[5] = 0. This bit with function after 0x1D[5] = “1” Bit[3]: DCM enable when in 1 phase “0” always CCM; “1” DCM Bit[2]: Loadline enable “0” disables LL; “1” enables Bit[1]: USM/PSM selection when in DCM “0” enable PSM (pulse skip mode); “1” enables USM (ultrasonic mode) Bit[0]: OCP_L enable control “0” to disable; “1” to enable	R/W	9Ch

Table 19. I²C REGISTERS FOR MAIN RAIL

Reg Addr	Register Name	Description	Access	Default
0x1F	WD[7:5]	Watchdog timer, (Note: I²C watchdog timer expires, all I²C registers return to default settings.) Bit[7]: 1 = Enable; 0 = Disable Bit[6]: Reset I²C registers to default values (except for register 0x1F, this is independent of the watchdog timer). Bit[5]: Timer 0 = 800 ms; 1 = 1600 ms	R/W	00h
0x20	VRSHDN_TH[7:4]	Bit[7:4]: Main Rail VRSHDN Threshold Setting. See Table 12 for threshold values Bit[3:0]: Reserved	R/W	70h
0x22	VRSHDN_BH[7] VRSHDN_EN[6] OCPTH[5] VRHOT_ALERT_EN[4] TEMP_VRHOT#[3:0]	*Select Behavior of VRSHDN* Bit[7]: OTP behavior selection 0 = VRSHDN# go low only; 1 = controller shutdown only Bit[6]: OTP function enable/disable 0 = Disable; 1 = Enable Bit[5]: Total OCP threshold control when single phase operation. 0 = Default; 1 = Double Bit[4]: VRHOT# “0” = Enable; “1” = Disable Note: when VR_HOT is disabled ALERT will not assert and the Temp Status bit (SVID reg 0x10 bit) is not set. Bit[3:0]: VRHOT# Threshold See Table 12 for threshold values	R/W	04h
0x26	IMON_OFS[7:0]	IMON offset 2’s compliment value (positive and negative adjustment)	R/W	00h
0x27	DVID_OFS[7:0]	DVID offset function (2’s compliment, 5 mV step) Note: 0x1D[4] must be set to ”1” to enable this function (Note 12)	R/W	00h
0x41	VBOOT_ENABLE[7] VBOOT_VOLTAGE[6:0]	Bit[7]: VBOOT Operation ’0’ => VBOOT follows H/W resistor setting. (See Table 6) ’1’ => VBOOT follows I2C setting. Bits[6:0] VBOOT voltage setting ’0’ => VBOOT = 0 V ’N’, where 1 ≤ N ≤ 127 => VBOOT = 300 mv + VDAC_STEP X (2N − 11) VDAC_STEP is the output voltage step size as shown in Table 6.	R/W	00h
0x43	TM[7:0]	*I²C Thermal Monitor Value Reading.* Temperature reports in degree celsius (°C). To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resistor in parallel. NTC uses 100 kΩ under 25°C and B25/50 approximates 4250. Use 13.5 kΩ for parallel resistor and 0.3 kΩ for series resistor.	RO	–
0x52	ROSC_OFFSET_CTRL[7:0]	Bit[7]: Reserved Bit[6]: Control setting function (ROSC) “0” = Disable (follow H/W resistor setting) “1” = Enable (follow I²C setting) Bit[5]: ICC*2_MAIN_RAIL setting ”0” = Disable ”1” = Enable Bit[3]: Reserved Bit[2]: Control setting function (ROSCA) “0” = Disable (follow H/W resistor setting) “1” = Enable (follow I²C setting) Bit[1:0]: Reserved	R/W	0x20
0x55	AC_NOISE_SLOPE[5:4] AC_NOISE_MULTI_LOPE[3] AC_NOISE_SR[2:1] AC_NOISE_EN[0]	Bit[7:6]: Reserved Bit[5:4]: Acoustic noise set point to change DVID down slope “00” = Every 4 VID Steps for VID Down “01” = Every 8 VID Steps for VID Down “10” = Every 16 VID Steps for VID Down “11” = Every 32 VID Steps for VID Down Bit[3]: Acoustic noise multi slope on DVID Down “0” = Disable (Default); “1” = Enable Bit[2:1]: Acoustic noise slew rate control “00” = 1/2 (Default); “01” = 1/4; “10” = 1/8; “11” = 1/16 Bit[0]: Acoustic noise mode enable “0” = Disable; “1” = Enable (Note 13)	R/W	01h

Table 19. I²C REGISTERS FOR MAIN RAIL

Reg Addr	Register Name	Description	Access	Default
0x56	BST_CAP_LOW_TIME[5:4] BST_CAP_ON_DVID[3] BST_CAP_TIME[2] BST_CAP_PULSED[1] BST_CAP_EN[0]	Bit[7:6]: Reserved Bit[5:4]: Boost cap low time. ”00” = 400 ns, ”01” = 200 ns, ”10” = 800 ns, ”11” = 600 ns Bit[3]: Boost cap in parallel with DVID on VID up from low power state “0” = Disable; “1” = Enable Bit[2]: Shorter Boost Cap Refresh ”0” = when ps_exit_timer Eh; ”1” = when ps_exit_timer 7h Bit[1]: Boost cap low PS exit ”0” = Continuous Boosting when Phases are off ”1” = Boost Cap Refresh at PS Exit only Bit[0]: Boost Cap Mode Enable “0” = Disable “1” = Enable	R/W	0Bh
0x59	TEMP_ALERT#[7:4] STEMP_ALERT#[3:0]	Bit[s7:4]: Thermal Alert Threshold for Main Rail Bits[3:0] Thermal Alert Threshold for A−Rail See Table 12 for threshold values	R/W	33h
0x5A	ACTIVE_PHASE[7:0]	Real time active phase indicator for Main rail. ”1” = Active Bit[7]: Phase8 active indicator Bit[6]: Phase7 active indicator Bit[5]: Phase6 active indicator Bit[4]: Phase5 active indicator Bit[3]: Phase4 active indicator Bit[2]: Phase3 active indicator Bit[1]: Phase2 active indicator Bit[0]: Phase1 active indicator	RO	–

12. Offset should only be changed or enabled/disabled when the controller is operating in PS0 mode.
13. This functionality will only be available if it is also enabled using the pin function resistor (See Table 8).

Table 20. I²C REGISTERS FOR A RAIL

Reg Addr	Register Name	Description	Access	Default
0x05	VM2_HYST[5:3] SVM0_Hys_Arail[2:0]	Bit[5:3]: Set VM2 Hysteresis, 8 steps VM2 Hys = (ICCMAX/100) x (2 + [5:3]) Bit[2:0]: Set SVM0 Hysteresis, 8 steps SVM0 Hys = (ICCMAX/100) x (2 + [2:0])	R/W	00h
0x1C	VR_SR[3:0] SVR_SR[7:4]	DVID slew rate. Range is from 8 mV/μs to 48 mV/μs. 0x0~0x5, 8 mV/μs~18 mV/μs, 2 mV/μs per step 0x6~0xF, 21 mV/μs~48 mV/μs, 3 mV/μs per step Note: 0x1D[7] must be set to enable I²C slew rate control using this register	R/W	33h
0x21	SVRSHDN_TH[7:4]	Bit[7:4]: A Rail VRSHDN Threshold Setting. See Table 12 for threshold values Bit[3:0]: Reserved	R/W	70h
0x29	SVM0[7:0]	Current Threshold for SLCS0 (SVM0) Resolution = (ICCMAX / 255) A/bit	R/W	00h
0x2A	 SIICP1[1] SIICP0[0]	*Number of phases active in each I²C state* Phase count while in I²C defined states Bit[7:2]: Reserved Bit[1]: phases on in SLCS1 Bit[0]: phases on in SLCS0 “0”: 2 phases, “1”: 1 phase	R/W	02h
0x2B	SVOFS0[7:0]	*Voltage Offset Adjustment* (Note 15) Offsets for I²C states SLCS0 – SLCS1 (5 mV/step). SVOFS is 2’s compliment, Bit 7 is sign bit. Voltage change slew rate is SLOW. Note: 0x39[4] must be set to enable offset function.	R/W	00h
0x2C	SVOFS1[7:0]		R/W	00h
0x2D	SIICF0[7:4] SIICF1[3:0]	SIICF0[7:4] = SLCS0 operating frequency SIICF1[3:0] = SLCS1 operating frequency Refer to switching frequency configuration settings in Table 9. Note: 0x52[2] must be set to enable I²C frequency control	R/W	00h
0x2E	SIICLL0[7:4] SIICLL1[3:0]	DC Load Line Weighting LL adjustment in each I²C state SLCS0 – SLCS1 0% – 93.75%, 6.25% steps Default = 50% of externally programmed LL Note: 0x3A[2] must be set to enable DC loadline adjustment	R/W	88h
0x2F	SCB_EN[7] SPH1_IGAIN[6:4] SPH2_IGAIN[2:0]	Adjustment SCB_EN [7] = Enable/Disable current balance feature. Enable = 0 (Default), Disable = 1 *Current Balance Gain* SPH1_IGAIN[6:4] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5% SPH2_IGAIN[2:0] 000 = 50%; 001 = 62.5%; 010 = 75%; 011 = 87.5%; 100 = 100%; 101 = 112.5%; 110 = 125%; 111 = 137.5%	R/W	44h
0x32	SLCHVID[7:0]	Latch VID register – default = 1.1 V (Abh) Refer to IMVP9.1 SVID table. VDAC control by LCHVID when 0x39[6] = “1”	R/W	ABh
0x33	SIOUT[7:0]	8 bit ADC reading. Reads FFh when IOUTA = ICCMAXA	RO	–
0x34	SVOUT_MSB[7:0]	A Rail Voltage Reading, 8−bit MSB If 0x3A[6] = ”0”, VOUT = VDAC, 5 mV/step If 0x3A[6] = ”1”, VOUT = Sense Voltage, 3.9 mV/step Note: Read this register before reading SVOUT_LSB (0x35).	RO	–
0x35	SVOUT_LSB[1:0]	A Rail Voltage Reading, 2−bit LSB If 0x3A[6] = ”0”, VOUT = VDAC, 5 mV/step If 0x3A[6] = ”1”, VOUT = Sense Voltage, 3.9 mV/step Note: Read SVOUT_MSB (0x34) before reading this register.	RO	–

Table 20. I²C REGISTERS FOR A RAIL (continued)

Reg Addr	Register Name	Description	Access	Default
0x36	Sprotection Indicator[5:0]	*Protection Enable/Disable Indicator* Bit[5]: OCP Indicator 0 = Not Active; 1 = Active Bit[4]: Per phase OCP Indicator 0 = Not Active; 1 = Active Bit[3]: OVP Indicator 0 = Not Active; 1 = Active Bit[2]: UVP Indicator 0 = Not Active; 1 = Active Bit[1:0]: Per phase OCP indicator if Bit[4] = 1 phase 1 = 01; phase 2 = 10; No fault = 00	RO	–
0x37	STotal OCP[7:4] SOCP_L[3:1] SOCP_L Hys[0]	*Total OCP threshold, OCP_L flag assertion level and hysteresis setting* SOCP[7:4]: Total Current OCP Ratio of ILIM (Over Current Protection) 0000: 50%; 0001: 60%; 0010: 70%; 0011: 80%; 0100: 90%; 0101: 100%; 0110: 110%; 0111: 120%; 1000: 130%(Default); 1001: 140%; 1010: 150%; 1011: 160%; 1100: 170%; 1101: 180%; 1110: 190%; 1111: 200% SOCP_L[3:1]: OCP_L Ratio of ILIM (Over Current Protection) 000: 65%; 001: 70%; 010: 75%; 011: 80%; 100: 85%; 101: 90%(Default); 110: 95%; 111: 100% SOCP_L Hys[0]: OCP_L Hysteresis Ratio of ILIM (Over Current Protection) 0: 10% (Default); 1: 20% Note: 0x39[3] must be set to enable Total Current OCP function.	R/W	8Ah
0x38	SIMONOvR[7:6] SOC[5:4] SUV[3:2] SOV[1:0]	SIMONOvR[7]: Overwrite SVID 0x15h (IMON) “1” = Enable; “0” = Disable SIMONOvR[6]: Overwrite SVID 0x15h (IMON) “1” = 1/2; “0” = 1/4 SOCP[5:4]: Per Phase OCP 00 = 400 mV; 01 = 500 mV (Default); 10 = 600 mV; 11 = 700 mV The lowest threshold for each phase is 400mV/amp gain. The default gain is 6 so this corresponds to 83 mV across CSPxA/CSREFA. Bit[3:2]: UVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV Bit[1:0]: OVP Setting 00 = 400 mV (default); 01 = 500 mV; 10 = 600 mV; 11 = 700 mV	R/W	50h
0x39	SMisc1[7:0]	Bit[7]: Slew Rate Control 0 = Select from pin 1 = Select from register Bit[6]: VDAC Control 0 = SVID 0x31 VDAC follow SVID 1 = SVID 0x31 VDAC ignore SVID. VDAC control by SLCHVID Bit[5]: PWR State Control 0 = SVID 0x32 PWR state follow SVID 1 = SVID 0x32 PWR state ignore SVID. Phase control by I²C Bit[4]: OFS control (Note 15) 0 = SVID 0x33 Offset follow SVID 1 = SVID 0x33 Offset ignore SVID. Offset control by I²C Bit[3]: Total OCP Control 0 = Disable Total OCP function (OCPL# = H) 1 = Enable Total OCP function Bit[2]: Per−phase OCP Control 0 = Disable Per−phase OCP function 1 = Enable Per−phase OCP function Bit[1]: OVP Control 0 = Disable OVP function (VR_OVP# = H) 1 = Enable OVP function Bit[0]: UVP Control 0 = Disable UVP function 1 = Enable UVP function	R/W	0Fh

Table 20. I²C REGISTERS FOR A RAIL (continued)

Reg Addr	Register Name	Description	Access	Default
0x3A	SMisc2[7:0]	Bit[7]: Spread Spectrum (Note 14) “0” to disable; “1” to enable Bit[6]: SVOUT Voltage value select “0” for SVID register; “1” actual A/D Bit[5]: Output voltage offset control (Note 15) “0” to disable; “1” to enable Bit[4]: Auto phase function control (Note 14) “0” disable; “1” to enable If Bit[4] is 0, follow SIICP0 if 39[5] = 1; or follow SVID PS if 39[5] = 0. This bit with function after 0x39[5] = “1” Bit[3]: DCM enable when in 1 phase “0” always CCM; “1” DCM Bit[2]: Loadline enable “0” disables LL; “1” enables (default) Bit[1]: USM/PSM selection when in DCM “0” enable PSM (pulse skip mode); “1” enables USM (ultrasonic mode) Bit[0]: OCP_L# enable control “0” to disable; “1” to enable	R/W	9Ch
0x3B	SVRSHDN_BH[7] SVRSHDN_EN[6] SOCPTH[5] SVRHOT_ALERT_EN[4] STEMP_VRHOT#[3:0]	*Select Behavior of VRSHDN* Bit[7]: OTP behavior selection 0 = VRSHDN# go low only; 1 = controller shutdown only Bit[6]: OTP function enable/disable 0 = Disable; 1 = Enable Bit[5]: Total OCP threshold control when single phase operation. 0 = Default; 1 = Double Bit[4]: VRHOT# “0” = Enable; “1” = Disable Note: when VR_HOT is disabled ALERT will not assert and the Temp Status bit (SVID reg 0x10 bit) is not set. Bit[3:0]: VRHOT. Threshold See Table 12 for threshold values	R/W	04h
0x3F	SIMON_OFS[7:0]	IMON offset [7:0] (can be positive or negative) SVID IMON Offset: 0x15 ± Bit[7:0] I²C IMON Offset: 0x33 ± Bit[7:0]	R/W	00h
0x40	SDVID_OFS[7:0]	DVID offset function (2’s compliment, 5 mv step) Enable this register after 0x39[4] = “1” (Note 15)	R/W	00h
0x42	SVBOOT_ENABLE[7] SVBOOT_VOLTAGE[6:0]	Bit[7]: VBOOTA Operation ’0’ => VBOOTA follows H/W resistor setting as per table 6. ’1’ => VBOOTA follows I2C setting. Bits[6:0] VBOOTA voltage setting = 0 => VBOOTA = 0 V = N, where 1 ≤ N ≤ 127 = > VBOOTA = 300 mV + VDAC_STEP X (2N – 11) VDAC_STEP is the output voltage step size as shown in Table 6.	R/W	00h
0x44	STM[7:0]	*I²C Thermal Monitor Value Reading.* Temperature reports in degree celsius (°C). To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resistor in parallel. NTC uses 100 kΩ under 25°C and B25/50 approximates 4250. Use 13.5 kΩ for parallel resistor and 0.3 kΩ for series resistor.	RO	–
0x57	SAC_NOISE_SLOPE[5:4] SAC_NOISE_MULTI_LOPE[3] SAC_NOISE_SR[2:1] SAC_NOISE_EN[0]	Bit7:6]: Reserved Bit5:4]: Acoustic noise set point to change DVID down slope “00” = Every 4 VID Steps for VID Down “01” = Every 8 VID Steps for VID Down “10” = Every 16 VID Steps for VID Down “11” = Every 32 VID Steps for VID Down Bit[3]: Acoustic noise multi slope on DVID Down “0” = Disable (Default); “1” = Enable Bit[2:1]: Acoustic noise slew rate control “00” = 1/2 (Default); “01” = 1/4; “10” = 1/8; “11” = 1/16 Bit[0]: Acoustic noise mode enable “0” = Disable; “1” = Enable (Note 14)	R/W	01h

Table 20. I²C REGISTERS FOR A RAIL (continued)

Reg Addr	Register Name	Description	Access	Default
0x58	SBST_CAP_LOW_TIME[5:4] SBST_CAP_ON_DVID[3] SBST_CAP_TIME[2] SBST_CAP_PULSED[1] SBST_CAP_EN[0]	Bit[7:6]: Reserved Bit[5:4]: Boost cap low time. ”00” = 400 ns, ”01” = 200 ns, ”10” = 800 ns, ”11” = 600 ns Bit[3]: Boost cap in parallel with DVID on VID up from low power state “0” = Disable (Default); “1” = Enable Bit[2]: Shorter Boost Cap Refresh ”0” = when ps_exit_timer Eh; ”1” = when ps_exit_timer 7h Bit[1]: Boost cap low PS exit ”0” = Continuous Boosting when Phases are off ”1” = Boost Cap Refresh at PS Exit only Bit[0]: Boost Cap Mode Enable “0” = Disable “1” = Enable	R/W	0Bh
0x59	TEMP_ALERT#[7:4] STEMP_ALERT#[3:0]	Bit[7:4]: Thermal Alert Threshold for Main Rail Bit[3:0]: Thermal Alert Threshold for A−Rail See Table 12 for threshold values	R/W	33h
0x5B	SACTIVE_PHASE[1:0]	Real time active phase indicator for A Rail. ”1” = Active Bit[1]: Phase2 active indicator Bit[0]: Phase1 active indicator	R0	–

14. This functionality will only be available if it is also enabled using the pin function resistor (See Table 8).
15. Offset should only be changed or enabled/disabled when the controller is operating in PS0 mode.

Table 21. GENERAL REGISTERS

Reg Addr	Register Name	Description	Access	ASP2100	ASP2100R
0x48	Version ID		RO	01h	
0xB2	Chip ID		RO	50h	70h

Table 22. SVID REGISTER MAP

Index	Register Name	Description	Access	Default 00h	PSYS 0Dh
00h	VENDOR_ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to **onsemi** is 1Ah.	R	1Ah	1Ah
01h	PROD_ID	Uniquely identifies the VR product. The VR vendor assigns this number.	R	ASP2100: 50h ASP2100R: 70h	ASP2100: 50h ASP2100R: 70h
02h	PROD_REV	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R	01h	01h
05h	PROTOCOL_ID	Identifies the SVID Protocol the controller supports	R	0Eh	0Eh
06h	CAPABILITY	*Informs the Master of the controller's Capabilities* "1" = supported, "0" = not supported Bit[7]: Output Current reported as a fraction of IC-CMAX. Default = "1" Bit[6]: ADC Measurement of Temp Supported. Default = "1" Bit[5]: ADC Measurement of Pin Supported. Default = "0" Bit[4]: ADC Measurement of Vin Supported. Default = "1" Bit[3]: ADC Measurement of Iin Supported. Default = "0" Bit[2]: ADC Measurement of Pout Supported. Default = "1" Bit[1]: ADC Measurement of Vout Supported. Default = "1" Bit[0]: ADC Measurement of Iout Supported. Default = "1"	R	D7h	N/A
10h	STATUS1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR. Bit[7]: Read status Bit[6:4]: Reserved Bit[3]: VID 30mV above target Bit[2]: ICCMAX status Bit[1]: Temp status Bit[0]: VR settled status	R	–	N/A
11h	STATUS2	Data register showing optional status_2 data. Bit[7:3]: Reserved Bit[2]: Cycle to cycle current limit Bit[1]: Data frame fault Bit[0]: Parity fault	R	–	N/A
12h	TEMPERATURE	Data register showing temperature zones the system is operating in.	R	–	N/A
14h	LASTREAD	Contains last read value read by GET command.	R	00h	N/A
15h	IOUT_H	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max.	R	01h	01h
16h	VOUT_H	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 15.625 mV.	R	01h	N/A
17h	VR_TEMP	8 bit binary word ADC of voltage. Binary format in deg C, IE 100°C = 64h. A value of 00h indicates this function is not supported. To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resistor in parallel. NTC uses 100 kΩ under 25°C and B25/50 approximates 4250. Use 13.5 kΩ for parallel resistor and 0.3 kΩ for series resistor.	R	01h	N/A
18h	POUT_H	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported.	R	01h	N/A

Table 22. SVID REGISTER MAP (continued)

Index	Register Name	Description	Access	Default 00h	PSYS 0Dh
1Ah	VIN_H	8 bit binary word ADC of voltage. Input voltage is ”1Ah / 255 * 2.5 *12”, unit is Volt.	R	01h	N/A
1Bh	PIN_H	Required for Input Power Domain Address 0Dh.	R	N/A	00h
1Ch	STATUS2_LASTREAD	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	–	N/A
1Fh	I_C2CL	Cycle−to−cycle current limit level.	R/W	00h	N/A
21h	ICC_MAX	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.	R	–	–
22h	TEMP_MAX	Data register containing the max temperature the platform supports and the level (No Suggestions) asserts. This value defaults to 106°C and programmable over the SVID Interface	R	6Ah	N/A
24h	SR_FAST	Slew Rate for SetVID_fast commands. Binary format in mV/μs.	R	By setting	N/A
25h	SR_SLOW	Slew Rate for SetVID_slow commands. It is 16, 8, 4 or 2 times slower than the SR_fast rate. Binary format in mV/μs. FAST/4 is default for IMVP9.1.	R	1/4 Fast	N/A
26h	VBOOT	The VBOOT is resistor programmed at startup. The controller will ramp to VBOOT and hold at VBOOT until it receives a new SVID SetVID command to move to a different voltage.	R	By setting	N/A
2Ah	SLOW_SR_SEL_HC	Fast_SR/2 (Default), Fast_SR/4, Fast_SR/8, Fast_SR/16	R/W	02h	N/A
2Bh	PS4_EXIT_LAT	Reflects the latency of exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the output voltage beginning to ramp.	R	7Bh	N/A
2Ch	PS3_EXIT_LAT	Reflects the latency of exiting PS3 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID/SetPS command until the controller is capable of supplying max current of the command PS state.	R	55h	N/A
2Dh	EN_SVID_RDY_T	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands.	R	CAh	N/A
30h	VID_MAX	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP9.1 VID format.	R/W	FFh	N/A
31h	VID_SETTING	Data register containing currently programmed VID voltage. VID data format.	R	–	N/A
32h	PWR_STATE	Register containing the current programmed power state.	R	–	N/A
33h	OFFSET	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0 = positive margin, 1 = negative margin. Remaining 7 BITS are #. VID steps for margin 2 s complement 00h = no margin 01h = +1 VID step 02h = +2 VID steps FFh = −1 VID step FEh = −2 VID steps	R/W	00h	N/A

Table 22. SVID REGISTER MAP (continued)

Index	Register Name	Description	Access	Default 00h	PSYS 0Dh
34h	MULTI_VR_CFG	Bit mapped data register that configures multiple VRs behavior on the same bus and can be programmed to reset behavior of VR_Ready under 0.0 V VID command.	R/W	01h	00h
35h	MAIN_ADDR_PTR	Write address pointer for main address space.	R	–	N/A
49h	PSYS_DBC_CLR	Sets the duration of the Deassert Debounce applied to the PSYS critical comparator. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R/W	N/A	00h
4Ah	PSYS_CR_LVL_H	Sets the threshold level of the PSYS critical comparator, while PSYS is higher than this threshold the VR_HOT signal is asserted. Must be scaled to the same voltage level as PSYS ADC. Delay from PSYS exceeding threshold to VR_HOT# assertion is dependent on register 0x4F debounce time.	R/W	N/A	00h
4Bh	PSYS_W2_LVL_H	Sets the threshold level of the PSYS warning 2 comparator. Must be scaled to the same voltage level as PSYS ADC	R/W	N/A	00h
4Ch	PSYS_W1_LVL_H	Sets the threshold level of the PSYS warning 1 comparator. Must be scaled to the same voltage level as PSYS ADC	R/W	N/A	00h
4Dh	PSYS_WARN2_CNT	This counter accumulates the duration of time that the PSYS input is above the warning 2 level set by register 0x4B. This register is only cleared on each read or when the threshold level in 0x4B is changed. This register does not roll over when it reaches 0xFF. Data is held while in PS4. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R	N/A	–
4Eh	PSYS_WARN1_CNT	This counter accumulates the duration of time that the PSYS input is above the warning 1 level set by register 0x4C. This register is only cleared on each read or when the threshold level in 0x4C is changed. This register does not roll over when it reaches 0xFF. Data is held while in PS4. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R	N/A	–
4Fh	PSYS_DBC_SET	Sets the duration of the Assert Debounce applied to the PSYS critical comparator. This value is encoded in the Mantissa and Exponent format. Bits [7:4] contains Mantissa and [3:0] contains the Exponent.	R/W	N/A	00h
50h	ICCMAX_ADD	ICCMAX additional capability Bit[7:2]: Optional if not supported reads 0's Bit[1:0]: "00" indicates 1A/bit scaling, "01" indicates 2A/bit scaling	R	By setting	N/A
5Ch	C2CL_EVENT_CNT	Cycle−to−cycle current limit triggered event counter.	R	–	N/A

Table 23. IVMP9.1 VID COMMAND

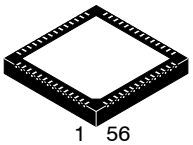
VID Code (Hex)	Setting Voltage (V) (5 mV/Step)	Setting Voltage (V) (10 mV/Step)
00h	0	0
01h	0.250	0.200
02h	0.255	0.210
03h	0.260	0.220
04h	0.265	0.230
05h	0.270	0.240
…	…	…
A1h	1.050	1.800
…	…	…
FBh	1.500	2.700
FCh	1.505	2.710
FDh	1.510	2.720
FEh	1.515	2.730
FFh	1.520	2.740

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

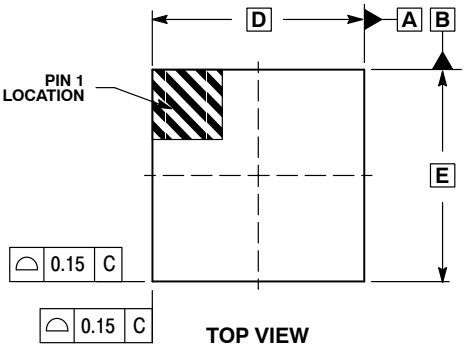
ON Semiconductor®

QFN56 7x7, 0.4P
CASE 485BT
ISSUE A

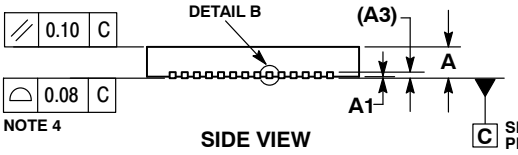
DATE 02 DEC 2014



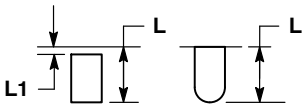
SCALE 2:1



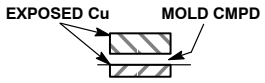
TOP VIEW



SIDE VIEW



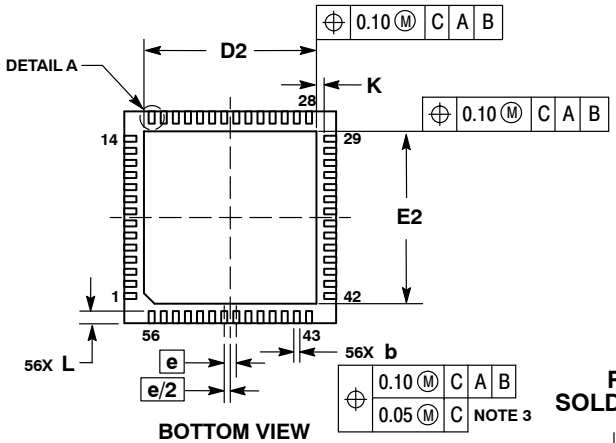
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

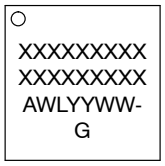
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAILS A AND B, ALTERNATE CONSTRUCTION PERTAINING TO THE L1 DIMENSION, ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	7.00 BSC	
D2	5.60	5.80
E	7.00 BSC	
E2	5.60	5.80
e	0.40 BSC	
K	0.25 REF	
L	0.30	0.50
L1	0.05	0.15



BOTTOM VIEW

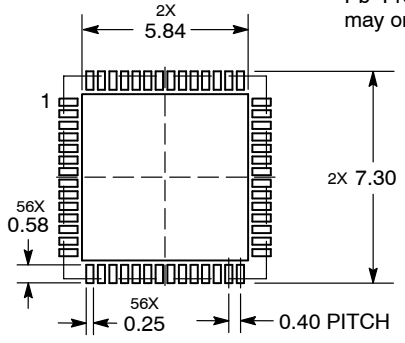
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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