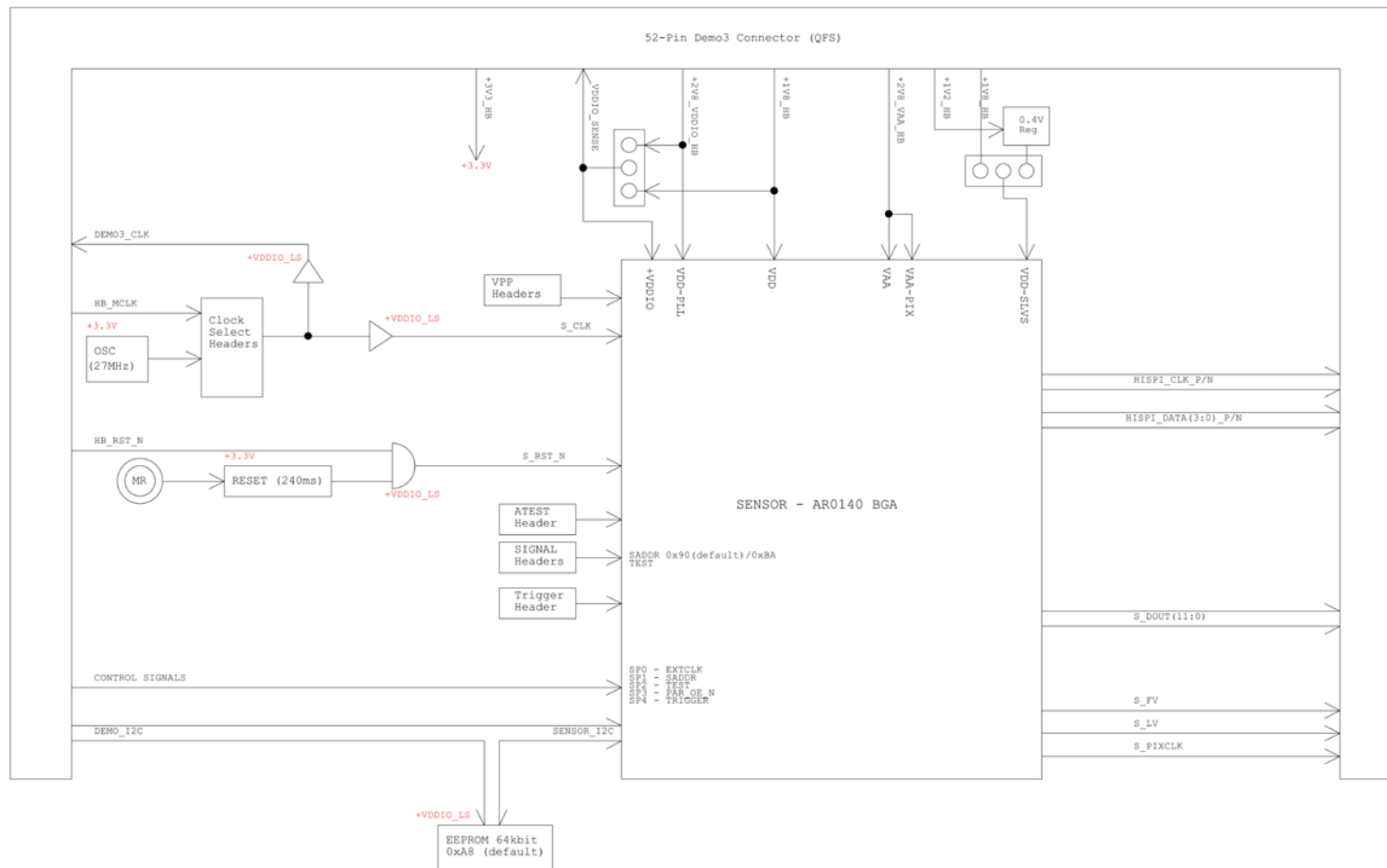
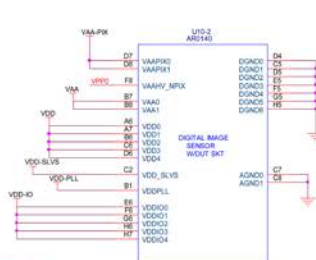
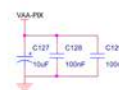


Schematic for the AR0140CS2M00AUEAH3-GEVB Evaluation Board

Block Diagram



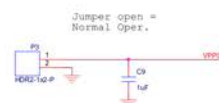
Signal	Pin	Signal	Pin
+5V0	4	+5V0	4
+3V3	4.5	+3V3	4.5
+VDDIO_L5	4.5.6	+VDDIO_L5	4.5.6
VDD	4	VDD	4
VDD-IO	4	VDD-IO	4
VDD-SLVS	4	VDD-SLVS	4
VDD-PLL	4	VDD-PLL	4
VWA	4	VWA	4
VWA-PX	4	VWA-PX	4



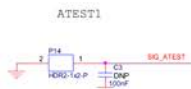
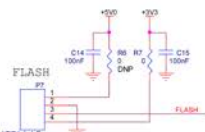
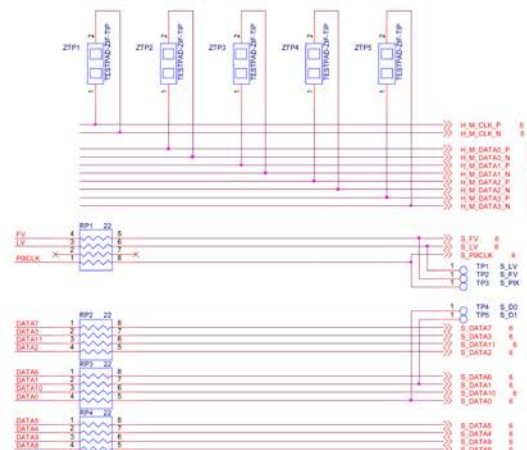
TRIGGER



Default state : 1-2 shorted
Open: Connect generator between pins 1 and ground

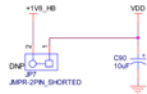


(Note for layout: - Place these testpads near the Demo3 I/F connector at the top side of PCB)

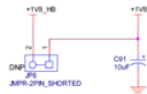


Debug Headers: Cut away the shorted trace and mount header for power debugging

VDD 1.8V SUPPLY



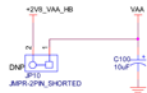
VDD-SLVS 1.8V SUPPLY



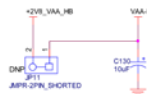
VDD-PLL 2.8V SUPPLY



VAA 2.8V SUPPLY

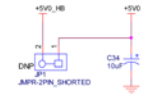


VAA-PIX 2.8V SUPPLY

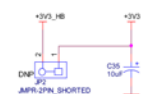


Power

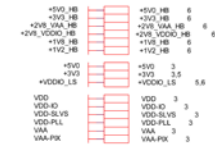
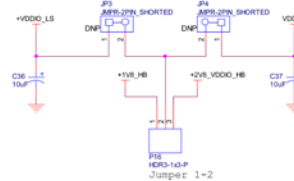
PERIPHERAL 5V SUPPLY



PERIPHERAL 3.3V SUPPLY



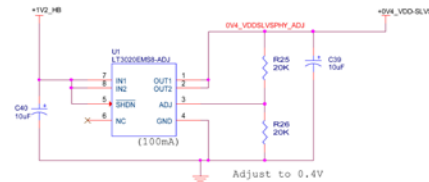
VDDIO & VDDIO LS 1.8V/2.8V SUPPLY



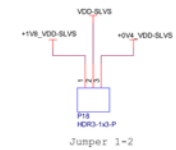
5V LED



VDDSLVSPHY 0.4V SUPPLY



Selection of 0.4V or 1.2V/1V8 for VDDSLVSPHY supply

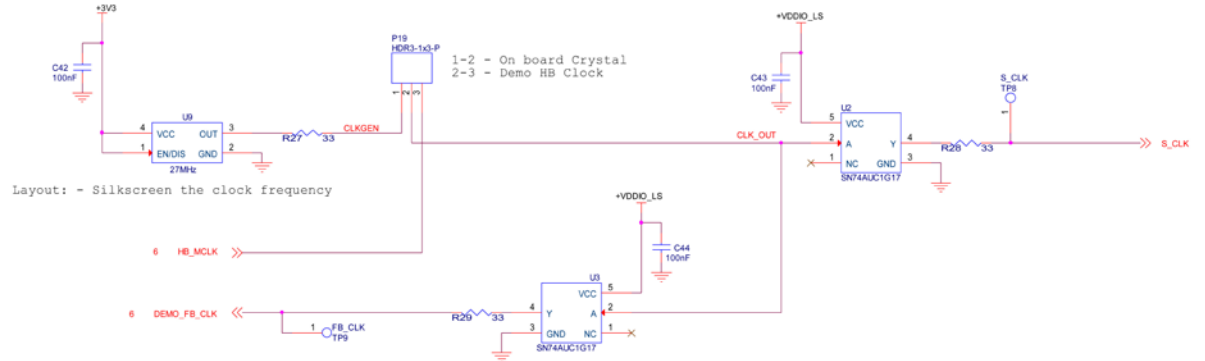




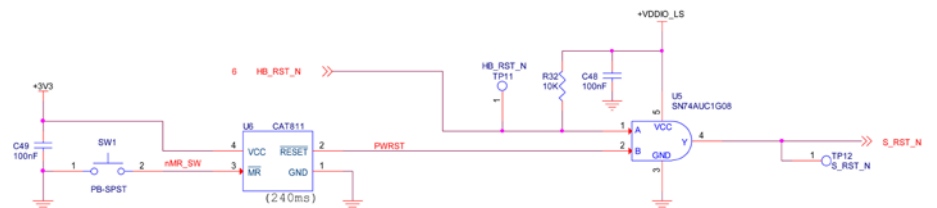
Clock and Reset

+5V0	3,4
+3V3	3,4
+VDDIO_LS	4,6

CLOCK CIRCUIT



RESET CIRCUIT



+SV0_HB		+SV0_HB	4
+SV3_HB		+SV3_HB	4
+ZVS_VAA_HB		+ZVS_VAA_HB	4
+ZVS_VOCIO_HB		+ZVS_VOCIO_HB	4
+1VS_HB		+1VS_HB	4
+1V2_HB		+1V2_HB	4
+SV3		+SV3	3.4.5
+VOCIO_LS		+VOCIO_LS	4.5

[illegible]

EPROM Address Switch Settings:

A2	A1	A0	Address =>
HIGH	LOW	LOW	0xA8 (default)
HIGH	HIGH	LOW	0xAC
LOW	HIGH	LOW	0xA4
LOW	LOW	LOW	0xA0

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