



Schematic for the AR0135 Evaluation Board



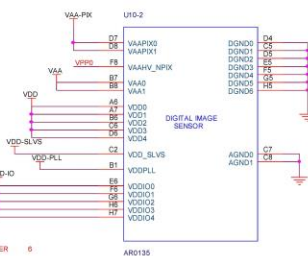
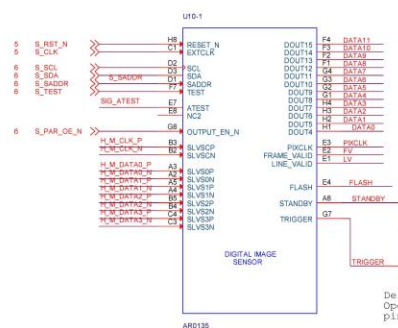
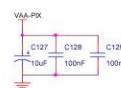
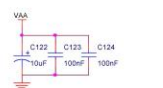
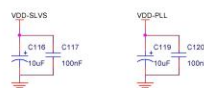
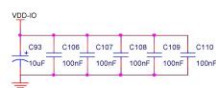
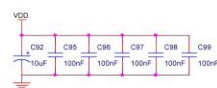
AR0135_BGA_Demo3Head

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1	Title Page
2	Block Diagram
3	Sensor
4	Power
5	Clock and Reset
6	External Interfaces


Rev	Who	Date	Description
Rev 0.0	aralex	05/07/14	Initial
Rev 0.0	aralex	05/08/14	Removed the 10nF Decaps on VDD and VDDIO for Sensor
		05/13/14	Updated the sensor with the new non socketed part, and added C-mount lens
		05/15/14	Updated the sensor with the new non socketed part, and added the socket for demo3 board
Rev 0.1	aralex	05/16/14	Removed text near R8 for TRIGGER signal Replaced R25 with a fixed resistor of 20K
	aralex	05/20/14	Removed Skip Block Fiducials FD4 and FD8.
Rev 1.0	aralex	04/23/15	Added a 2 pin header P28 for Trigger signal, deleted R8

Block Diagram

Signal	Level	Signal	Level
+5V0	4	+5V0	4
+3V3	4.5	+3V3	4.5
+VDDIO_LS	4.56	+VDDIO_LS	4.56
VDD	4	VDD	4
VDD-IO	4	VDD-IO	4
VDD-SLVS	4	VDD-SLVS	4
VDD-PLL	4	VDD-PLL	4
VAA	4	VAA	4
VAA-PXK	4	VAA-PXK	4

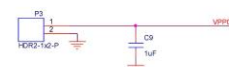
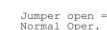


TRIGGER

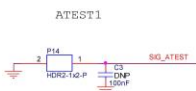
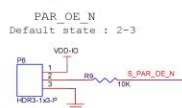
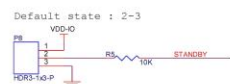
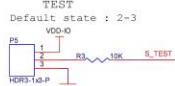
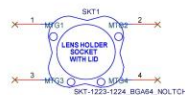
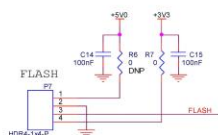
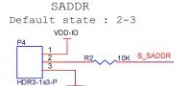
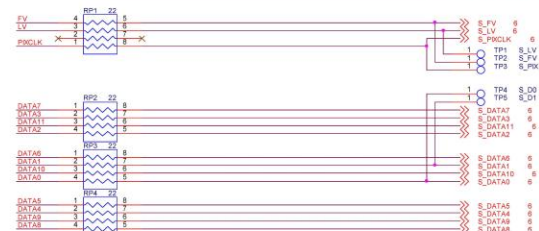
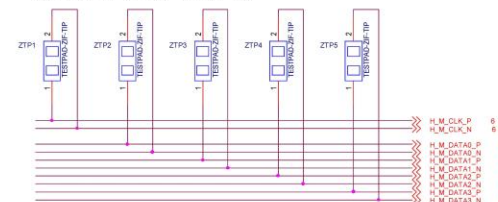


1 P26 2
HDR2-12-P S_TRIGGER 0

Default state : 1-2 shorted
Open: Connect generator between
pins 1 and ground



(Note for layout: - Place these testpads near the Demo3 I/F connector at the top side of PCB)

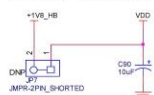




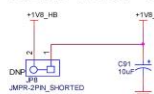
Power

Debug Headers: Cut away the shorted trace and mount header for power debugging

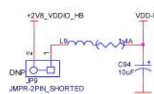
VDD 1.8V SUPPLY



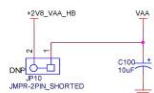
VDD-SLVS 1.8V SUPPLY



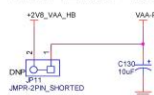
VDD-PLL 2.8V SUPPLY



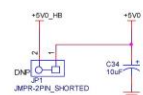
VAA 2.8V SUPPLY



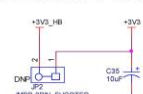
VAA-PIX 2.8V SUPPLY



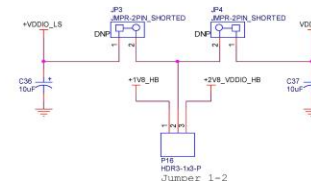
PERIPHERAL 5V SUPPLY



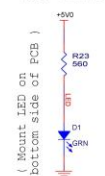
PERIPHERAL 3.3V SUPPLY



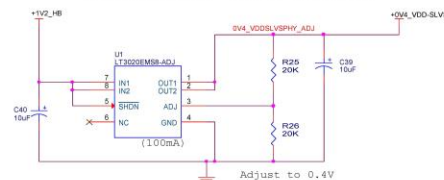
VDDIO & VDDIO LS 1.8V/2.8V SUPPLY



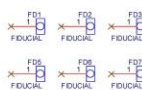
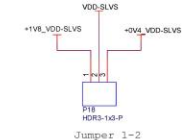
5V LED



VDDSLVSPHY 0.4V SUPPLY



Selection of 0.4V or 1.2V/1V8 for VDDSLVSPHY supply



Ground Testpoints



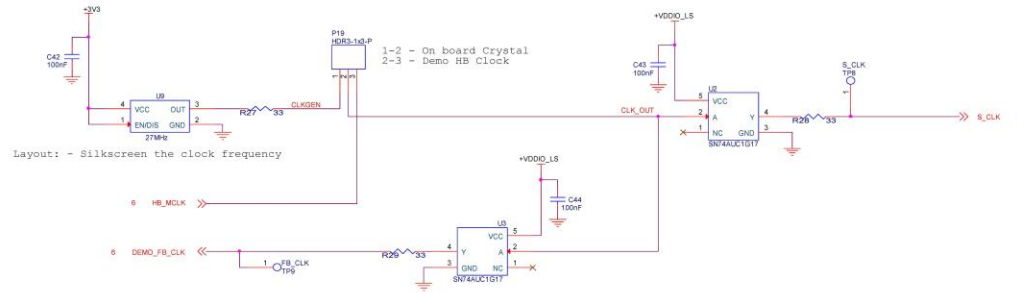
Mounting Holes



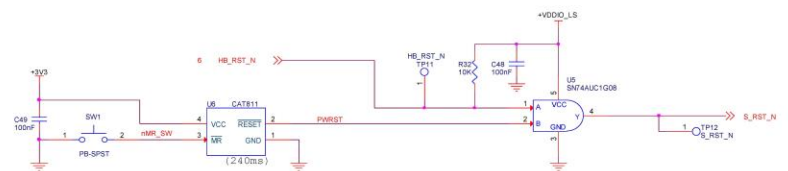


Clock and Reset

CLOCK CIRCUIT



RESET CIRCUIT



+5V0_HB		+5V0_HB	4
+3V3_HB		+3V3_HB	4
+2V8_VAA_HB		+2V8_VAA_HB	4
+2V8_VDDIO_HB		+2V8_VDDIO_HB	4
+1V8_HB		+1V8_HB	4
+1V2_HB		+1V2_HB	4
+3V3		+3V3	3.4.5
+VDDIO_LS		+VDDIO_LS	4.5

Figure 10 shows the internal circuitry of the HD96-20-P connector. It features two +VDDIO_1S power pins. Each pin is connected to a 100pF capacitor (C63, C64) and a 1.5k resistor (R36, R37) to the internal pins. The internal pins are labeled 2, 4, 5, and 6. Pin 2 is connected to DEMO_SDA, pin 4 to DEMO_SCL, pin 5 to S_SDA, and pin 6 to S_SCL. A jumper is indicated between pins 1-2 and 3-4 (default status).

EPROM Address Switch Settings:

A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
 A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xA9
 A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
 A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0

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