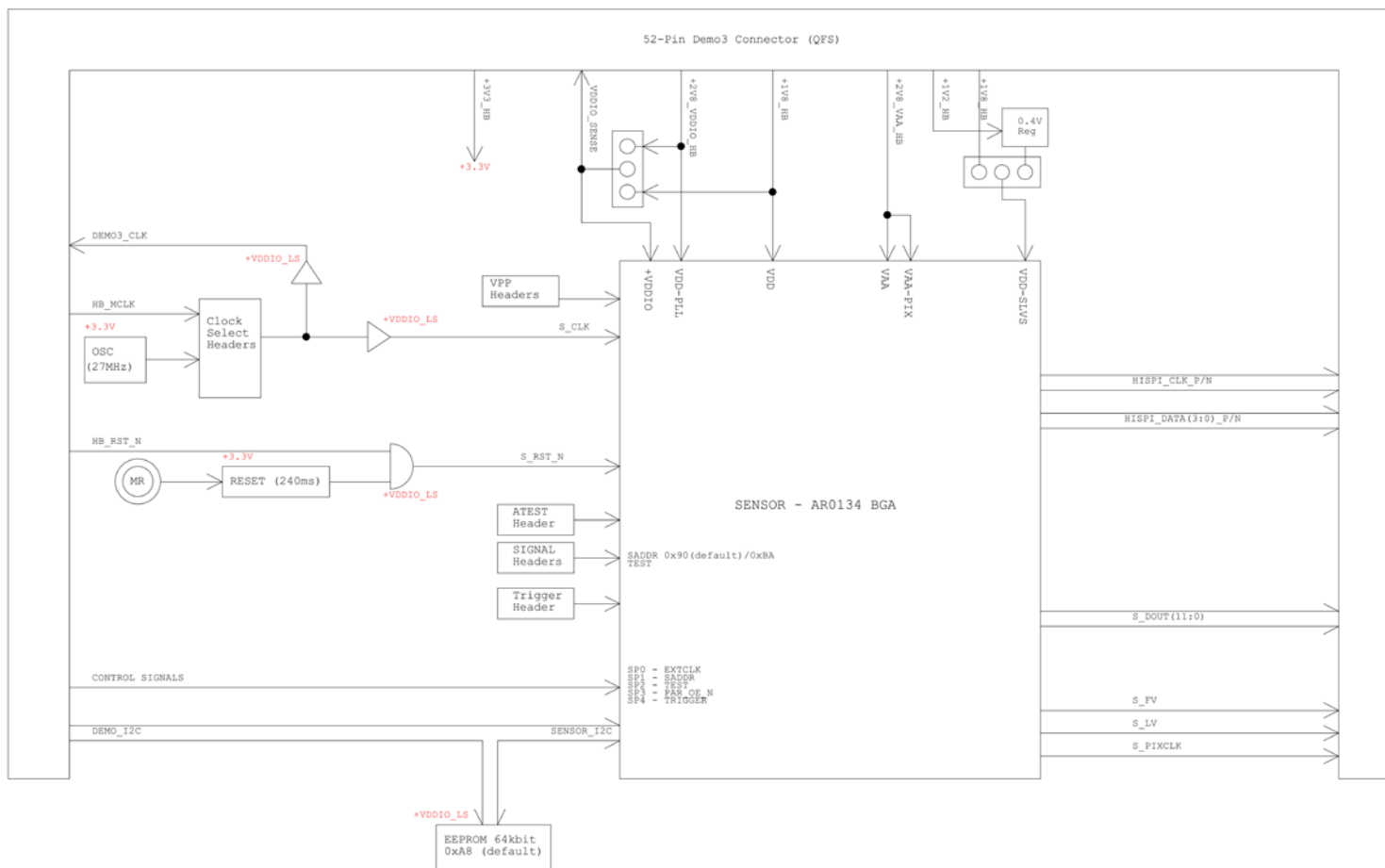
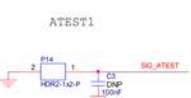
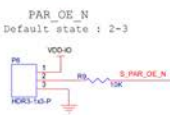
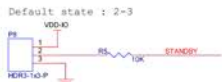
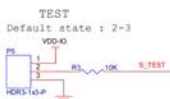
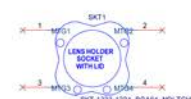
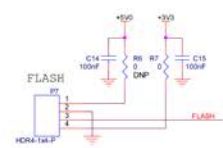
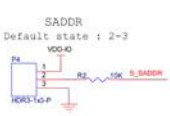
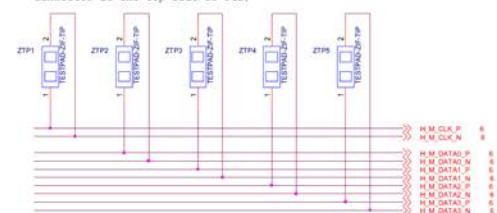
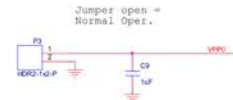
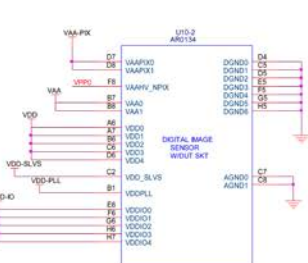
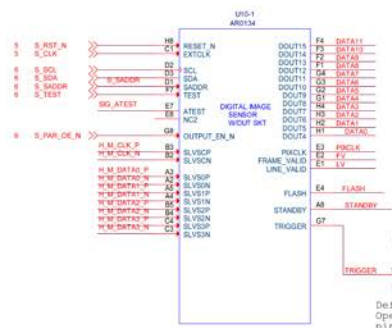
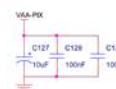
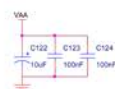
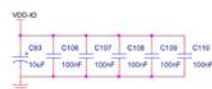
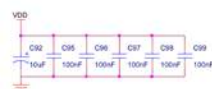


Block Diagram



Signal	Value	Signal	Value
+5V0	4	VDD	4
+3V3	4.5	VDD-IO	4
+VDDIO_L5	4.5	VDD-SLV5	4
VDD	4	VDD-PLL	4
VDD-IO	4	VAA	4
VDD-SLV5	4	VAA-PX	4
VDD-PLL	4		
VAA	4		
VAA-PX	4		

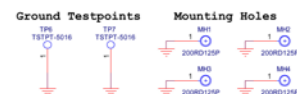
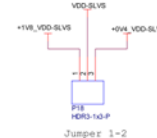
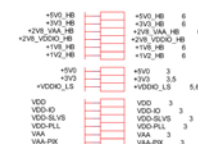


Power

[illegible]

The diagram shows a voltage divider circuit. The input is +12V_HB, which is connected to a 10µF capacitor and the IN pin of the LM3302EM88-ADJ (U1). The NC pin is connected to a 100nA current source. The OUT1 pin is connected to a 20k resistor (R25), which is then connected to another 20k resistor (R26) leading to the output 0V4_VDD5_VL. The OUT2 pin is connected to the output 0V4_VDD5_VSP4H_ADJ. The ADJ pin is connected to the output 0V4_VDD5_VL. The GND pin is connected to ground. A note indicates to 'Adjust to 0.4V'.

(Mount LED on bottom side of PCB)

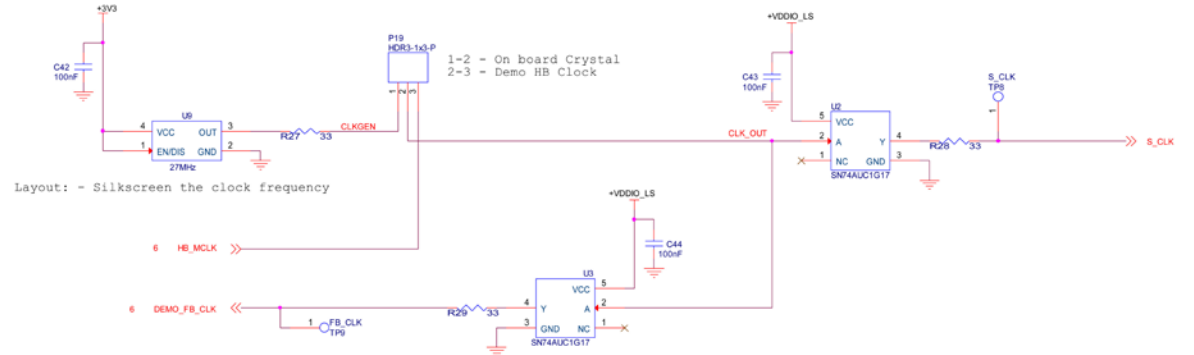




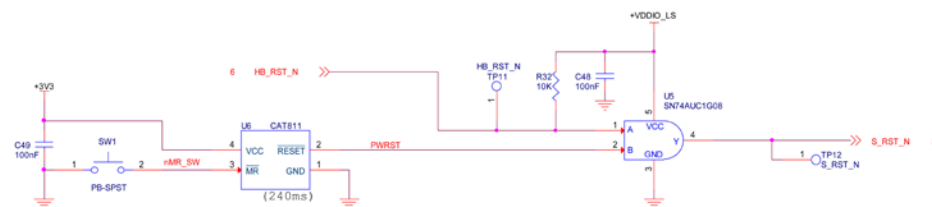
Clock and Reset

+5V0 3.4
+3V0 3.4
+VDDIO_LS 4.8

CLOCK CIRCUIT



RESET CIRCUIT



+5V0_HB		+5V0_HB	4
+3V3_HB		+3V3_HB	4
+2V5_VAA_HB		+2V5_VAA_HB	4
+2V5_VDDIO_HB		+2V5_VDDIO_HB	4
+1V8_HB		+1V8_HB	4
+1V2_HB		+1V2_HB	4
+3V3	3.4.5	+3V3	3.4.5
+VDDIO_LS	4.6	+VDDIO_LS	4.6

[illegible]

Demio: SDA
Demio: SCL

Demio: SDA
Demio: SCL

HDMR-230-P

Jumper: 1-2 & 3-4 (default status)

EPROM Address Switch Settings:

- A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
- A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
- A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0XA4
- A2 = LOW, A1 = LOW, A0 = LOW; Address => 0XA0

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