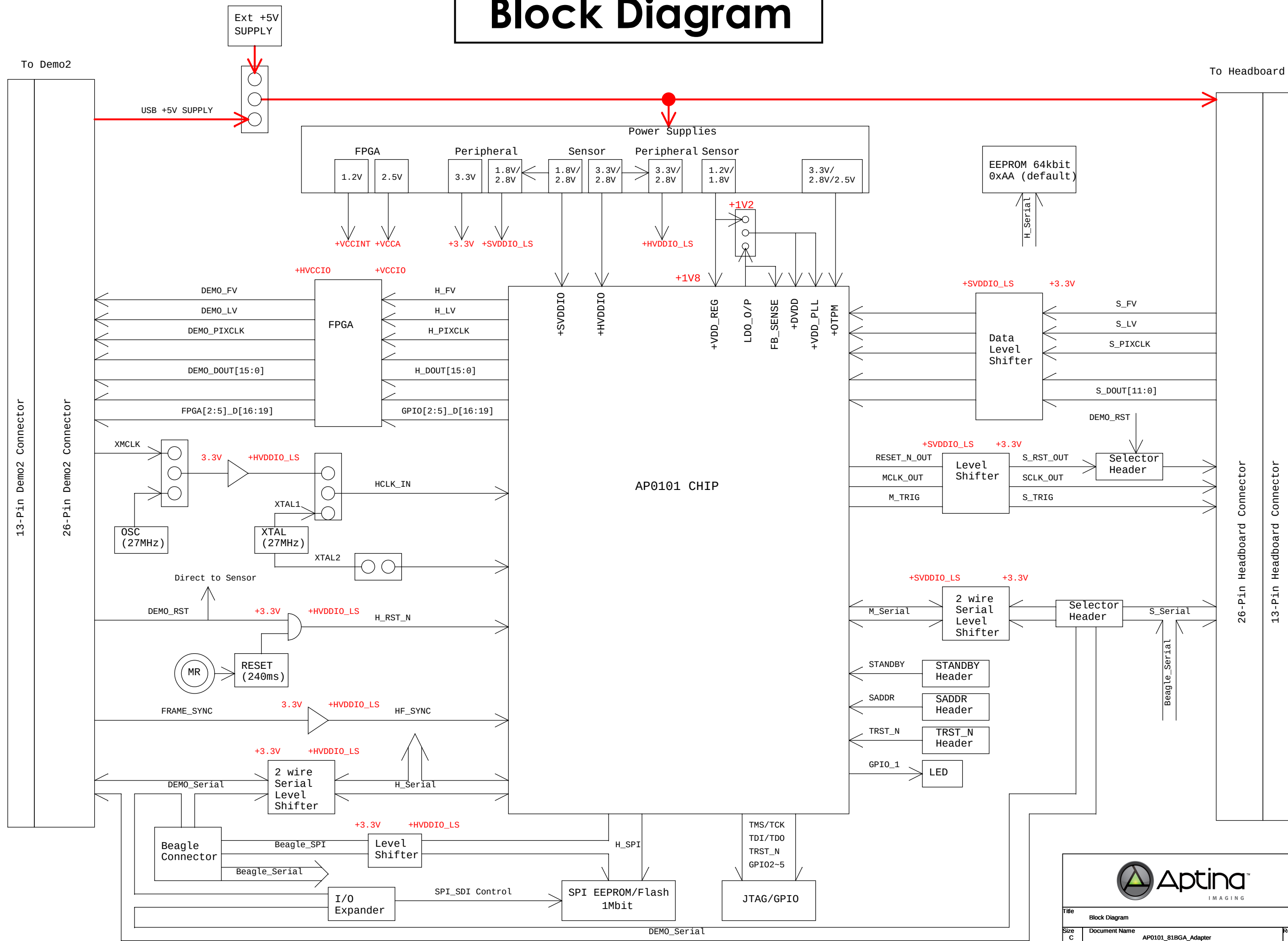


AP0101_81BGA_Adapter_Rev2

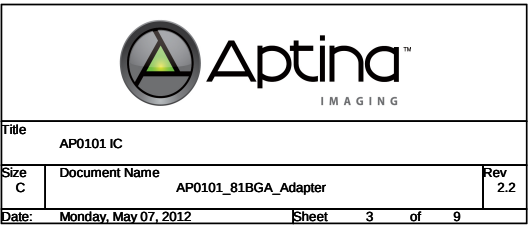
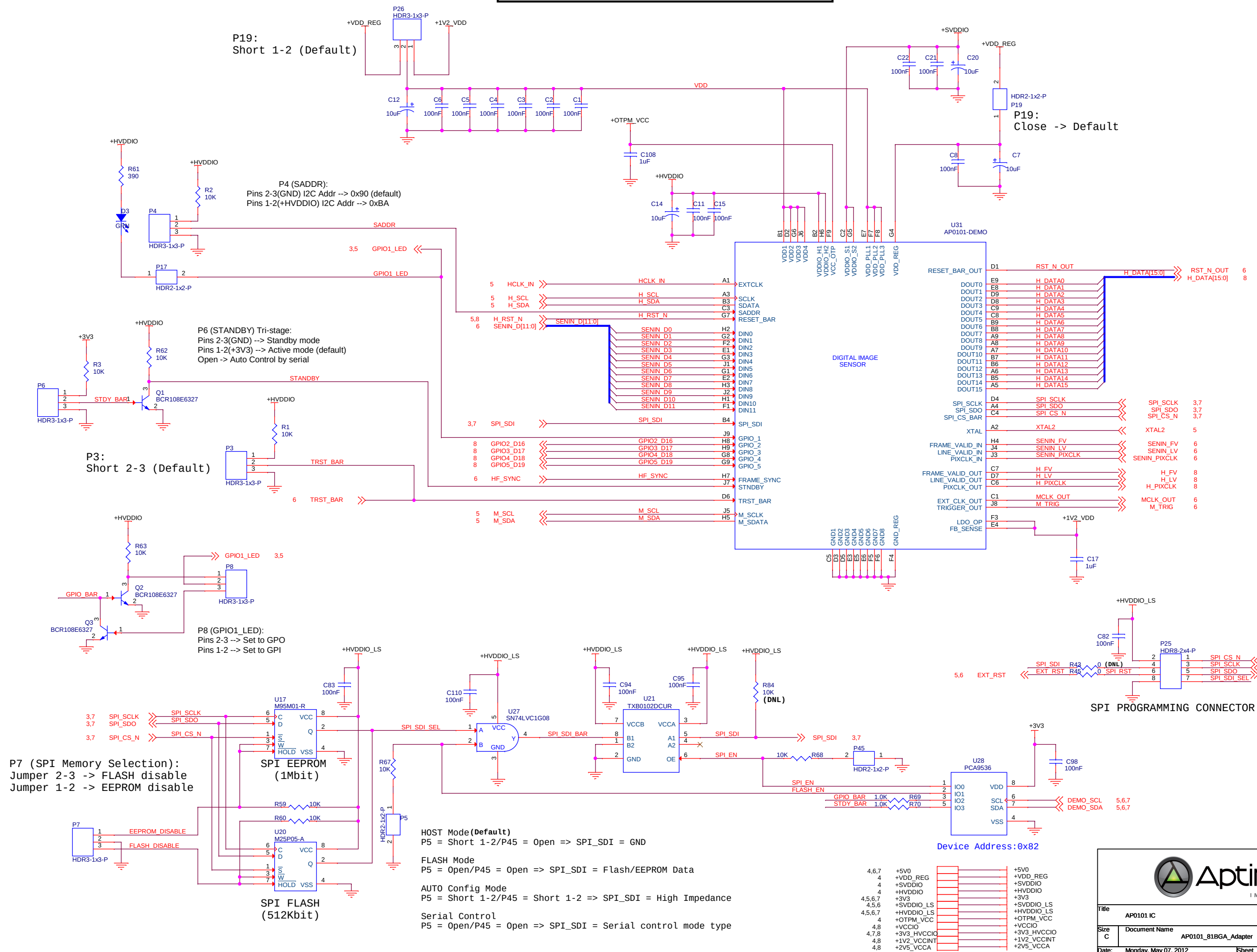
Page	Description
1	Title Page
2	Block Diagram
3	AP0101
4	Power
5	Clock and Reset
6	External Interfaces
7	BEAGLE/FPGA EXT I/F
8	FPGA Interface
9	Configuration Setting

Rev	Who	Date	Description
Rev 0.0	W.B.Foo	06/20/11	Initial.
Rev 0.1	W.B.Foo	08/18/11	Add P5, P51 and P19
Rev 0.2	W.B.Foo	08/19/11	Add U20, R63, Q1 and change P29 to polarized type type connector
Rev 0.3	W.B.Foo	08/23/11	Add P30, P31, P52, P53, R63, Q2, Q3, P8 and R55
Rev 1.0	W.B.Foo	10/10/11	Change Level Translator U11/U12 from PCA9517 to TXB0102 & R24/R25 to 2.2K resistor on Pg 5
Rev 1.1	W.B.Foo	10/28/11	Change test point TP6/TP7/TP8/TP11/TP10 to through hole type
Rev 1.2	W.B.Foo	12/19/11	1) Change U16/U24 to single part of U24(SN74AVCH4T245) combine M_TRIG/MCLK_OUT/RST_N_OUT 2) Add power supply for FPGA +1V2_VCCINT/+2V5_VCCA/+VCCIO/+3V3_HVCCIO 3) Add FPGA U32 & Flash Memory U47 4) Change P29 to smallest dimension type connector 5) Change U21 to TXB0102DCUR and add AND gate logic U27 SN74LVC1G08 FOR Auto-Config Circuit
Rev 1.3	W.B.Foo	01/30/12	1) Add external signal access for FRAME_SYNC 2) Change U31 AP0101 Symbol to non socket type
Rev 1.4	W.B.Foo	02/06/12	Add feedback resistor (R86) for XTAL (Y3)
Rev 1.5	W.B.Foo	02/22/12	Change U11 & U12 from TXB0102DCUR to TXS0102DCUR
Rev 2.0	W.B.Foo	04/25/12	Initial. 1) Change net name of U7 pin 5 VDDREG_ADJ to VCCINT_ADJ 2) Change U47 from N25Q128A13ESF40F to M25P64
Rev 2.1	W.B.Foo	05/03/12	Change SMPTE from J5 pin 15 to J6 pin 10 to support full PIXCLK of 20bit mode
Rev 2.2	W.B.Foo	05/08/12	Add Serial EEPROM (U16) on Host serial

Block Diagram

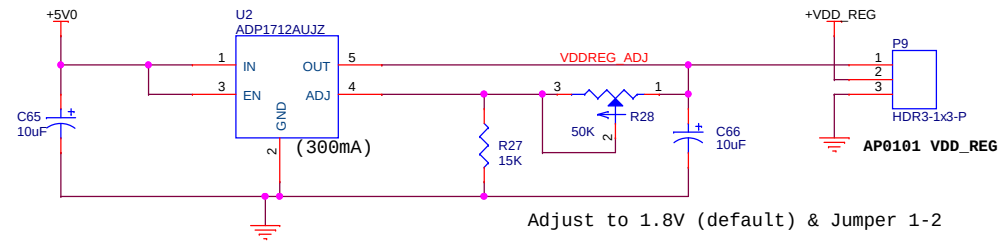


AP0101 IC

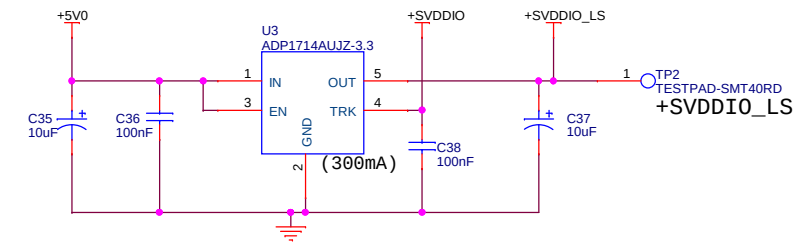


Power

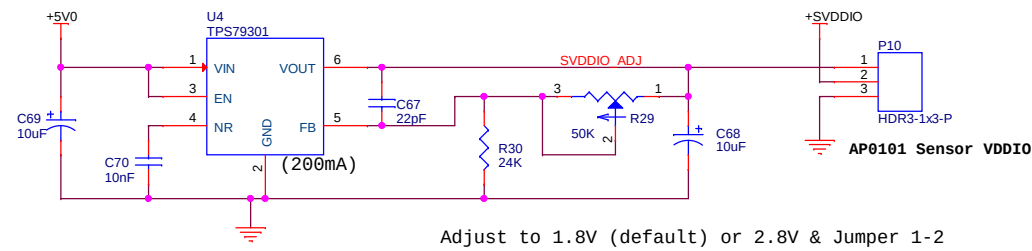
VDD_REG 1.8V SUPPLY



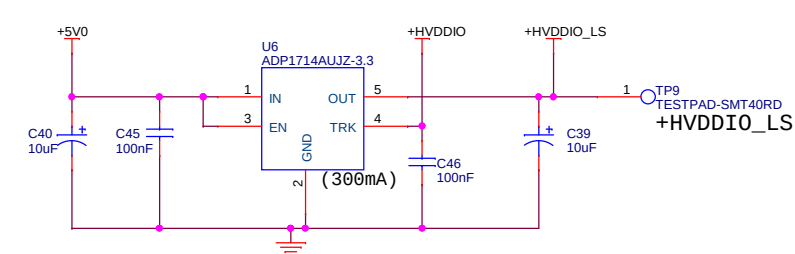
PERIPHERAL SVDDIO_LS SUPPLY



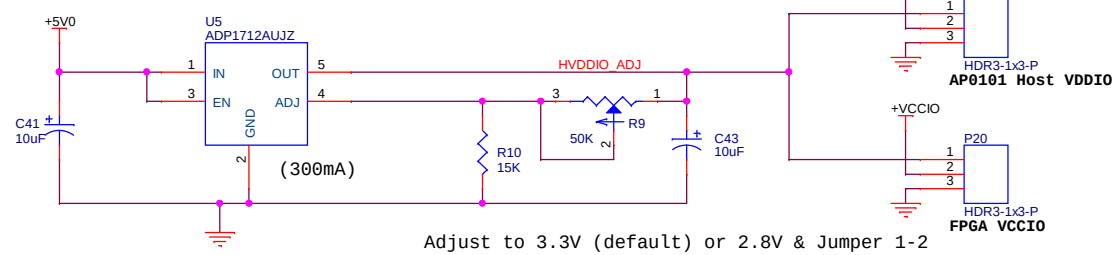
SVDDIO 1.8V or 2.8V SUPPLY



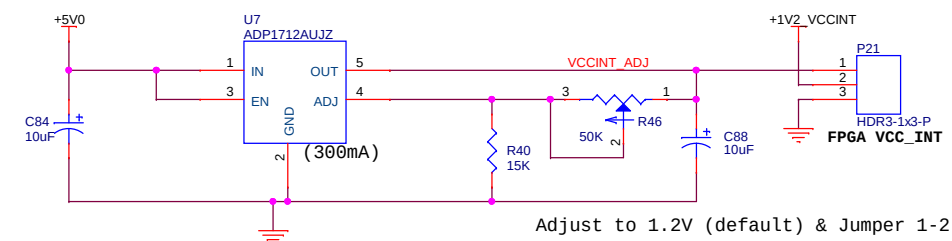
PERIPHERAL HVDDIO_LS SUPPLY



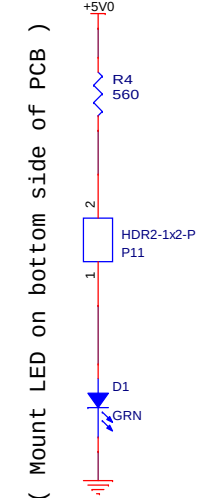
VCCIO & HVDDIO 3.3V or 2.8V SUPPLY



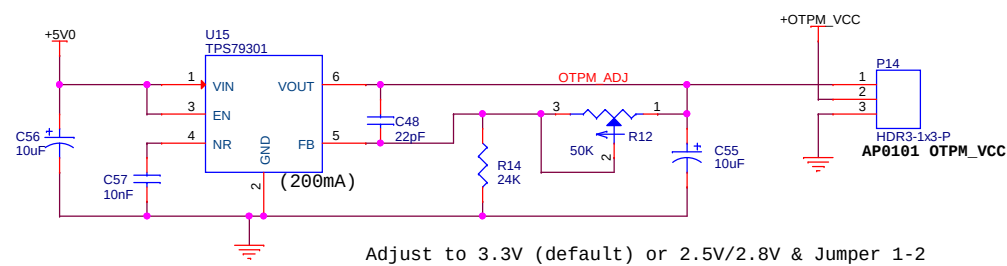
VCCINT 1.2V SUPPLY



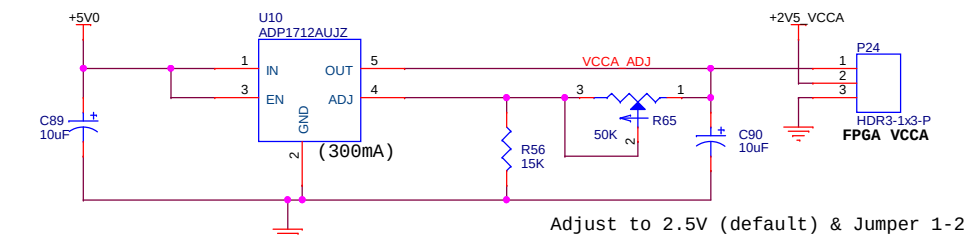
5V LED



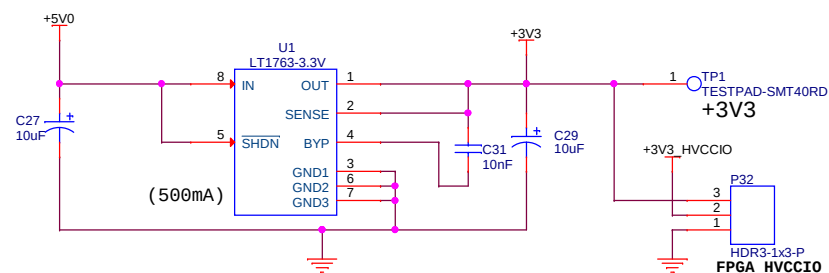
VDD_OTPM 3.3V, 2.8V or 2.5V SUPPLY



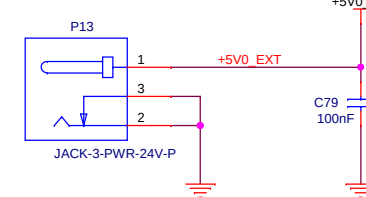
VCCA 2.5V SUPPLY



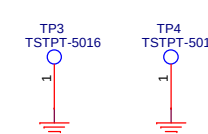
PERIPHERAL 3.3V SUPPLY



External +5V



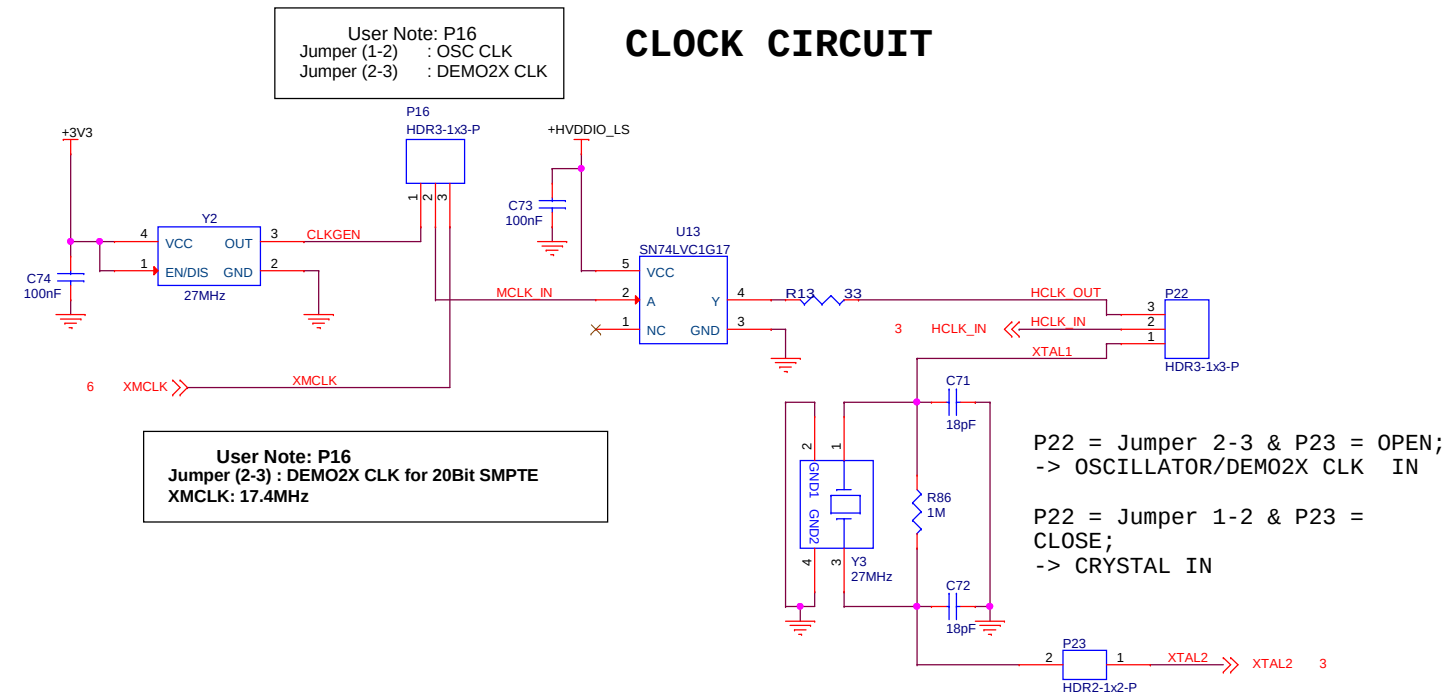
Ground Testpoints



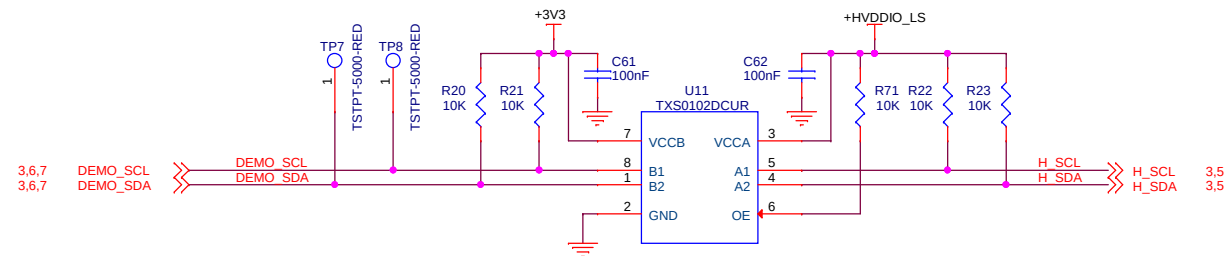
6,7	+5V0	+5V0
3	+VDD_REG	+VDD_REG
3	+SVDDIO	+SVDDIO
3	+HVDDIO	+HVDDIO
3,5,6,7	+3V3	+3V3
3,5,6,7	+SVDDIO_LS	+SVDDIO_LS
3	+HVDDIO_LS	+HVDDIO_LS
8	+OTPM_VCC	+OTPM_VCC
8	+VCCIO	+VCCIO
7,8	+3V3_HVCCIO	+3V3_HVCCIO
8	+1V2_VCCINT	+1V2_VCCINT
8	+2V5_VCCA	+2V5_VCCA

Clock/Reset/I2C Interface

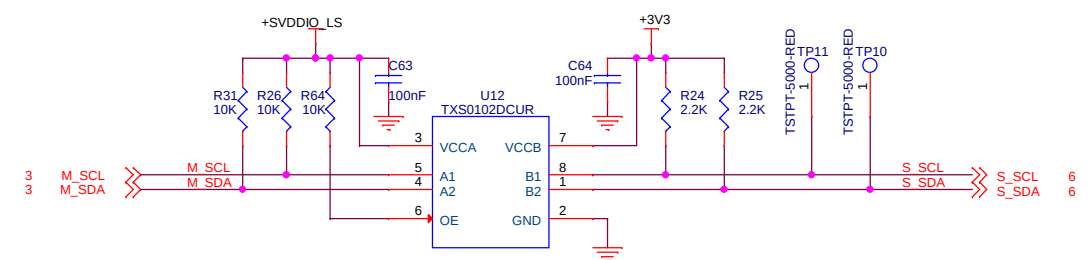
CLOCK CIRCUIT



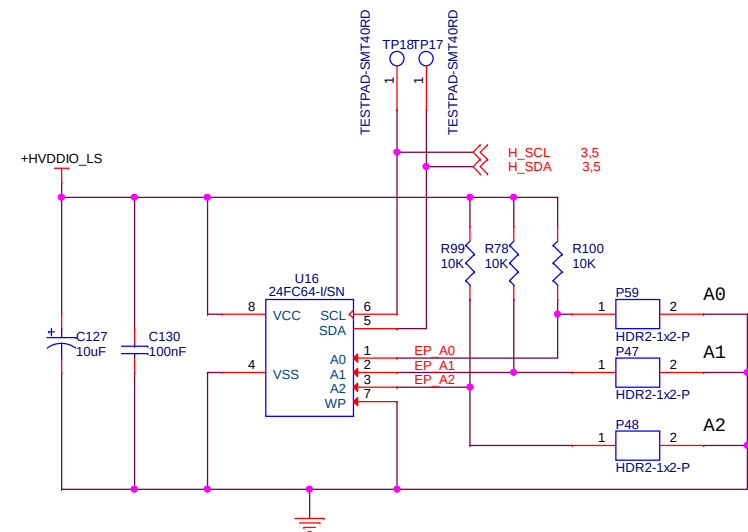
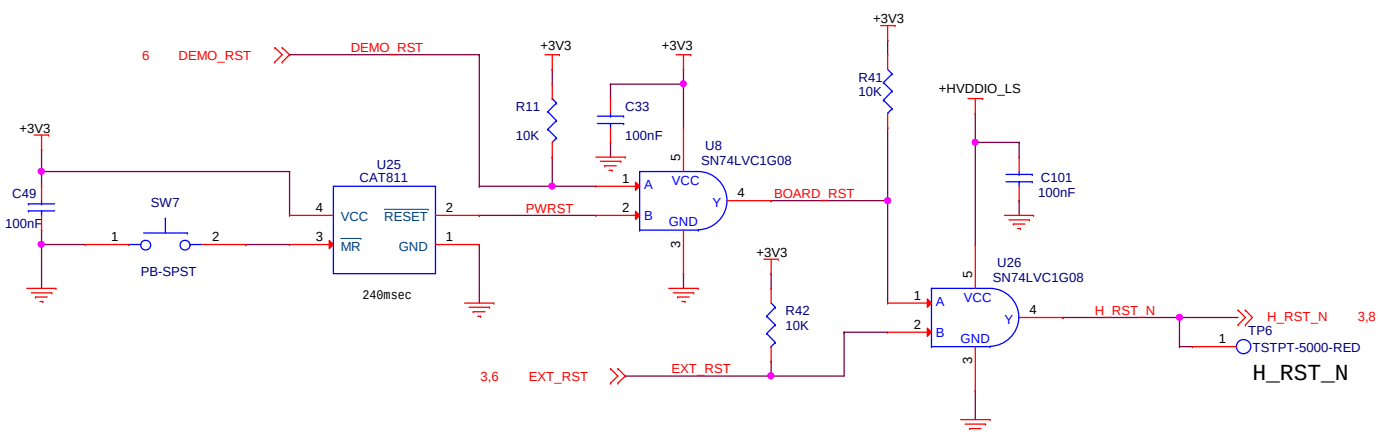
Host I2C BUFFER



Sensor I2C BUFFER



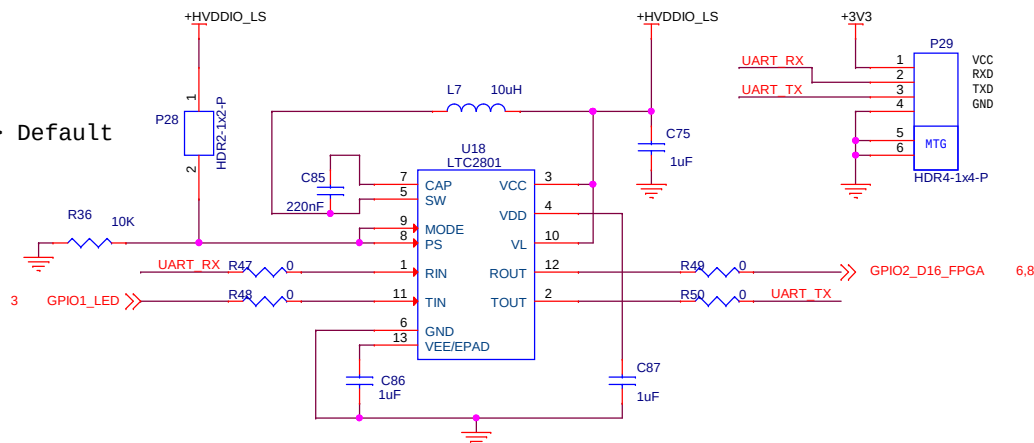
RESET CIRCUIT



Primary EEPROM Address Switch Settings:

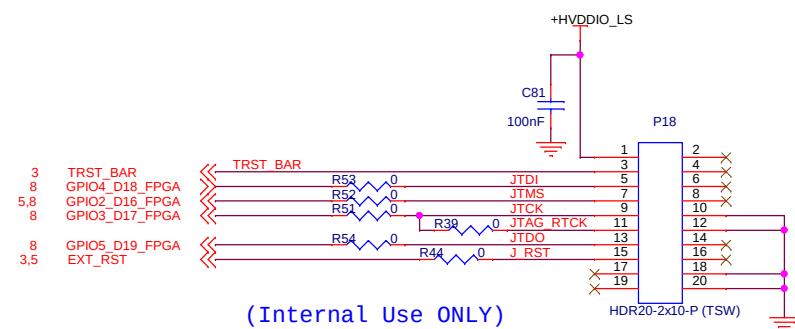
A2=HIGH, A1=LOW, A0=HIGH; Address => 0xAA (default)
A2=LOW, A1=LOW, A0=HIGH; Address => 0xA2
A2=LOW, A1=HIGH, A0=HIGH; Address => 0xA6
A2=HIGH, A1=HIGH, A0=HIGH; Address => 0xAE

P28:
Open -> Default

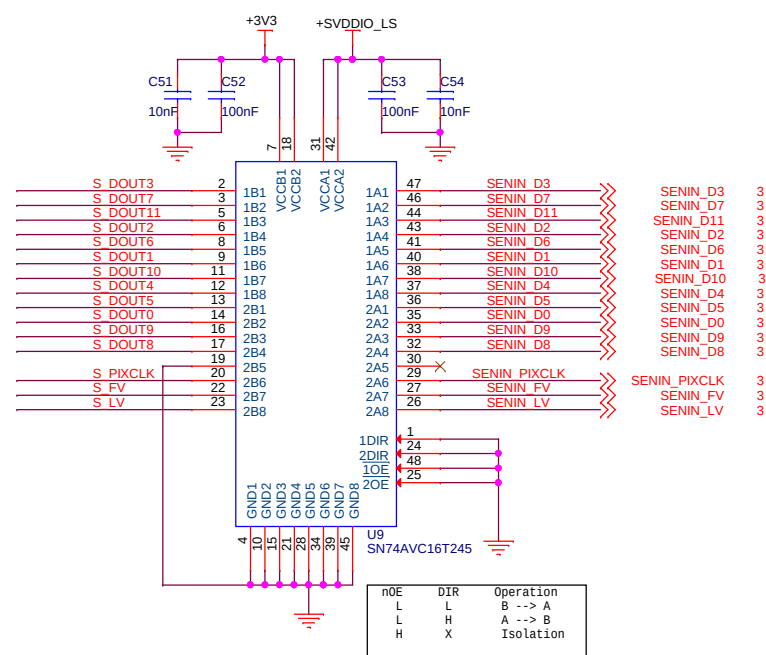


4,6,7	+5V0		+5V0
3,4	+VDD_REG		+VDD_REG
3,4	+SVDDIO		+SVDDIO
3,4	+HVDDIO		+HVDDIO
3,4,6,7	+3V3		+3V3
4,6	+SVDDIO_LS		+SVDDIO_LS
3,4,6,7	+HVDDIO_LS		+HVDDIO_LS
3,4	+OTPM_VCC		+OTPM_VCC
4,8	+VCCIO		+VCCIO
4,7,8	+3V3_HVCCIO		+3V3_HVCCIO
4,8	+1V2_VCCINT		+1V2_VCCINT
4,8	+2V5_VCCA		+2V5_VCCA

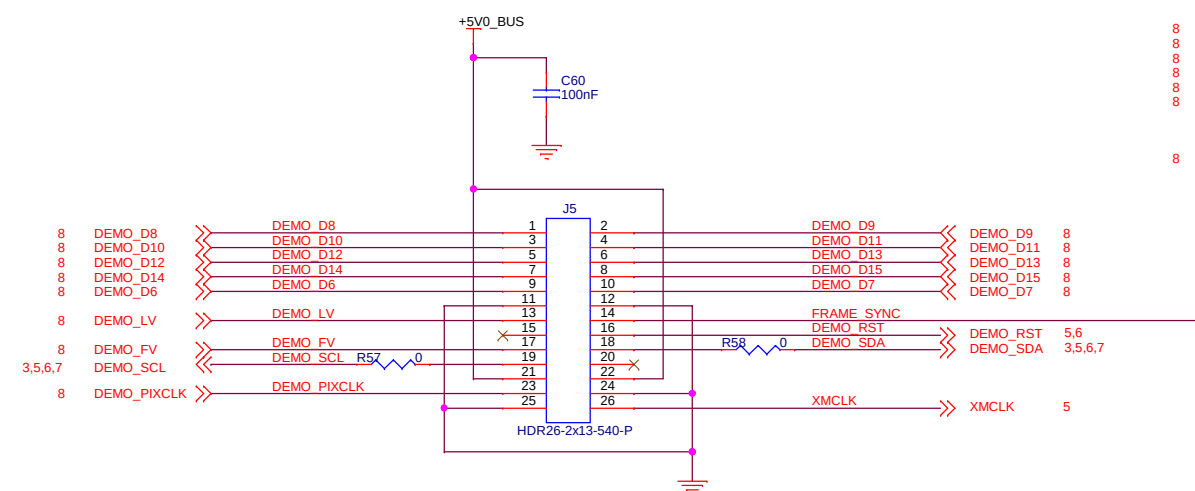
External Interface



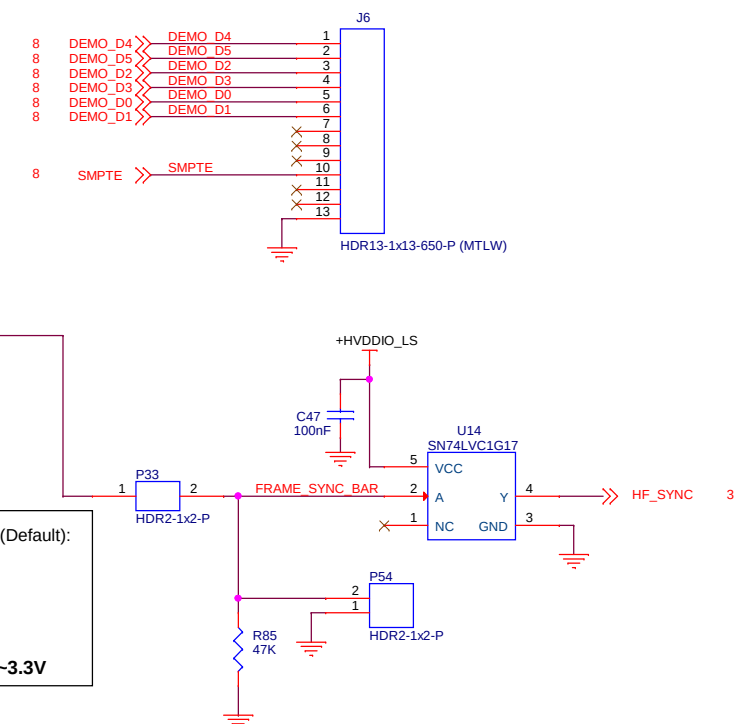
Parallel Data Level Shifter (HeadBoard -> AP0101 board)



Demo2X I/F



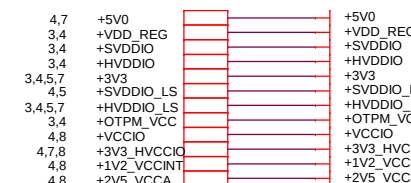
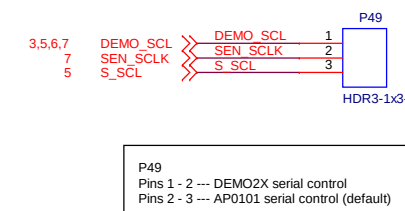
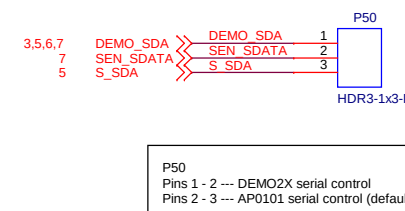
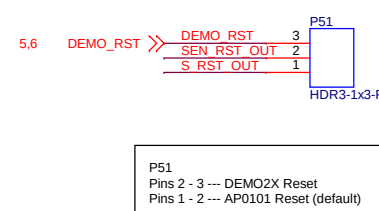
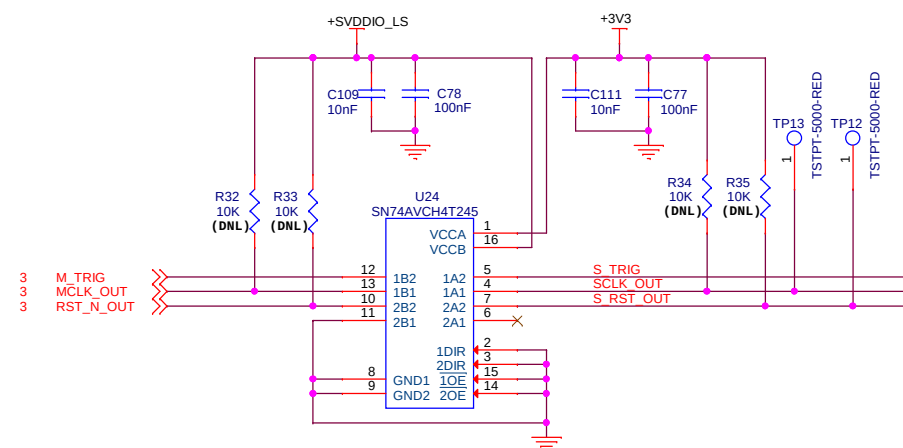
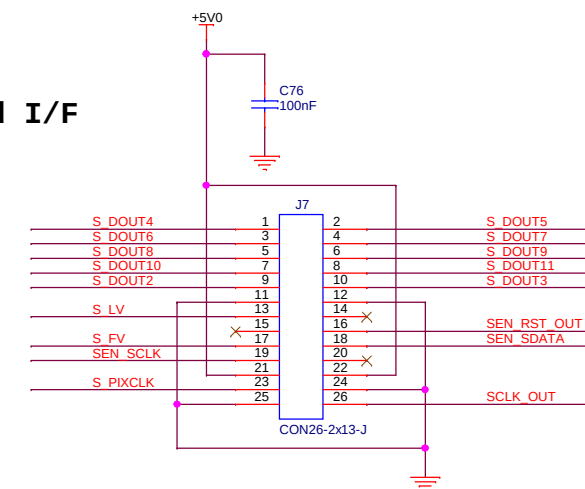
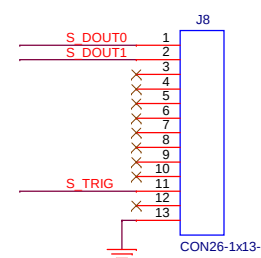
Demo2X I/F



DEMO2X access to SYNC signal (Default):
Close P33 --> Pin 1-2
Open P54

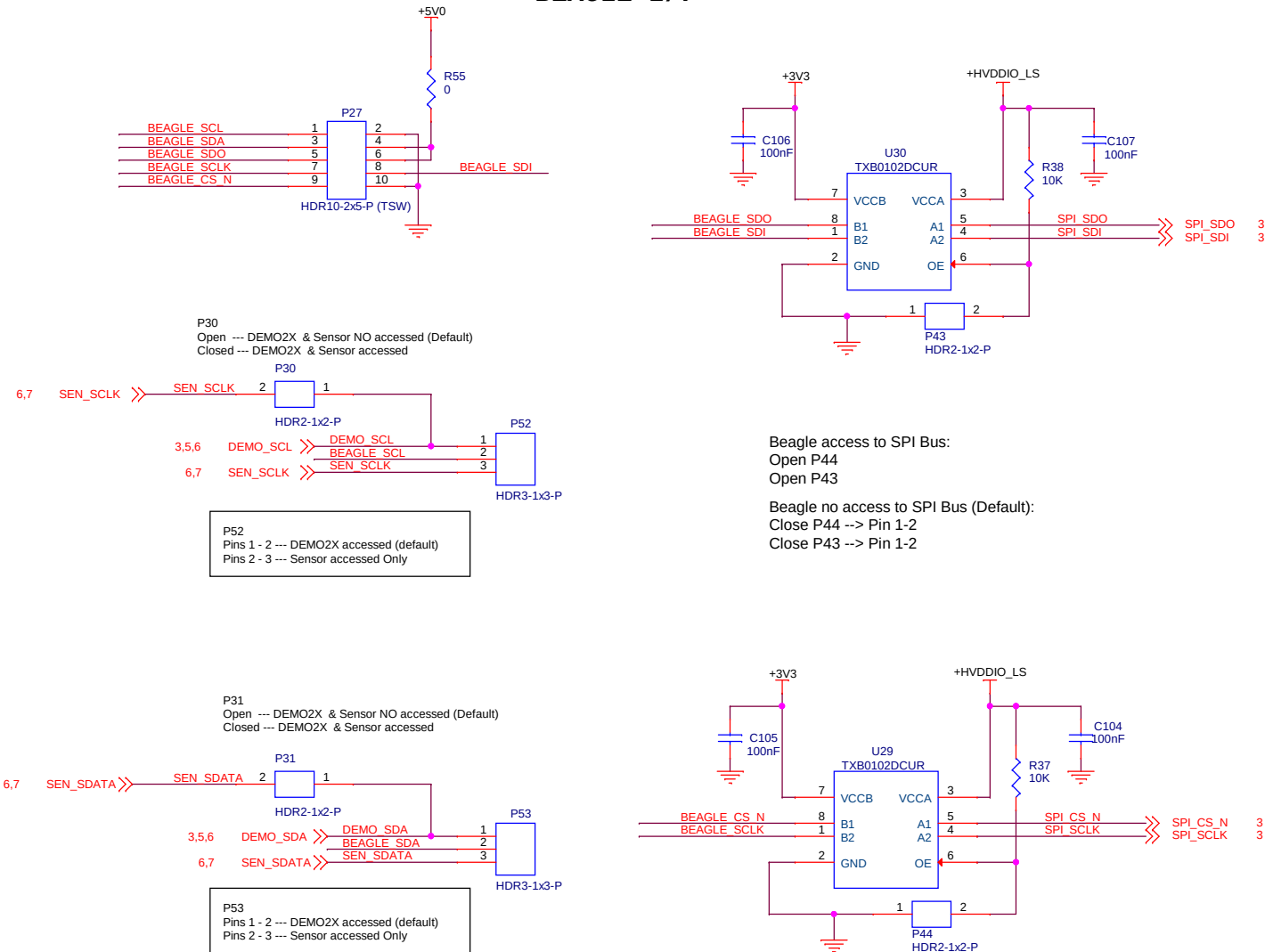
EXT access to SYNC signal:
Open P33
Input Signal P54 --> Pin 2
Input signal Voltage => 2.8V ~3.3V

Headboard I/F

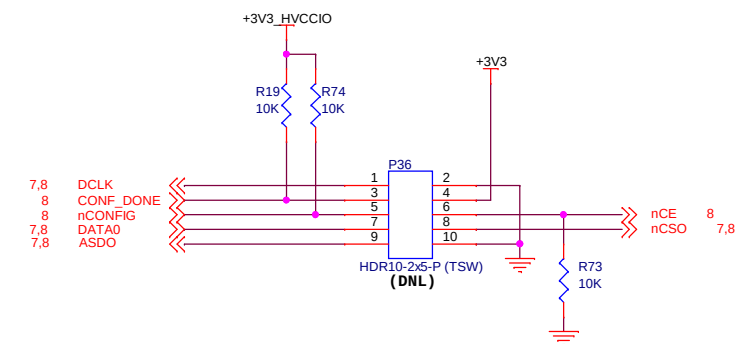
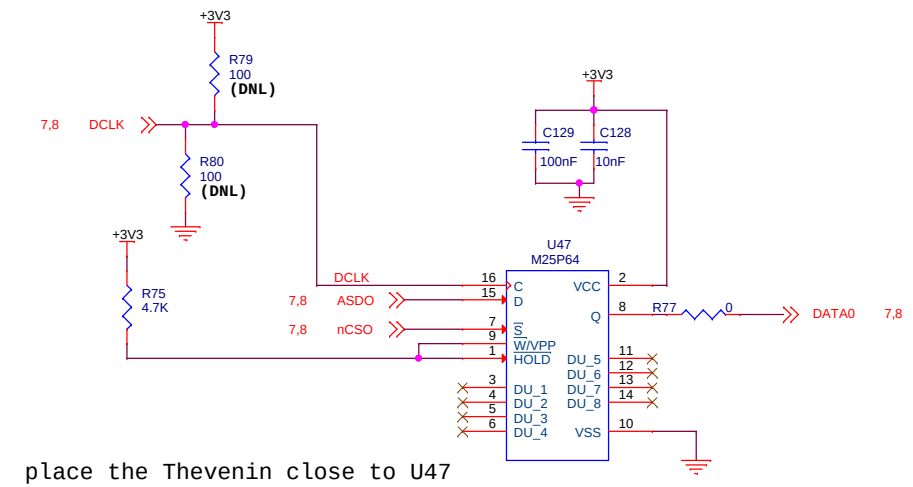


BEAGLE/FPGA EXT I/F

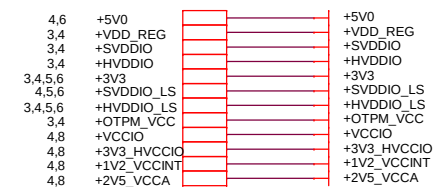
BEAGLE I/F



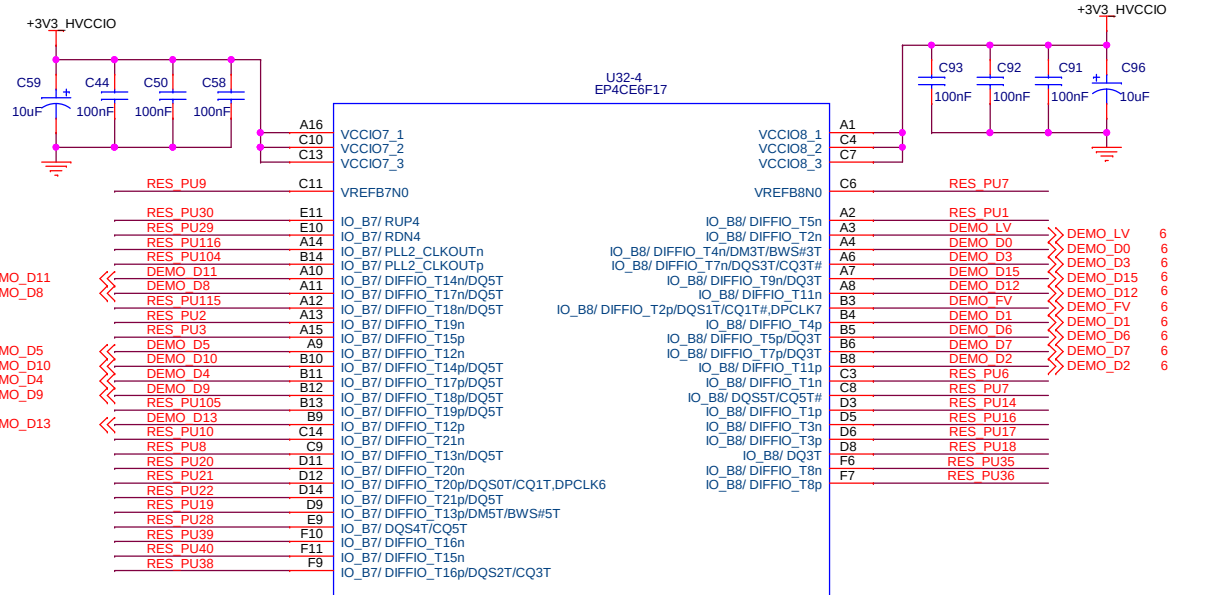
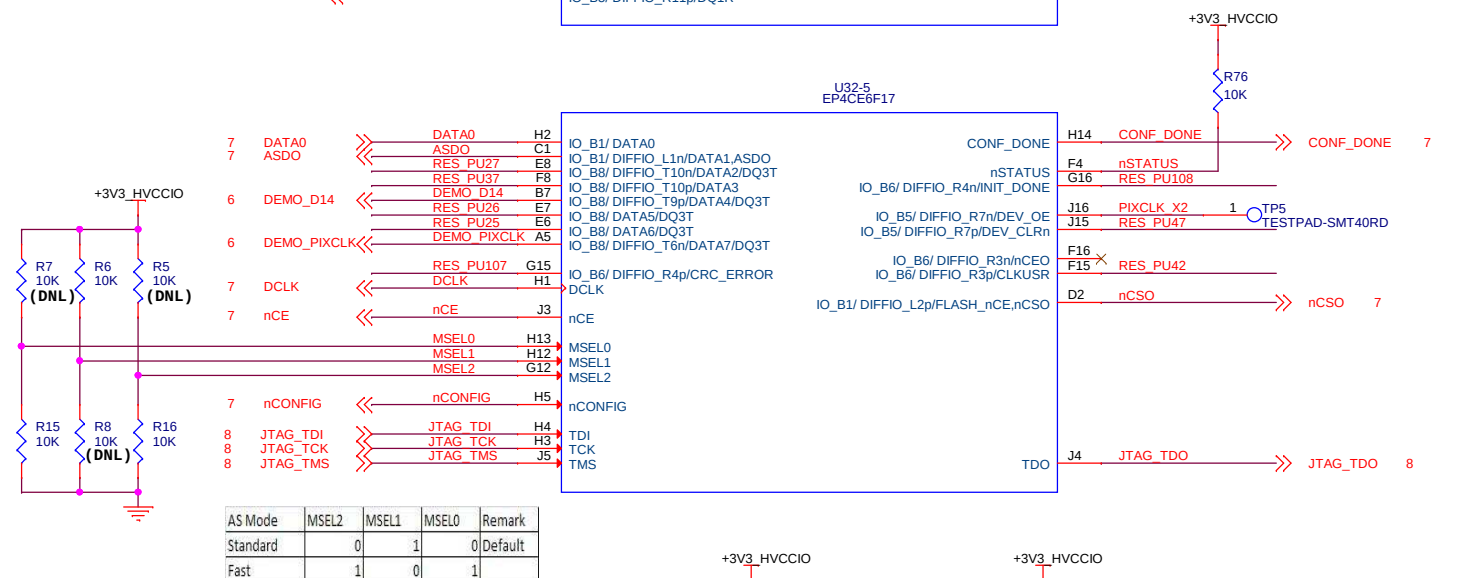
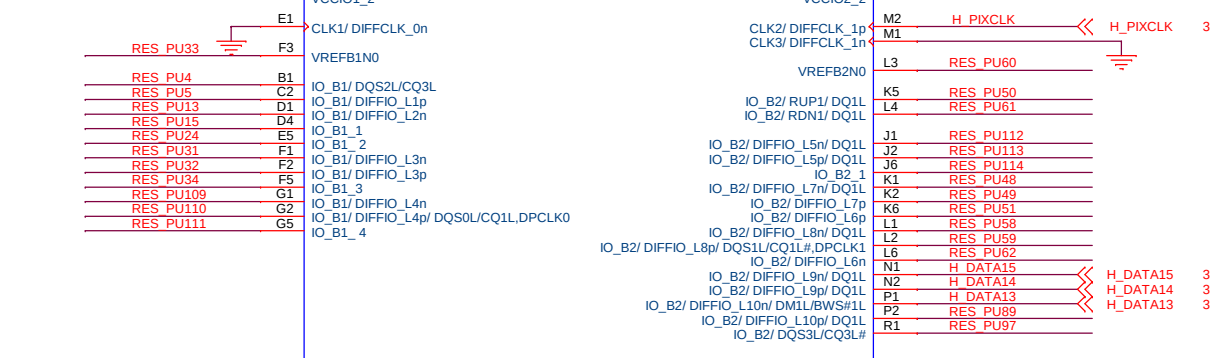
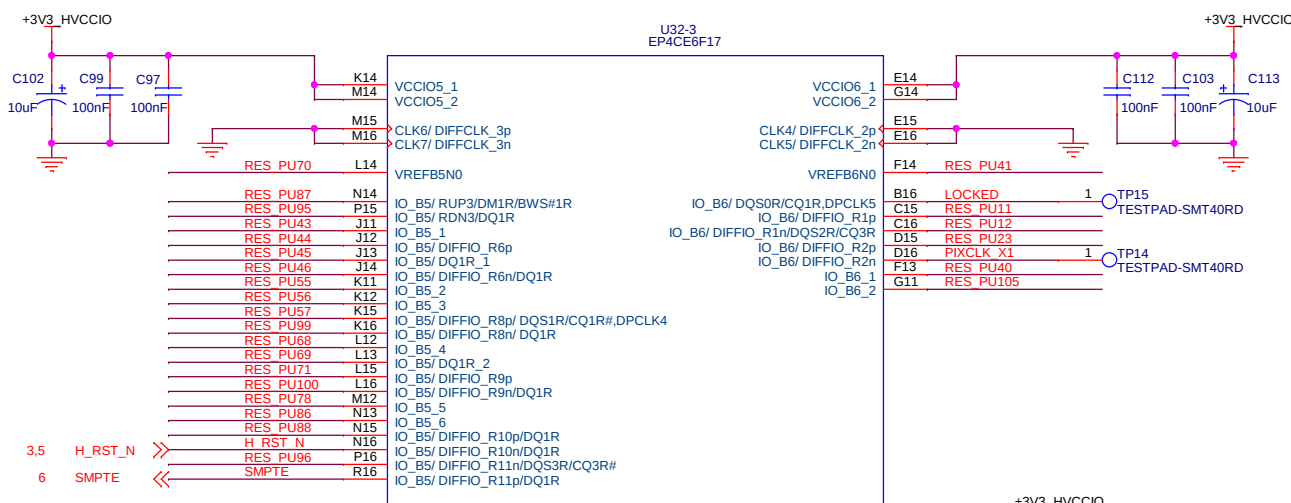
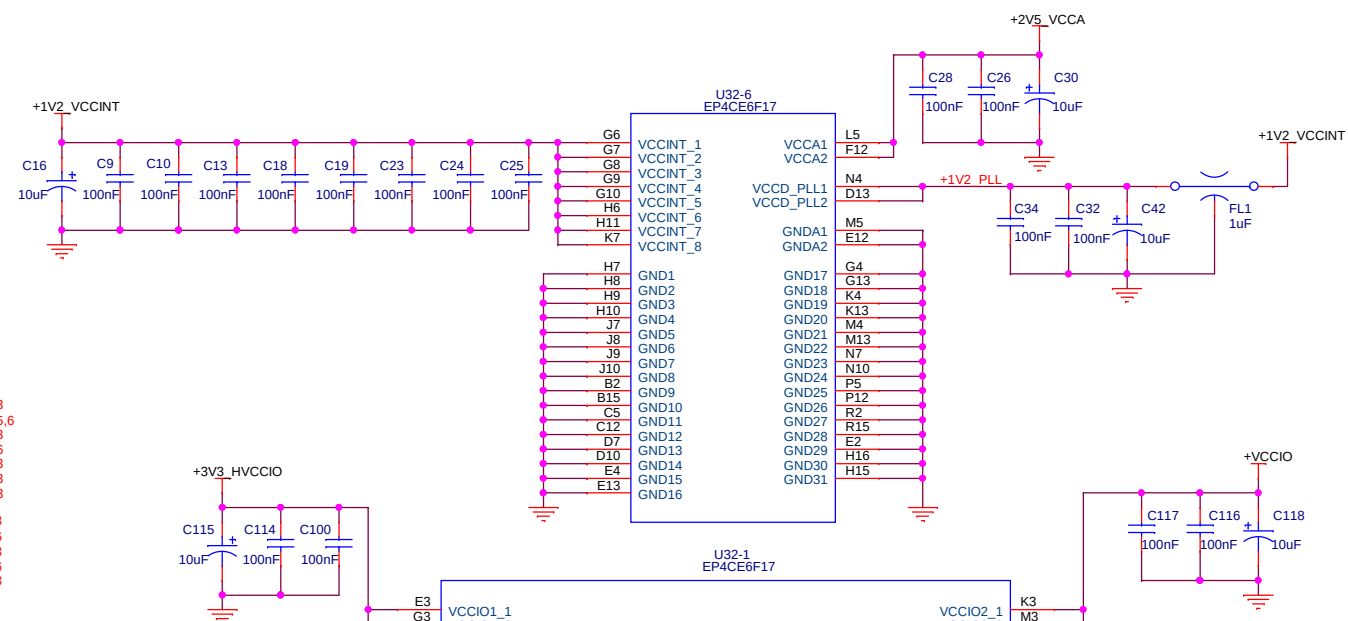
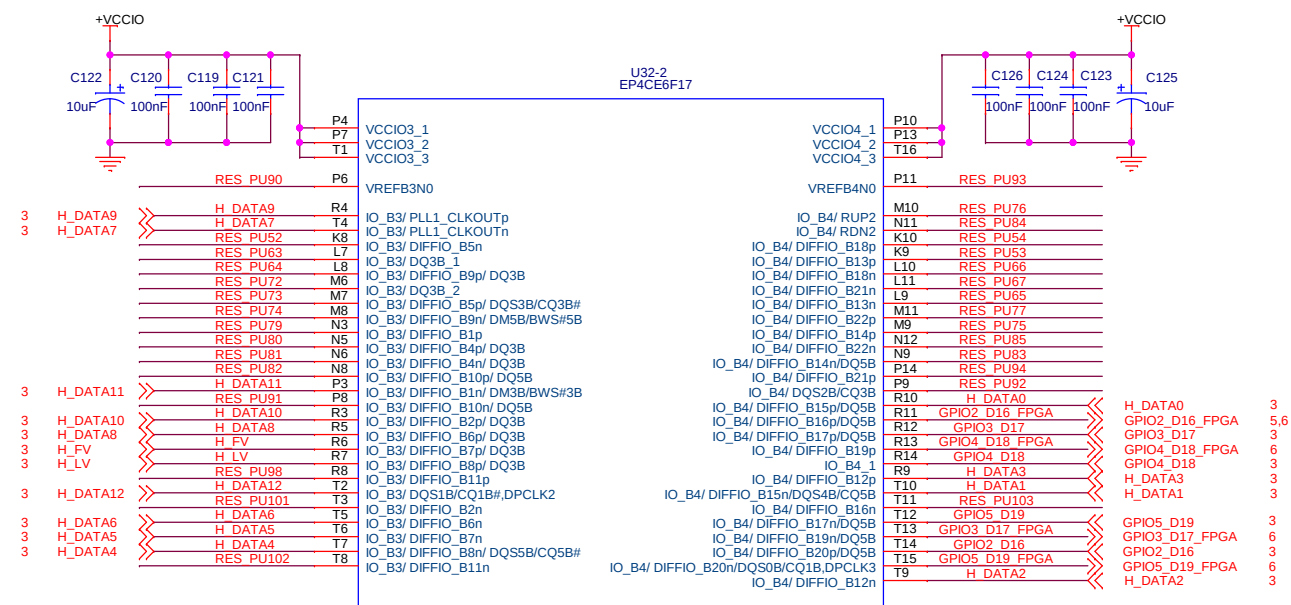
FPGA Memory I/F



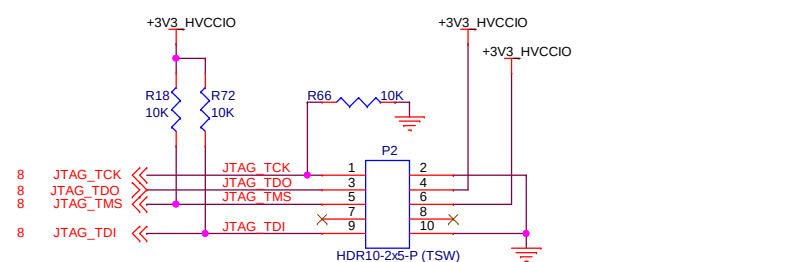
Beagle Serial configuration			
Header	Pin condition	Signal connection	Remark
P52/P53	Pin 1-2	BEAGLE_Serial => DEMO_Serial	Beagle master control AP0101, Remove R58/R57 DEMO2X master remove
P52/P53	Pin 2-3	BEAGLE_Serial => SEN_Serial	Beagle master control Sensor, no control on AP0101
P52/P53 & P49/P50	Pin 1-2 OPEN for P49/P50	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, Open P50/P49 AP0101 master remove to Sensor
P52/P53 & P30/P31	Pin 1-2 Close for P30/P31	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, AP0101 serial to Sensor still connected



FPGA Interface



AS Mode	MSEL2	MSEL1	MSEL0	Remark
Standard	0	1	0	Default
Fast	1	0	1	

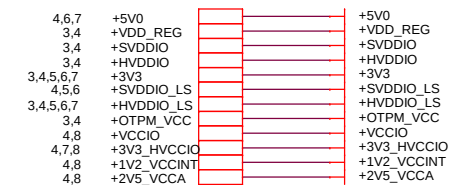


4,6,7	+5V0					+5V0
3,4	+VDD_REG					+VDD_REG
3,4	+SVDDIO					+SVDDIO
3,4	+HVDDIO					+HVDDIO
3,4,5,6,7	+3V3					+3V3
3,4,5,6,7	+SVDDIO_LS					+SVDDIO_LS
3,4,5,6,7	+HVDDIO_LS					+HVDDIO_LS
3,4	+OTPM_VCC					+OTPM_VCC
3,4	+VCCIO					+VCCIO
4,7	+3V3_HVCCIO					+3V3_HVCCIO
4	+1V2_VCCINT					+1V2_VCCINT
4	+2V5_VCCA					+2V5_VCCA



Configuration Setting

Beagle Serial configuration			
Header	Pin condition	Signal connection	Remark
P50/P49	Pin 2-3	AP0100_Serial => SEN_Serial	AP0101 master control Sensor
P50/P49	Pin 2-3	AP0100_Serial => SEN_Serial	AP0101 master control Sensor
P52/P53	Pin 1-2	BEAGLE_Serial => DEMO_Serial	Beagle master control AP0101, Remove R58/R57 DEMO2X master
P52/P53	Pin 2-3	BEAGLE_Serial => SEN_Serial	Beagle master control Sensor, no control on AP0101, Open
P52/P53 & P49/P50	Pin 1-2	BEAGLE_Serial => DEMO_Serial	Beagle master control AP0101, Open P50/P49 AP0101 master remove to Sensor, Open P30/P31
	OPEN for P49/P50		
P52/P53 & P30/P31	Pin 1-2	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, AP0101 serial to Sensor still connected
	Close for P30/P31		
P49/P50,P52/P53 & P30/P31	Pin 1-2	BEAGLE_Serial => DEMO_Serial/SEN_Serial	Beagle master control AP0101/Sensor, Open P50/P49 AP0100 master remove to Sensor
	Close for P30/P31		
	OPEN for P49/P50		
Auto-configuration			
Header	Pin condition	Signal Condition	Remark
P43/P44	P44 = Short 1-2/P43 = Short 1-2	Disable U30/U29	Beagle no access to SPI Bus
P5/P45	P5 = Short 1-2/P45 = Open	Host Mode (SPI_SDI = GND)	SPI_SDI Table:
	P5 = Open/P45 = Open	Flash Mode (SPI_SDI = Flash/EEPROM Data)	SPI_SDI => High Impedance (Auto-config)
	P5 = Short 1-2/P45 = Short 1-2	Auto-Configuration (SPI_SDI = High Impedance)	SPI_SDI => Data (Flash Mode)
	P5 = Open/P45 = Open	Host/Flash/Auto-Config	SPI_SDI => Serial Control Mode type
P43/P44	P43/P44 = Short 1-2	SP1_SDO/SDI/SCLK/CS_N	Disable Beagle SPI access



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