DATA SHEET

TJA1010
Octal Low Side Driver (OLSD)

Product specification
Supersedes data of 1998 Feb 09
File under Integrated Circuits, IC18

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Philips Semiconductors

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Octal Low Side Driver (OLSD) TJA1010

FEATURES

- Eight independent low side drivers
- Small outline/medium power package for surface mounting, SO28 (20 + 4 + 4)
- Serial input control by writing to internal shift register
- Overvoltage clamping for each driver
- Each driver protected against short-circuited load
- Undervoltage shutdown
- All logic pins CMOS microcontroller compatible
- Standby mode for minimum current consumption
- Two status outputs indicating short-circuited load and open load respectively at any driver stage
- Channel selective diagnostic information available by reading from internal shift register
- Serial output allows cascading of several OLSDs
- Outputs can be used in parallel
- Two-stage thermal protection
- Power-on reset.

GENERAL DESCRIPTION

The TJA1010 is an octal low side driver for relays in automotive applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	operating	5.5	–	25	V
		load dump	–	–	50	V
$V_{o(clamp)}$	drain-to-source clamp voltage	I_o = 20 mA	50	60	70	V
$R_{o(on)}$	on resistance	I_o = 0.2 A	–	–	3	Ω
I_o	output current	continuous at all outputs; T_{amb} = 85 °C	–	–	0.2	A

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1010T	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

BLOCK DIAGRAM

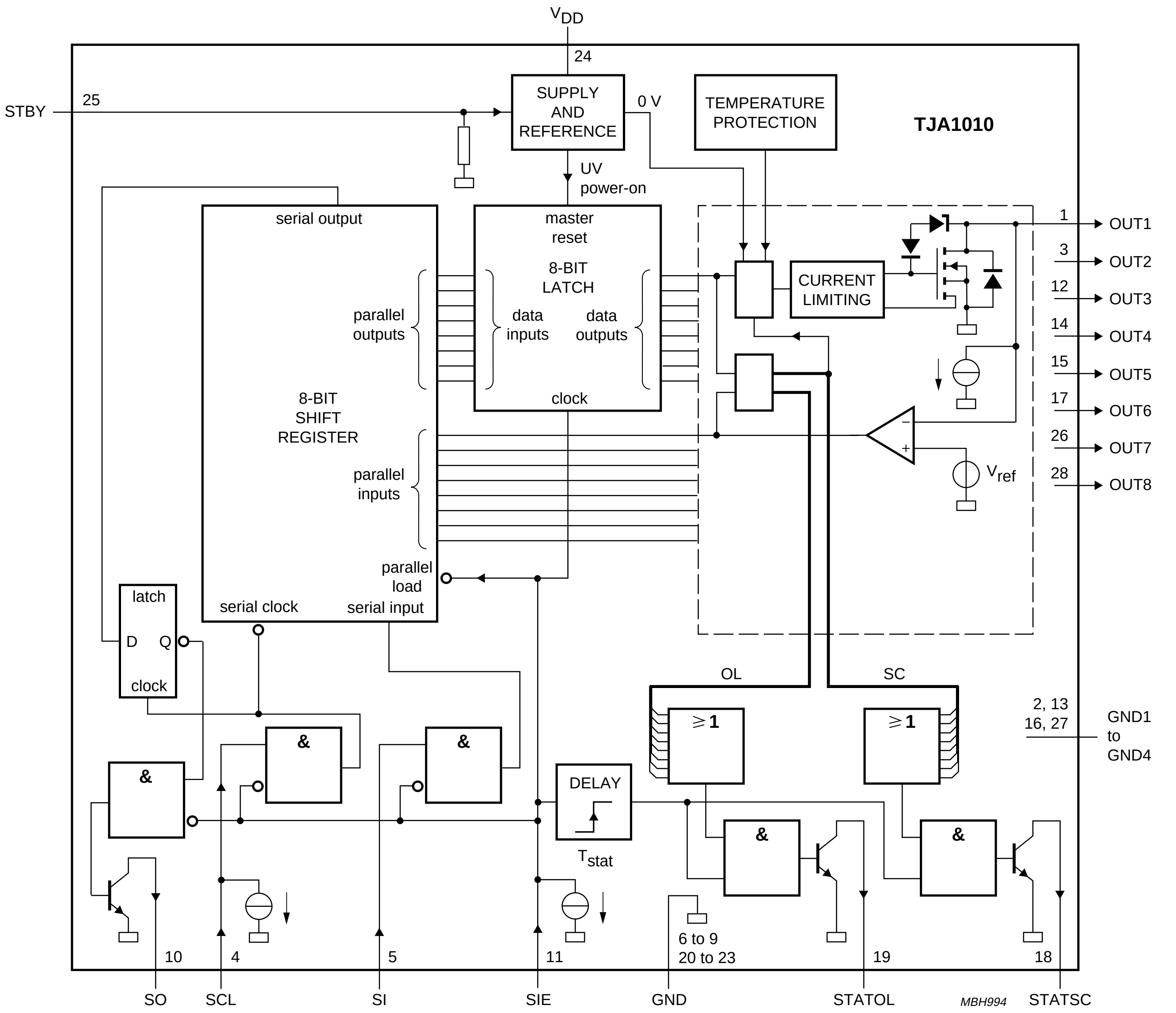


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
OUT1	1	output 1
GND1	2	ground 1
OUT2	3	output 2
SCL	4	serial clock input
SI	5	serial input
GND	6	ground
GND	7	ground
GND	8	ground
GND	9	ground
SO	10	serial output
SIE	11	serial input enable
OUT3	12	output 3
GND2	13	ground 2
OUT4	14	output 4
OUT5	15	output 5
GND3	16	ground 3
OUT6	17	output 6
STATSC	18	status output short-circuited load
STATOL	19	status output open load
GND	20	ground
GND	21	ground
GND	22	ground
GND	23	ground
V_{DD}	24	supply voltage
STBY	25	standby input
OUT7	26	output 7
GND4	27	ground 4
OUT8	28	output 8

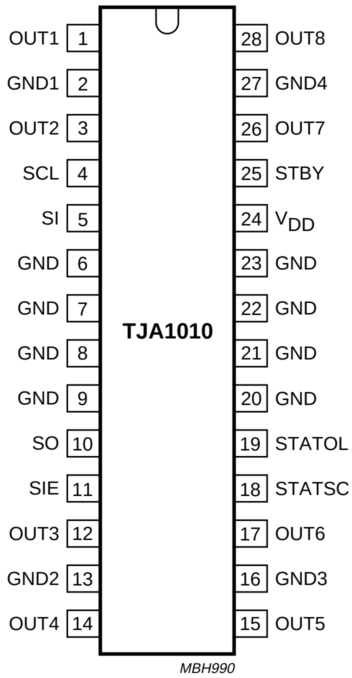


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION (see Figs 1, 3 and 4)

This octal low side driver is intended to drive relays in automotive applications. It is optimized to withstand the wide temperature and supply voltage range that is typical for this application area. It consists of 8 protected outputs, including diagnostic functions, controlled by a serial interface. These outputs can be used in parallel without the need for additional components.

Serial control interface

Serial control of the drivers is provided by an 8-bit shift register with parallel outputs and an 8-bit latch which controls the DMOS output stages. Using this configuration the number of pins needed for control of the eight drivers is reduced to three; Serial Input (SI), Serial CLock (SCL) and Serial Input Enable (SIE). When pin SIE is LOW, serial data at pin SI is shifted into the shift register at each HIGH-to-LOW transition at the SCL pin and serial data is shifted out at the Serial Output (SO) pin at a LOW-to-HIGH transition on the SCL pin. The last bit read in before a LOW-to-HIGH transition at the SIE pin is bit D8. A HIGH level at the SI pin causes a driver to switch-on. With a LOW-to-HIGH transition at the SIE pin, parallel output data in the shift register is written to the 8-bit latch, which controls the DMOS outputs. When SIE is HIGH, signals at pins SI, SCL and SO are disabled. For pin SO this results in a HIGH level because pin SO is an open-collector output.

Diagnostic interface

The OLSD detects open loads and short-circuited loads at each driver stage by comparing its output voltages (V_o) to a reference voltage (V_{ref}). To allow distinction between short-circuit and open load conditions, a short-circuit is detected for $V_o > V_{ref}$ in the on-state, while an open load is detected for $V_o < V_{ref}$ in the off-state of a driver stage.
In both cases the corresponding status pin is set to a LOW level and the respective bit in the shift register will be inverted.

With a HIGH-to-LOW transition at the SIE pin, the status of the eight outputs is written into the shift register. The actual contents (the control byte eventually modified by errors) can be read out via pin SO. Comparing this byte with the original control byte previously written, faults can be localized and identified (e.g. open load at driver stage number 5).

Protection of DMOS outputs

Each driver contains a DMOS power FET. The drivers are protected against overvoltage, short-circuit and overtemperature conditions.

An overvoltage clamp circuit at each driver causes the respective DMOS power FET to turn partially on, if its drain-to-source voltage level exceeds the clamp level [$V_{o(clamp)}$]. Consequently each driver can withstand voltage peaks caused by turning off inductive loads, such as relays coils without freewheel diodes. It should be noted that if outputs are used in parallel the amount of inductive energy which can be handled will not increase but will remain equal to that of a single output.

Each driver is protected against a short-circuited load by current limiting. In the event of a short-circuited load at a driver stage, the current will be limited and the HIGH level of its drain-to-source voltage will force the comparator output to go LOW. This in turn will set the STATSC pin to a LOW level.

A two-stage temperature protection circuit is included to protect the device against overheating caused by high dissipation in the output transistors.

When the temperature exceeds the overtemperature threshold level, it will switch-off those outputs with a short-circuit condition for the duration of the overtemperature condition. The status and diagnostic function will not be influenced.

If the chip temperature still rises and exceeds the emergency threshold level, the emergency shutdown will become active and shut down all of the outputs until the temperature drops below the overtemperature threshold.

The outputs are fully protected against short-circuit to battery conditions for the whole supply voltage range.

To protect the outputs against device threatening dissipation peaks, the overtemperature control is extended with local power dissipation sensors. If one or more outputs dissipate too much power all outputs with a short-circuit condition will be switched off for the duration of the local overtemperature condition.

To protect the outputs against high dissipation during load dump, an overvoltage protection is included. This will switch-off those outputs with a short-circuit condition if the supply voltage exceeds the overvoltage threshold $V_{DD(0\ V)}$ for the duration of the overvoltage condition.

The diagnostic and status information will not change due to the interference of the overvoltage and overtemperature protections.

To avoid a false LOW signal at the SC pin due to switching transients at the DMOS outputs, the SC pin is disabled for a sufficient delay time whenever a new input control byte has been written into the 8-bit latch with a LOW-to-HIGH transition of SIE.

Other features

When using several OLSDs, input control and diagnostics can be provided, as described above, without spending further microcontroller pins by cascading, i.e. connecting the SO pin of one OLSD to the SI pin of the following OLSD.

A standby input (STBY) pin allows the off state current consumption in the OLSD to be minimized. Thus the OLSD can be connected permanently to a battery.

A power-on reset ensures a defined off state for all drivers when the device is switched on i.e. by switching on the power supply or by activating the device via the STBY pin. Thus the STBY input can also be used as a reset pin.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	continuous	0	25	V
		transient	0	50	V
V_n	input voltage at pins SI, SCL and SIE		0	5.5	V
$V_{I(STBY)}$	input voltage at pin STBY		0	7	V
$V_{o(STAT)}$	output voltage at pins STATOL and STATSC		0	18	V
$V_{o(SO)}$	output voltage at pin SO		0	18	V
I_o	output current		internally limited		
$I_{o(con)}$	continuous output current	T_j = 135 °C	–0.2	+0.2	A
		T_j = 95 °C	–0.3	+0.3	A
$I_{clamp(rep)}$	repetitive inductive turn-off current per output	T_j = 135 °C; note 1	see Fig.5		A
$E_{clamp(rep)}$	repetitive inductive turn-off energy per output	T_j = 95 °C; notes 1 and 2	–	5	mJ
$E_{clamp(nrep)}$	non-repetitive inductive turn-off energy per output	T_j = 95 °C; notes 1 and 3	–	60	mJ
T_{vj}	virtual junction temperature		–40	+135	°C
T_{stg}	storage temperature		–55	+150	°C
V_{esd}	electrostatic handling voltage	human body model	–	3	kV
		machine model	–	300	V

Notes

1. The amount of E_{clamp} per output can **NOT** be added if outputs are used in parallel. Thus, if two or more outputs are used in parallel it can handle the E_{clamp} of one output.
2. Defined for t_{clamp} = 1 ms.
3. Defined for t_{clamp} = 5 ms.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-amb)}$	from junction to ambient in free air	note 1	55	K/W
$R_{th(j-sp)}$	from junction to soldering point of ground pins 6 to 9 and 20 to 23	note 2	17	K/W

Notes

1. Printed on an FR-4 board with minimum foot print.
2. Power uniformly divided over all outputs.

CHARACTERISTICS

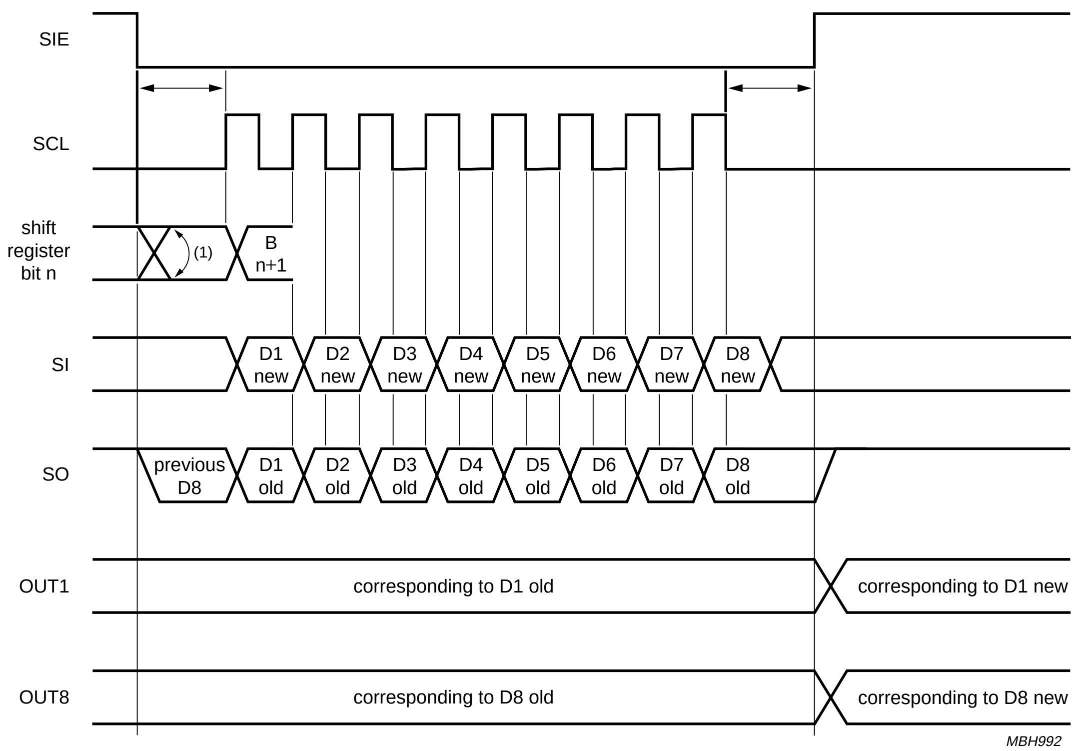
T_j = –40 to +135 °C; V_{DD} = 11 to 13.5 V; $V_{bat(max)} = V_{DD}$ + 1.5 V. All voltages are defined with respect to ground. Positive currents flow into the IC. All parameters are guaranteed over the temperature range by design, but only 100% tested at T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	supply current	I_o = 0 mA; V_{STBY} > 3 V	–	–	5	mA
		V_{STBY} < 1 V; V_{DD} = 13 V; T_j = –40 to +85 °C	–	–	10	µA
$V_{DD(UV)}$	undervoltage shutdown threshold		2	–	4.3	V
$V_{DD(0V)}$	overvoltage protection threshold		25	–	33	V
$V_{o(clamp)}$	output clamp voltage	I_o = 20 mA	50	60	70	V
I_{LO}	output leakage current (one output)	off-state, V_o = 13 V; standby	–		10	µA
		off-state, V_o = 13 V; operational	70	–	210	µA
		off-state, V_o = 1 V; operational	40	–	180	µA
$I_{o(lim)}$	output current limit (one output)	on-state	0.3	–	0.55	A
R_o	output resistance (one output)	I_o = 0.2 A; V_{DD} = 13 V; T_j = 135 °C	–	–	3	Ω
		I_o = 0.2 A; V_{DD} = 13 V; T_j = 25°C	–	–	2.5	Ω
		I_o = 0.1 A; V_{DD} = 5.5 V; see Fig.6	–	–	10	Ω
V_{ref}	open load/short-circuit reference voltage	note 1	1	–	1.9	V
$\delta I_o/\delta t$	maximum rise and fall time of output current	V_{DD} = 13 V; R_L = 100 Ω; note 2	–	–	100	mA/µs
V_{IH}	HIGH-level input voltage at pins SI, SCL, SIE and STBY		3	–	–	V
$V_{i(hys)}$	input voltage hysteresis at pins SI, SCL and SIE	note 2	0.2	–	1.2	V
V_{IL}	LOW-level input voltage at pins SI, SCL and SIE		–	–	0.8	V
$V_{IL(STBY)}$	LOW-level input voltage at pin STBY		–	–	1	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_i	input current at pins SCL and SIE	V_i = 3 V	20	–	60	µA
I_{LI}	input leakage current at pins SI, SIE and SCl	off-state; V_i = 3 V; T_j = 85 °C; V_{STBY} < 1 V	–	–	5	µA
$R_{i(STBY)}$	input resistance at pin STBY	V_i = 1 V; T_j < 85 °C	40	–	150	kΩ
$I_{i(STBY)}$	input current at pin STBY	V_i = 3 V	20	–	60	µA
$V_{STAT(L)}$	status LOW voltage	$I_{STAT(L)}$ = 1.6 mA	–	–	0.4	V
$V_{SO(L)}$	serial output LOW voltage	I_{SO} = 1.6 mA	–	–	0.4	V
$I_{LO(SO)}$	output leakage current at pin SO and status outputs	off-state; V_o = 5 V; V_{STBY} < 1 V; T_j < 85 °C	–	–	10	µA
f_{clk}	clock frequency		–	–	1	MHz
$t_{W(SCL)}$	SCL positive pulse width	HIGH-to-LOW transition	500	–	–	ns
$t_{d(SIE-SCL)}$	delay time from SIE HIGH to SCL LOW		100	–	–	ns
$t_{su(SIE-SCL)}$	set-up time from SIE LOW to SCL HIGH		250	–	–	ns
$t_{d(SCL-SO)}$	delay time from SCL HIGH to SO valid	note 3	–	–	250	ns
$t_{su(SI-SCL)}$	set-up time from SI to falling edge of SCL		150	–	–	ns
$t_{h(SCL-SI)}$	hold time from falling edge of SCL to SI		150	–	–	ns
$t_{h(SCL-SIE)}$	hold time from SCL LOW to SIE HIGH		250	–	–	ns
$t_{su(STBY)}$	STBY set-up time from STBY HIGH to SIE LOW		100	–	–	µs
$t_{h(STBY)}$	STBY hold time from SIE HIGH to STBY LOW		10	–	–	µs
$t_{d(STAT)}$	delay time for status pin enable		40	100	250	µs
$T_{th(otc)}$	threshold overtemperature control		–	170	–	°C
$T_{th(ets)}$	threshold emergency temperature shutdown		–	190	–	°C

Notes

1. Open load is indicated for $V_o < V_{ref}$ in the off-state, short-circuited load is indicated for $V_o > V_{ref}$ in the on-state.
2. Guaranteed by design.
3. Delay caused by load excluded.



(1) Inverting only when error (open load/short-circuit).

Fig.3 Serial interface timing.

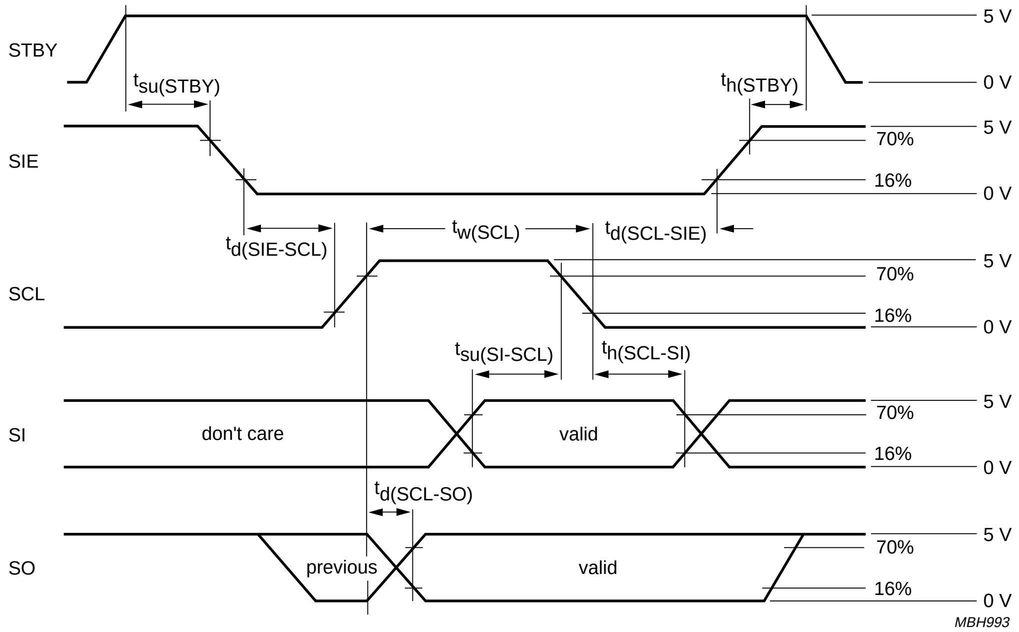
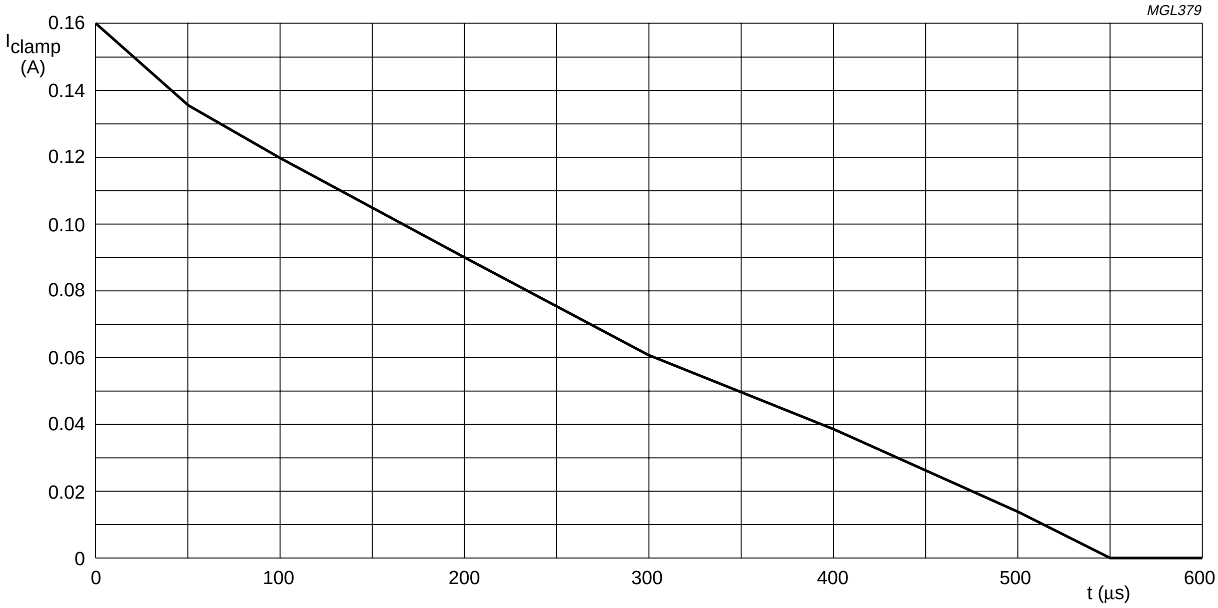


Fig.4 Input and output waveform timing.



The curve is based on behaviour of relays; Siemens A4001-X40.

Fig.5 Maximum current during inductive turn-off (T_{amb} = 85 °C).

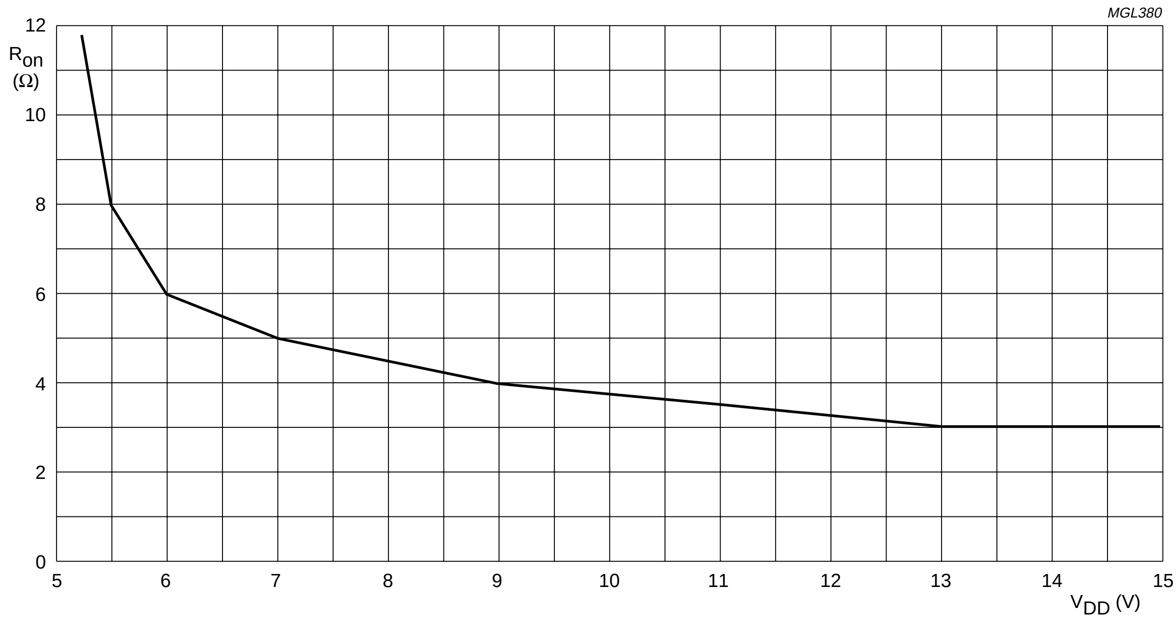


Fig.6 Maximum on-resistance as a function of supply voltage.

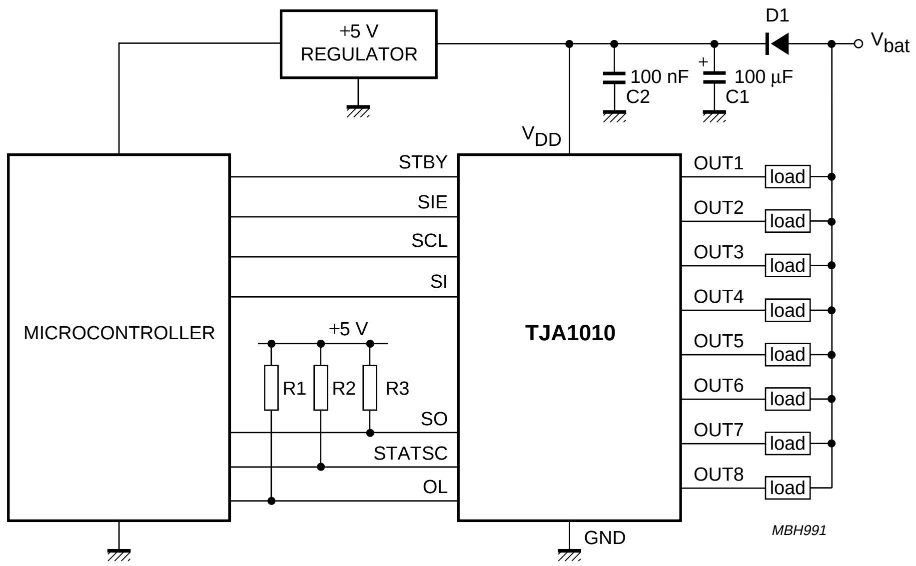
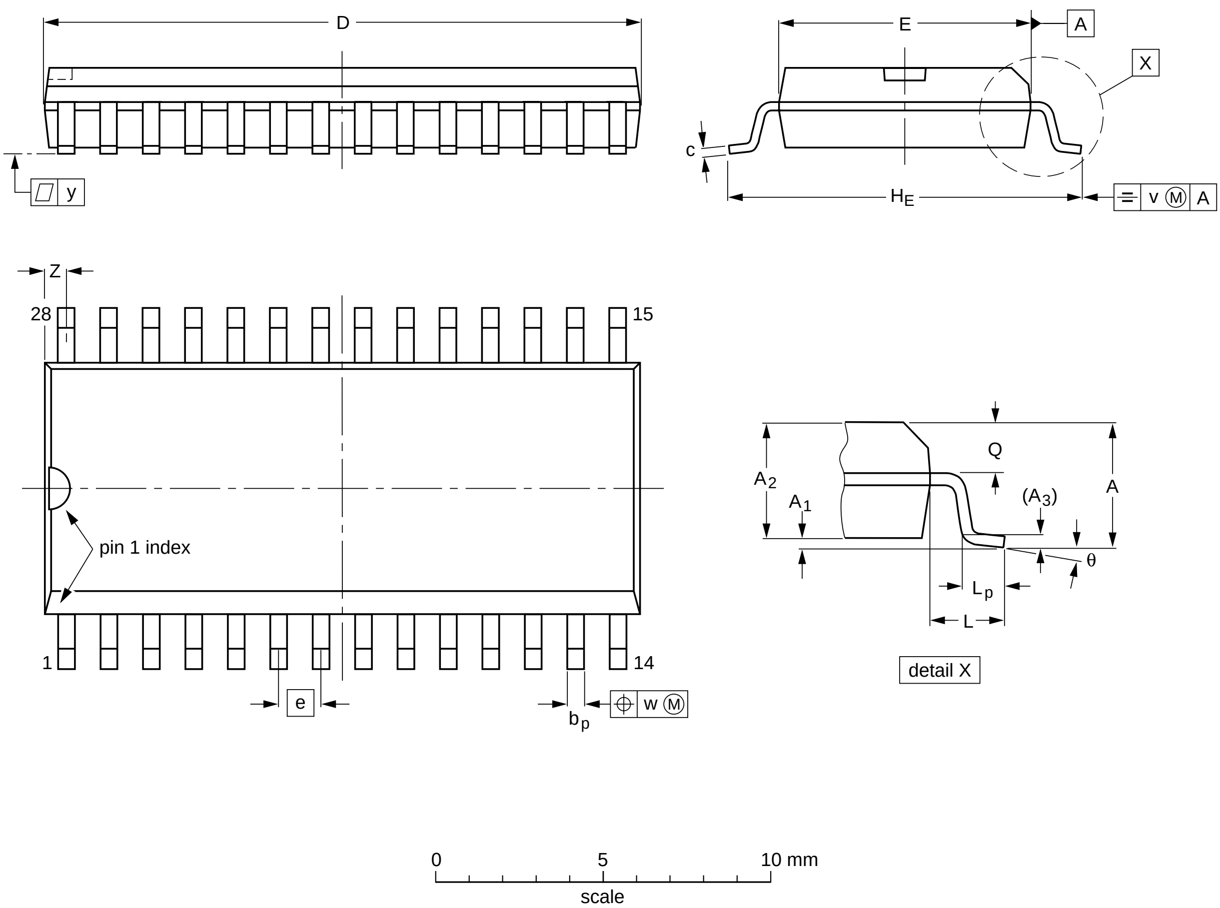


Fig.7 Application example.

PACKAGE OUTLINE

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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