DATA SHEET

TDA8552T; TDA8552TS

2 x 1.4 W BTL audio amplifiers with digital volume control and headphone sensing

Product specification
Supersedes data of 1998 Jun 02

2002 Jan 04

2 x 1.4 W BTL audio amplifiers with digital volume control and headphone sensing

TDA8552T; TDA8552TS

FEATURES

- One pin digital volume control (for each channel)
- Volume setting with up/down pulses
- Auto repeat function on volume setting
- Headphone sensing
- Maximum gain set by selection pin
- Low sensitivity for EMC radiation
- Internal feedback resistors
- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{DD} and across the load
- Thermally protected.

APPLICATIONS

- Portable consumer products
- Notebook computers
- Communication equipment.

GENERAL DESCRIPTION

The TDA8552T is a two channel audio power amplifier that provides an output power of 2×1.4 W into an 8 Ω load using a 5 V power supply. The circuit contains two BTL power amplifiers, two digital volume controls and standby/mute logic. Volume and balance of the amplifiers are controlled using two digital input pins which can be driven by simple push-buttons or by a microcontroller.

Using the selection pin (GAINSEL) the maximum gain can be set at 20 or 30 dB. The headphone sense input (HPS) can be used to detect if a headphone is plugged into the jack connector. If a headphone is plugged into the jack connector the amplifier switches from the BTL to the SE mode and the BTL loudspeakers are switched off. This also results in a reduction of quiescent current consumption.

The TDA8552T is contained in a 20-pin small outline package. For the TDA8552TS, which is contained in a 20-pin very small outline package, the maximum output power is limited by the maximum allowed ambient temperature. More information can be found in Section “Thermal design considerations”. The SO20 package has the four corner leads connected to the die pad so that the thermal behaviour can be improved by the PCB layout.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8552T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
TDA8552TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	5	5.5	V
I_q	quiescent supply current	BTL mode; V_{DD} = 5 V	–	14	20	mA
		BTL mode; V_{DD} = 3.3 V	–	10	15	mA
		SE mode; V_{DD} = 5 V	–	8.5	12	mA
		SE mode; V_{DD} = 3.3 V	–	5	8	mA
I_{stb}	standby current		–	1	10	μA
P_o	output power	THD = 10%; R_L = 8 Ω; V_{DD} = 5 V	1	1.4	–	W
G_v	voltage gain	low gain; maximum volume	–	20	–	dB
		low gain; minimum volume	–	–60	–	dB
		high gain; maximum volume	–	30	–	dB
		high gain; minimum volume	–	–50	–	dB
N_{step}	number of volume steps		–	64	–	
THD	total harmonic distortion	P_o = 0.5 W	–	0.1	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

BLOCK DIAGRAM

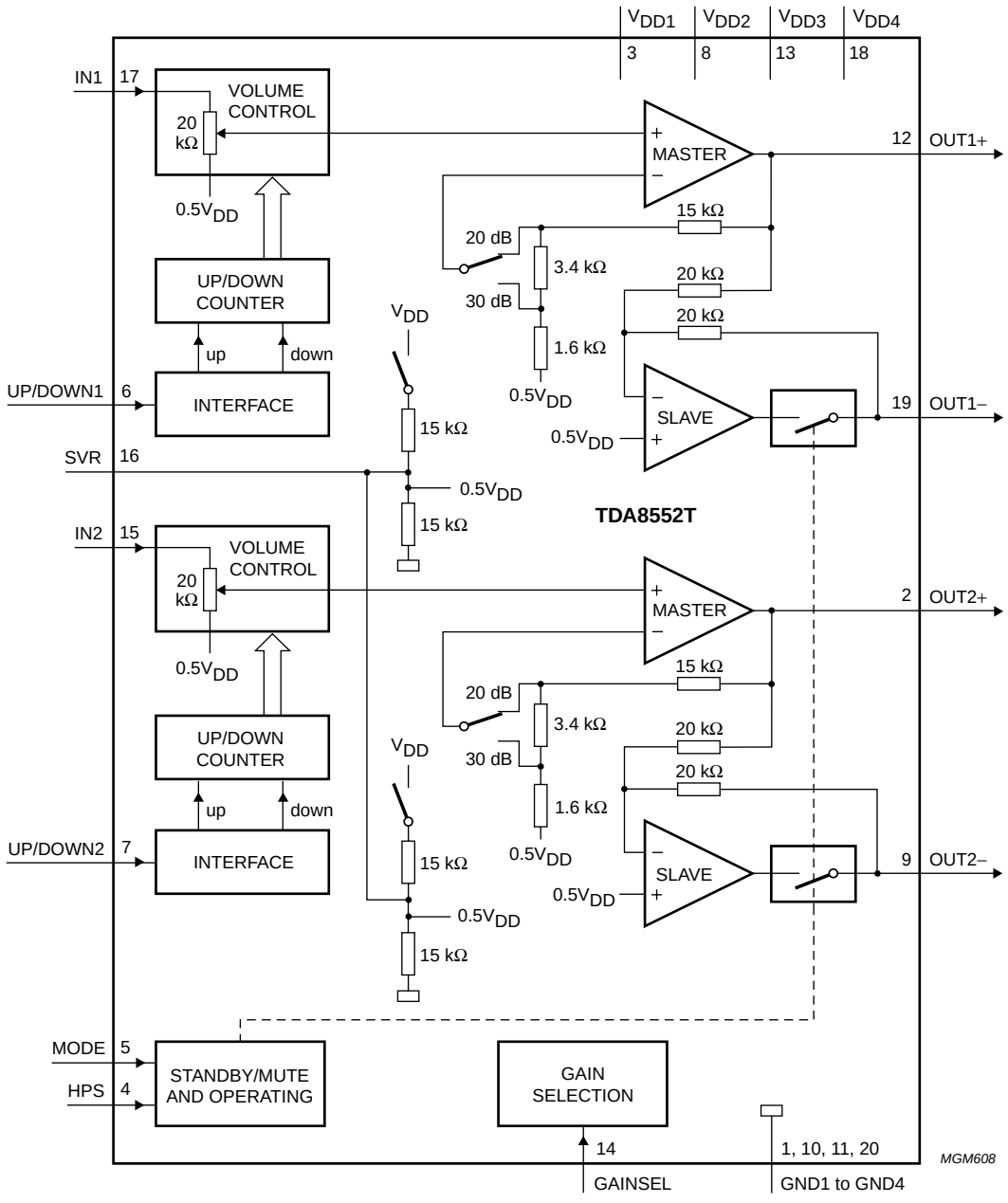


Fig.1 Block diagram.

PINNING

SYMBOL	PIN[1]	DESCRIPTION
GND1	1	ground 1, substrate/leadframe
OUT2+	2	positive loudspeaker terminal output channel 2
V_{DD1}	3	supply voltage 1
HPS	4	digital input for headphone sensing
MODE	5	digital trinary input for mode selection (standby, mute and operating)
UP/DOWN1	6	digital trinary input for volume control channel 1
UP/DOWN2	7	digital trinary input for volume control channel 2
V_{DD2}	8	supply voltage 2
OUT2−	9	negative loudspeaker terminal output channel 2
GND2	10	ground 2, substrate/leadframe
GND3	11	ground 3, substrate/leadframe
OUT1+	12	positive loudspeaker terminal output channel 1
V_{DD3}	13	supply voltage 3
GAINSEL	14	digital input for gain selection
IN2	15	audio input channel 2
SVR	16	half supply voltage, decoupling ripple rejection
IN1	17	audio input channel 1
V_{DD4}	18	supply voltage 4
OUT1−	19	negative loudspeaker terminal output channel 1
GND4	20	ground 4, substrate/leadframe

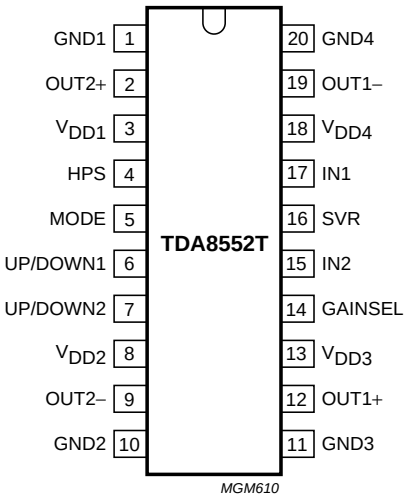


Fig.2 Pin configuration.

Note

1. For the SO20 (SOT163-1) package only: the ground pins 1, 10, 11 and 20 are mechanically connected to the leadframe and electrically to the substrate of the die. On the PCB the ground pins can be connected to a copper area to decrease the thermal resistance.

FUNCTIONAL DESCRIPTION

The TDA8552T is a 2 × 1.4 W BTL audio power amplifier capable of delivering 2 × 1.4 W output power into an 8 Ω load at THD = 10% using a 5 V power supply. The gain of the amplifier can be set by the digital volume control. The gain in the maximum volume setting is 20 dB (low gain) or 30 dB (high gain). This maximum gain can be selected by the gain selection pin. The headphone sense input (HPS) can be used to detect if a headphone is plugged into the jack connector. If a headphone is plugged into the jack connector the amplifier switches from the BTL to the SE mode and the BTL loudspeakers are switched off. This also results in a reduction of quiescent current consumption. Using the MODE pin the device can be switched to the standby condition, the mute condition or the normal operating condition. The device is protected by an internal thermal shutdown protection mechanism.

Power amplifier

The power amplifier is a Bridge-Tied Load (BTL) amplifier with a complementary CMOS output stage. The total voltage loss for both output power MOS transistors is within 1 V and with a 5 V supply and an 8 Ω loudspeaker an output power of 1.4 W can be delivered. The total gain of this power amplifier can be set at 20 or 30 dB by the gain selection pin.

Gain selection

The gain selection can be used for a fixed gain setting, depending on the application. The gain selection pin must be hard wired to ground (20 dB) or to V_{DD} (30 dB). Gain selecting during the operation is not advised, switching is not guaranteed plop free.

Input attenuator

The volume control operates as a digitally controlled input attenuator between the audio input pin and the power amplifier. In the maximum volume control setting the attenuation is 0 dB and in the minimum volume control setting the typical attenuation is 80 dB. The attenuation can be set in 64 steps by the UP/DOWN pin. Both attenuators for channels 1 and 2 are separated from each other and are controlled by there own UP/DOWN pin. Balance control can be arranged by applying UP/DOWN pulses only on pins 6 and 7, see Fig.5.

Volume control

Each attenuator is controlled with its own UP/DOWN pin (trinary input):

- Floating UP/DOWN pin: volume remains unchanged
- Negative pulses: decreasing volume
- Positive pulses: increasing volume.

Each pulse on the UP/DOWN pin results in a change in gain of $\frac{80}{64} = 1.25$ dB (typical value).

In the basic application the UP/DOWN pin is switched to ground or V_{DD} by a double push-button. When the supply voltage is initially connected, after a complete removal of the supply, the initial state of the volume control is an attenuation of 40 dB (low volume), so the gain of the total amplifier is −20 dB in the low gain setting or −10 dB in the high gain setting. After powering-up, some positive pulses have to be applied to the UP/DOWN pin for turning up to listening volume.

Auto repeat

If the UP/DOWN pin is LOW or HIGH for the wait time (t_{wait} in seconds) (one of the keys is pressed) then the device starts making up or down pulses by itself with a frequency given by $\frac{1}{t_{rep}}$ (repeat function).

The wait time and the repeat frequency are set using an internal RC oscillator with an accuracy of ±10%.

Volume settings in standby mode

When the device is switched with the MODE select pin to the mute or the standby condition, the volume control attenuation setting keeps its value, under the assumption that the voltage on the V_{DD} pin does not fall below the minimum supply voltage. After switching the device back to the operation mode, the previous volume setting is maintained. In the standby mode the volume setting is maintained as long as the minimum supply voltage is available. The current consumption is very low, approximately 1 μA (typ.). In battery fed applications the volume setting can be maintained during battery exchange if there is a supply capacitor available.

Mode select pin

The device is in the standby mode (with a very low current consumption) if the voltage at the MODE pin is between V_{DD} and $V_{DD} - 0.5$ V. At a mode select voltage level of less than 0.5 V the amplifier is fully operational. In the range between 1 V and $V_{DD} - 1$ V the amplifier is in the mute condition. The mute condition is useful for using it as a 'fast mute', in this mode the output signal is suppressed, while the volume setting remains at its value. It is advised to keep the device in the mute condition while the input capacitor is being charged. This can be achieved by holding the MODE pin at a level of $0.5V_{DD}$, or by waiting approximately 100 ms before giving the first volume-UP pulses.

Headphone sense pin (HPS)

A headphone can be connected to the amplifier by using a coupling capacitor for each channel. The common ground pin of the headphone is connected to the ground of the amplifier, see Fig.4. By using the HPS pin as illustrated in Fig.4, the TDA8552T detects if a headphone jack plug is inserted into the connector.

When no headphone is plugged in, the voltage level at the HPS pin will remain LOW. A voltage less than $V_{DD} - 1$ V at the HPS pin will keep the device in the BTL mode, thus the loudspeakers can be operational. If the HPS pin is not connected then the device will remain in the BTL mode.

When a headphone is plugged into the connector, the voltage at the HPS pin will be set to V_{DD}. The device then switches to the Single-Ended (SE) mode, this means that the slave power amplifiers at the outputs OUT1− and OUT2− will be switched to the standby mode. This results in floating outputs OUT1− and OUT2−, the loudspeaker signal is thus attenuated by approximately 80 dB and only the headphone can operate.

One of the benefits of this system is that the loudspeaker current does not flow through the jack connector switch, which could give some output power loss. The other benefit is that the quiescent current is reduced when the headphone jack is inserted.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	operating	−0.3	+5.5	V
V_i	input voltage		−0.3	V_{DD} + 0.3	V
I_{ORM}	repetitive peak output current		−	1	A
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	operating ambient temperature		−40	+85	°C
V_{sc}	AC and DC short-circuit safe voltage		−	5.5	V
P_{tot}	maximum power dissipation	SO20	−	2.2	W
		SSOP20	−	1.1	W

THERMAL CHARACTERISTICS

See Section “Thermal design considerations” in Chapter “Test and application information”.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient			
	for the TDA8552T (SO20)	in free air	60	K/W
		extra copper	55	K/W
	for the TDA8552TS (SSOP20)	in free air	110	K/W
		extra copper	80	K/W

Table 1 Power rating; note 1

V_{DD} (V)	R_L (Ω)	$P_{o\ (w)}$ THD = 10%	OPERATION	MUSIC POWER		
				P_{max} (W)	$T_{amb(max)}$ (°C)	
					SO20	SSOP20
3.3	4	0.9	BTL	0.55	120	106
3.3	8	0.6	BTL	0.28	134	127
3.3	16	0.3	BTL	0.14	142	139
3.3	32SE	0.035	headphone	0.03	150	150
5.0	4	2.0	BTL	1.25	81	50
5.0	8	1.4	BTL	0.65	114	98
5.0	16	0.8	BTL	0.32	132	124
5.0	32SE	0.09	headphone	0.07	146	144
				continuous sine wave		
3.3	4	0.9	BTL	1.1	89	62
5	8	1.4	BTL	1.25	81	50

Note

1. The power rating is based on $R_{th(j-a)}$ with recommended copper pattern of at least 4×1 cm^2 to the corner leads and copper under the IC package.

QUALITY SPECIFICATION

Quality specification in accordance with *"SNW-FQ-611 part E"*, if this type is used as an audio amplifier.

DC CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; total gain setting at 7 dB; according to Fig.4.; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.7	5	5.5	V
I_{DD}	supply current	BTL mode; V_{DD} = 5 V; R_L = ∞; note 1	–	14	20	mA
		SE mode; V_{DD} = 5 V	–	8.5	12	mA
		BTL mode; V_{DD} = 3.3 V; R_L = ∞; note 1	–	10	15	mA
		SE mode; V_{DD} = 3.3 V	–	5	8	mA
I_{stb}	standby current	V_{MODE} = V_{DD}	–	1	10	μA
V_O	DC output voltage	note 2	–	2.5	–	V
$\lvert V_{OUT+} - V_{OUT-} \rvert$	differential output offset voltage	GAINSEL = 0 V	–	–	50	mV
		GAINSEL = V_{DD}	–	–	150	mV
Mode select pin						
V_{MODE}	input voltage	standby	V_{DD} − 0.5	–	V_{DD}	V
		mute	1	–	V_{DD} − 1.4	V
		operating	0	–	0.5	V
I_{MODE}	input current	0 < V_{MODE} < V_{DD}	–	–	1	μA
α_{mute}	mute attenuation	note 3	80	tbf	–	dB
Gain select pin						
$V_{GAINSEL}$	input voltage	low gain (20 dB)	0	–	0.6	V
		high gain (30 dB)	4.1	–	V_{DD}	V
$I_{GAINSEL}$	input current		–	–	1	μA
Headphone sense pin						
V_{HPS}	input voltage	SE mode; headphone detected	V_{DD} − 1	–	V_{DD}	V
I_{HPS}	input current		–	–	1	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Volume control						
t_W	pulse width		50	–	–	ns
t_{rep}	pulse repetition time		100	–	–	ns
$V_{th(up)}$	UP/DOWN pin UP threshold level		4.1	–	V_{DD}	V
$V_{float(max)}$	UP/DOWN pin floating high level		–	–	3.4	V
$V_{float(min)}$	UP/DOWN pin floating low level		1.0	–	–	V
$V_{th(down)}$	UP/DOWN pin DOWN threshold level		0	–	0.6	V
$I_{I(up/down)}$	input current UP/DOWN pin	$0 < V_{UP/DOWN} < V_{DD}$	–	–	200	μA
t_{wait}	auto repeat wait time		–	500	–	ms
t_{rep}	repeat time	key pressed	–	130	–	ms
Volume attenuator						
$G_{v(l)}$	low gain; maximum volume (including power amplifier)		19	20	21	dB
	low gain; minimum volume (including power amplifier)		tbf	–60	tbf	dB
$G_{v(h)}$	high gain; maximum volume (including power amplifier)		29	30	31	dB
	high gain; minimum volume (including power amplifier)		tbf	–50	tbf	dB
N_{step}	number of gain steps		–	64	–	
ΔG_v	variation of gain per step		–	1.25	–	dB
Z_i	input impedance		14	20	–	kΩ
$V_{i(max)(rms)}$	maximum input voltage (RMS value)		–	–	1.75	V

Notes

1. With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to $2 \times \left(\frac{\text{DC output offset voltage}}{R_L}\right)$
2. The DC output voltage with respect to ground is approximately $0.5V_{DD}$.
3. Output voltage in mute position is measured with an input of 1 V (RMS) in a bandwidth of 20 kHz, so including noise, gain select pin is LOW (0 V).

AC CHARACTERISTICS (V_{DD} = 3.3 V)

T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; total gain setting at 7 dB; V_{MODE} = 0 V; gain select pin is at 0 V (maximum gain = 20 dB); according to Fig.4.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%; R_L = 4 Ω	–	0.9	–	W
		THD = 10%; R_L = 8 Ω	–	0.6	–	W
		THD = 10%; R_L = 16 Ω	–	0.3	–	W
		THD = 0.5%; R_L = 4 Ω	–	0.6	–	W
		THD = 0.5%; R_L = 8 Ω	–	0.4	–	W
		THD = 0.5%; R_L = 16 Ω	–	0.2	–	W
THD	total harmonic distortion	P_o = 0.1 W; note 1	–	0.1	–	%
$V_{o(n)}$	noise output voltage	note 2	–	60	–	μV
SVRR	supply voltage ripple rejection	note 3	tbf	55	–	dB
$V_{i(max)}$	maximum input voltage	THD = 1%; G_v = –50 to 0 dB	–	–	1.1	V
α_{sup}	channel suppression	V_{HPS} = V_{DD}; note 4	–	80	–	dB
α_{cs}	channel separation		–	55	–	dB

Notes

1. Volume setting at maximum.
2. The noise output voltage is measured at the output in a frequency band from 20 Hz to 20 kHz (unweighted), R_{source} = 0 Ω, gain select pin is LOW (0 V).
3. Supply voltage ripple rejection is measured at the output, with a source impedance of R_{source} = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS) is applied to the positive supply rail, gain select pin is LOW (0 V).
4. Channel suppression is measured at the output with a source impedance of R_{source} = 0 Ω at the input and a frequency of 1 kHz. The output level in the operating single-ended channel (OUT+) is set at 2 V (RMS).

AC CHARACTERISTICS (V_{DD} = 5 V)

T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; total gain setting at 7 dB; V_{MODE} = 0 V; Gain select pin is at 0 V (maximum gain = 20 dB); according to Fig.4; package is SO20.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%; R_L = 8 Ω	1.0	1.4	–	W
		THD = 10%; R_L = 16 Ω	–	0.8	–	W
		THD = 0.5%; R_L = 8 Ω	0.6	1.0	–	W
		THD = 0.5%; R_L = 16 Ω	–	0.6	–	W
THD	total harmonic distortion	P_o = 0.1 W; note 1	–	0.15	0.4	%
		P_o = 0.5 W; note 1	–	0.1	0.3	%
$V_{o(n)}$	noise output voltage	GAINSEL. = 0 V; note 2	–	60	100	μV
		GAINSEL. = V_{DD}; note 2	–	100	–	μV
SVRR	supply voltage ripple rejection	note 3	50	55	–	dB
$V_{i(max)}$	a maximum input voltage	THD = 1%; G_v = –50 to 0 dB	–	–	1.75	V
α_{sup}	channel suppression	V_{HPS} = V_{DD}; note 4	70	80	–	dB
α_{cs}	channel separation		50	–	–	dB

Notes

1. Volume setting at maximum.
2. The noise output voltage is measured at the output in a frequency band from 20 Hz to 20 kHz (unweighted), R_{source} = 0 Ω.
3. Supply voltage ripple rejection is measured at the output, with a source impedance of R_{source} = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS) is applied to the positive supply rail, gain select pin is LOW (0 V).
4. Channel suppression is measured at the output with a source impedance of R_{source} = 0 Ω at the input and a frequency of 1 kHz. The output level in the operating single-ended channel (OUT+) is set at 1 V (RMS).

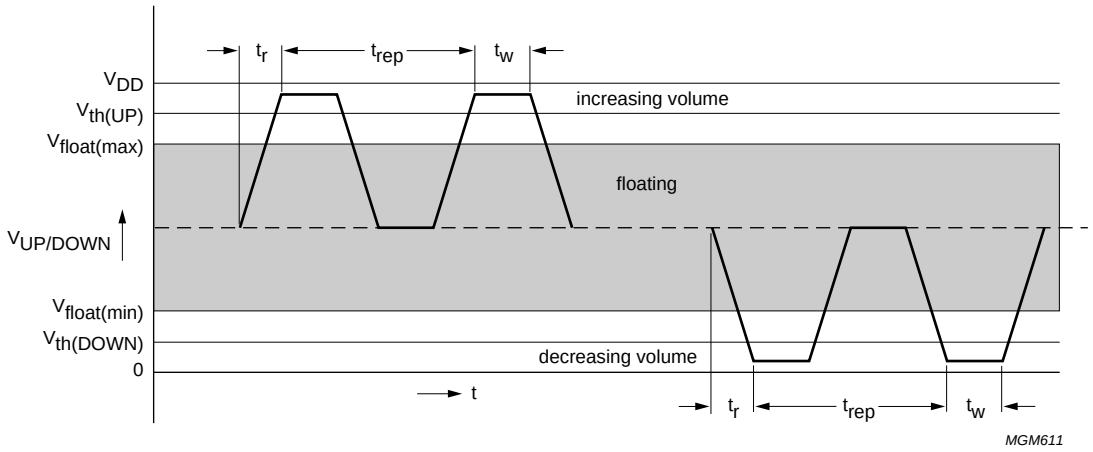
AC CHARACTERISTICS (FOR HEADPHONE; R_L = 32 Ω; CONNECTED SE)

V_{DD} = 5 V; T_{amb} = 25 °C; f = 1 kHz; total gain setting at 20 dB; V_{MODE} = 0 V; gain select pin is 0 V (maximum gain = 20 dB); according to Fig.4.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%; V_{DD} = 3.3 V	–	35	–	mW
		THD = 10%; V_{DD} = 5.0 V	–	90	–	mW
		THD = 0.5%; V_{DD} = 3.3 V	–	25	–	mW
		THD = 0.5%; V_{DD} = 5.0 V	–	60	–	mW
THD	total harmonic distortion	P_o = 60 mW	–	0.04	–	%
$V_{o(n)}$	noise output voltage	note 1	–	60	100	μV
SVRR	supply voltage ripple rejection	note 2	50	55	–	dB
$V_{i(max)}$	maximum input voltage	THD = 1%; G_v = −50 to 0 dB	–	–	1.75	V
α_{cs}	channel separation		50	–	–	dB

Notes

1. The noise output voltage is measured at the output in a frequency band from 20 Hz to 20 kHz (unweighted), R_{source} = 0 Ω, gain select pin is LOW (0 V).
2. Supply voltage ripple rejection is measured at the output, with a source impedance of R_{source} = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS) is applied to the positive supply rail, gain select pin is LOW (0 V).



The rise time (t_r) of the pulse may have any value.

Fig.3 Timing UP/DOWN pin.

TEST AND APPLICATION INFORMATION

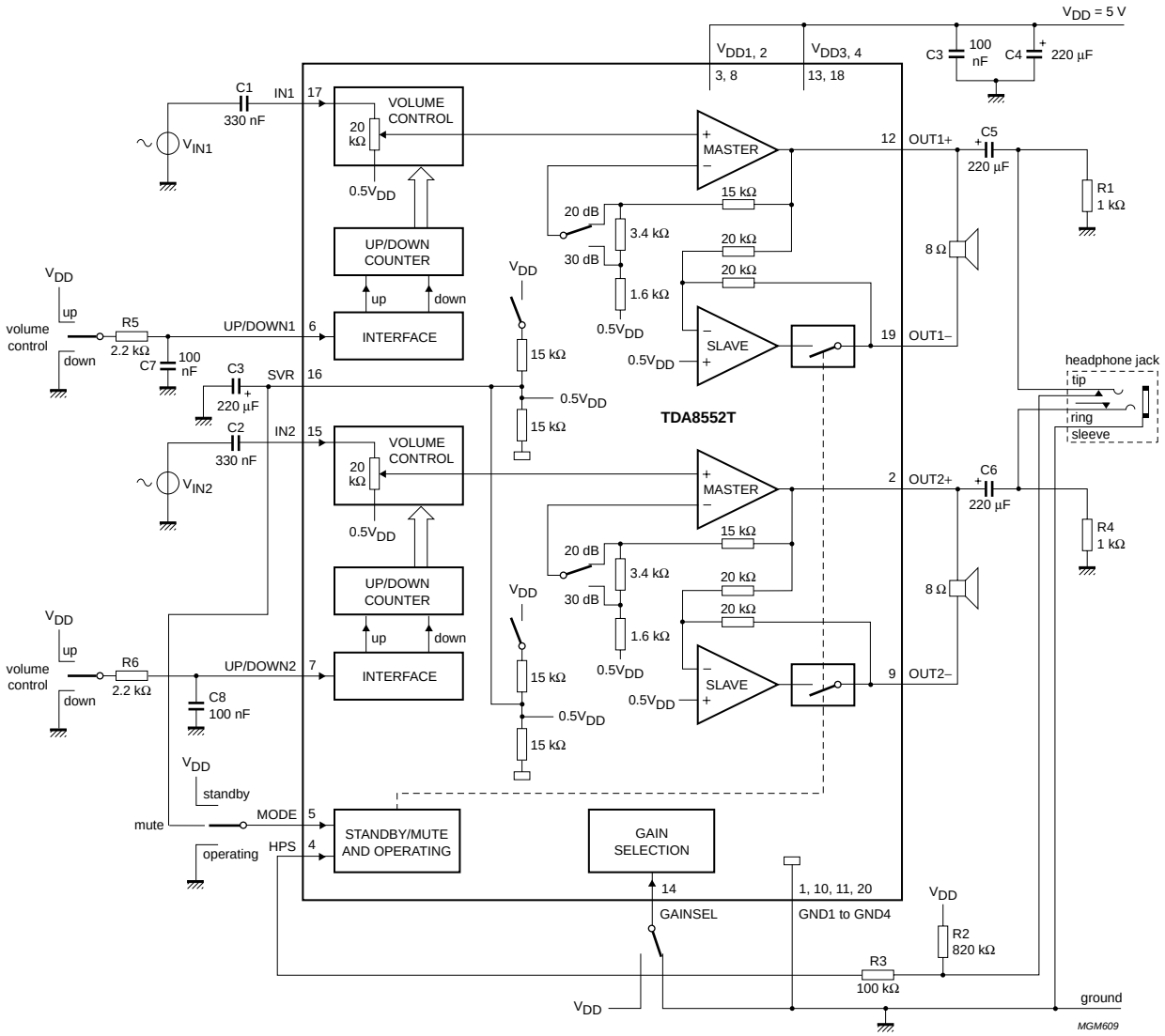


Fig.4 Test and application diagram.

Test conditions

T_{amb} = 25°C if not specially mentioned; V_{DD} = 5 V; f = 1 kHz, R_L = 8 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz. The thermal resistance (in standard print, without extra copper) = 110 K/W for the SSOP20; the maximum sine wave power dissipation is:

$$\frac{150 - 25}{110} = 1.14 \text{ W}$$

For T_{amb} = 60 °C the maximum total power dissipation is:

$$\frac{150 - 60}{110} = 0.82 \text{ W}$$

Thermal design considerations

The 'measured' thermal resistance of the IC package is highly dependent on the configuration and size of the application board. All surface mount packages rely on the traces of the PCB to conduct heat away from the package. To improve the heat flow, a significant area on the PCB must be attached to the (ground) pins. Data may not be comparable between different semiconductor manufacturers because the application boards and test methods are not (yet) standardized. Also, the thermal performance of packages for a specific application may be different than presented here, because the configuration of the application boards (copper area) may be different. NXP Semiconductors uses FR-4 type application boards with 1 oz copper traces with solder coating Solder Resist Mask (SRM).

The SSOP20 package has improved thermal conductivity which reduces the thermal resistance. Using a practical PCB layout (see Fig.18) with wider copper tracks to the corner pins and just under the IC, the thermal resistance from junction to ambient can be reduced to approximately 80 K/W. For T_{amb} = 60 °C the maximum total power dissipation for this PCB layout is: $\frac{150 - 60}{80} = 1.12$ W

The thermal resistance for the SO20 is approximately 55 K/W if applied to a PCB with wider copper tracks to the corner pins and just under the body of the IC.
The maximum total power dissipation for this practical application is:

$$\frac{150 - 60}{55} = 1.63 \text{ W}$$

BTL application

The BTL application diagram is illustrated in Fig.4.

The quiescent current has been measured without any load impedance. The total harmonic distortion as a function of frequency was measured with a low-pass filter of 80 kHz. The value of capacitor C3 influences the behaviour of the SVRR at low frequencies, increasing the value of C3 increases the performance of the SVRR.

Headphone application

T_{amb} = 25°C if not specially mentioned, V_{DD} = 5 V, f = 1 kHz, R_L = 32 Ω, G_v = 14 dB, audio band-pass 22 Hz to 22 kHz.

For headphone application diagram see: Fig.4

If a headphone is plugged into the headphone jack, the HPS pin will switch-off the outputs of the SLAVE output stage, this results in a mute attenuation >80 dB for the loudspeakers. In this condition the quiescent current will be reduced.

General remarks

Reduction of the value of capacitor C3 results in a decrease of the SVRR performance at low frequencies.

The capacitor value of C5 and C6 in combination with the load impedance of the headphone determines the low frequency behaviour.

To prevent against high output currents during inserting the headphone into the headphone jack, resistors of 5.1 Ω have to be connected in series with the SE output lines.

The UP/DOWN pin can be driven by a 3-state logic output stage (microprocessor) without extra external components. If the UP/DOWN pin is driven by push-buttons, then it is advised to have an RC-filter between the buttons and the UP/DOWN pin. Advised values for the RC-filter are 2.2 kΩ and 100 nF. Resistor R4 is not necessary for basic operation, but is advised to keep C6 charged to a voltage of $0.5V_{DD}$ This has the advantage that the plop noise when inserting the headphone plug is minimal. If the headphone sense function (HPS) is not used then the HPS-pin 4 should be hard-wired to ground. This pin should never be left unconnected.

Using double push buttons, the volume step for both channels can be controlled. When for the balance control only a single contact is used, the balance steps are 1.25 dB. If double contacts are used for the balance buttons and the dashed connection is made, then the balance steps are 2.5 dB.

Application without volume control

If pins 6, 7 and 8 are hardwired together the device operates with the volume control setting at maximum.

When the supply voltage is connected and the device is switched from standby to mute or operating for the first time then the gain is ramped up from −20 dB to +20 dB. This takes approximately 5 s.

This maximum gain setting is maintained until the supply voltage drops below the minimum value.

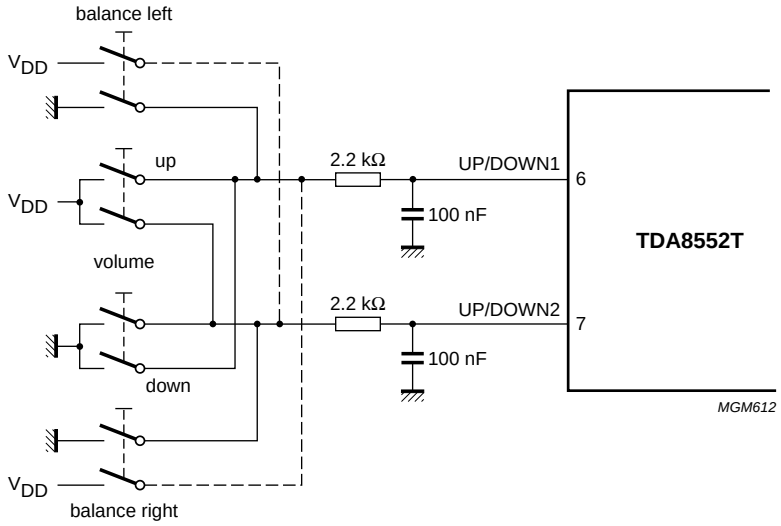
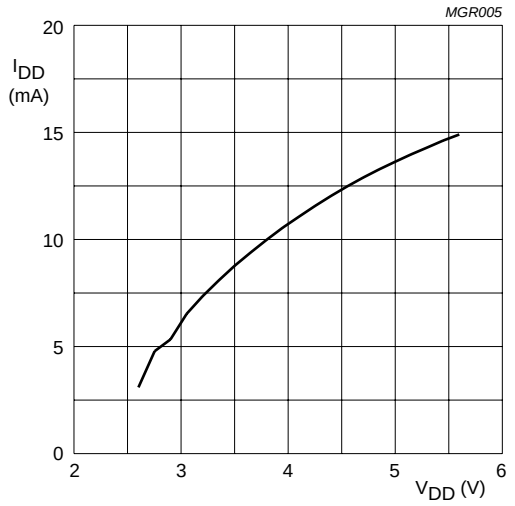
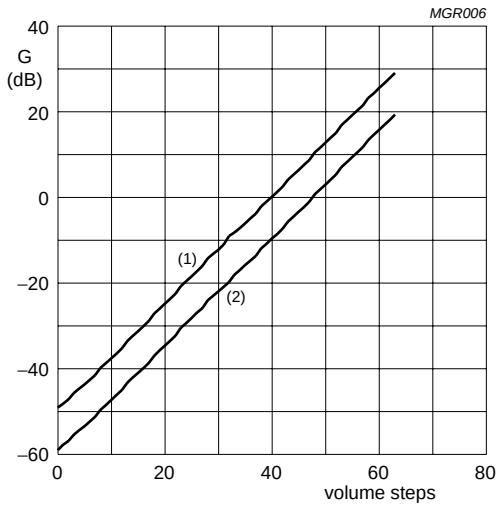


Fig.5 Volume and balance control using buttons.



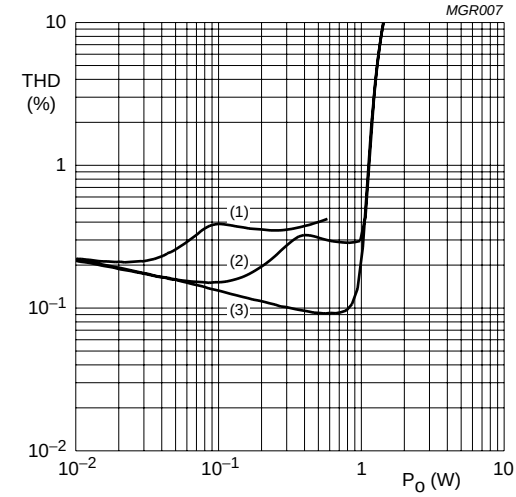
$R_L = \infty$.

Fig.6 I_{DD} as a function of V_{DD}.



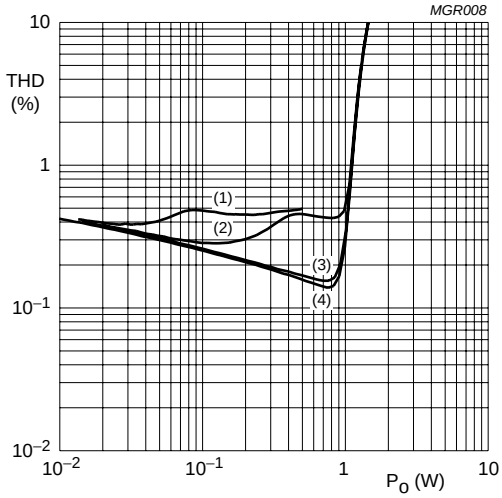
V_{DD} = 5 V; R_L = 8 Ω.
(1) G_v = 30 dB (max.).
(2) G_v = 20 dB (max.).

Fig.7 Gain as a function of volume steps.



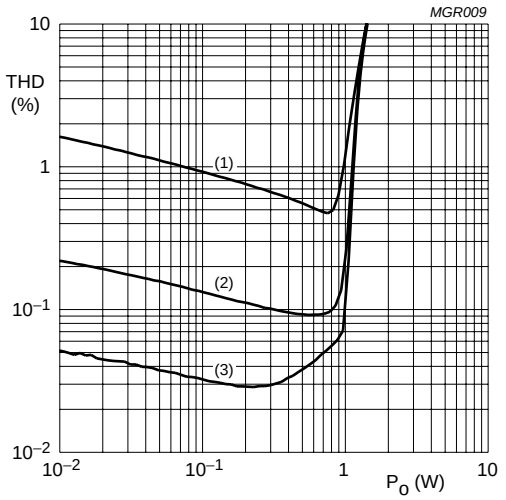
V_{DD} = 5 V; R_L = 8 Ω; f = 1 kHz; G_v = 20 dB (max.).
(1) G_v = 0 dB.
(2) G_v = 7 dB.
(3) G_v = 20 dB.

Fig.8 THD as a function of P_o.



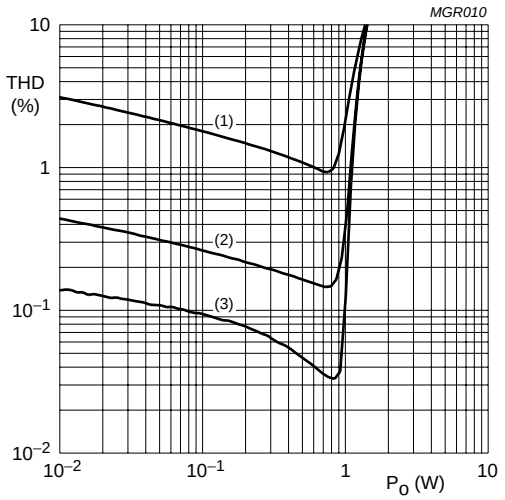
V_{DD} = 5 V; R_L = 8 Ω; f = 1 kHz; G_v = 30 dB (max.).
(1) G_v = 0 dB.
(2) G_v = 7 dB.
(3) G_v = 20 dB.
(4) G_v = 30 dB.

Fig.9 THD as a function of P_o.



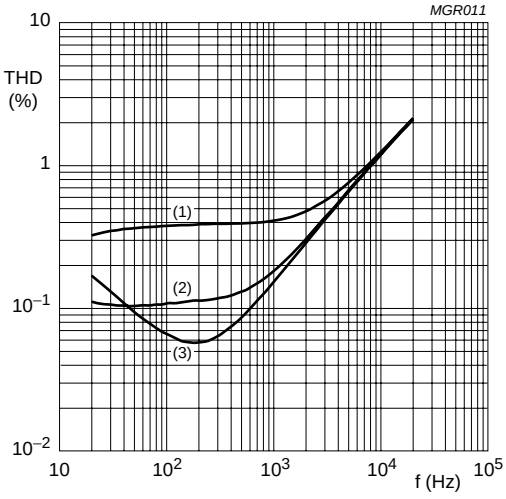
V_{DD} = 5 V; R_L = 8 Ω; G_v = 20 dB (max.).
(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.10 THD as a function of P_o.



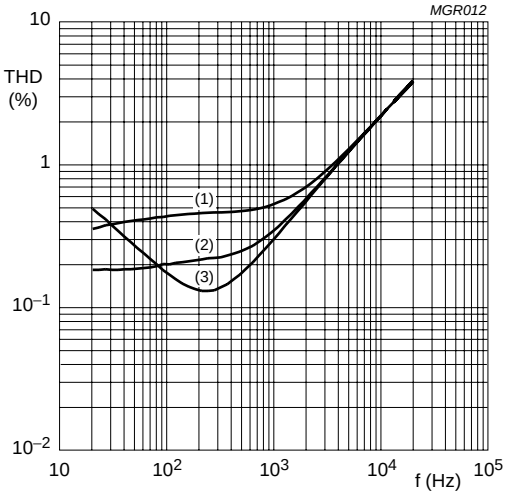
V_{DD} = 5 V; R_L = 8 Ω; G_v = 30 dB (max.).
(1) f = 10 kHz.
(2) f = 1 kHz.
(3) f = 100 Hz.

Fig.11 THD as a function of P_o.



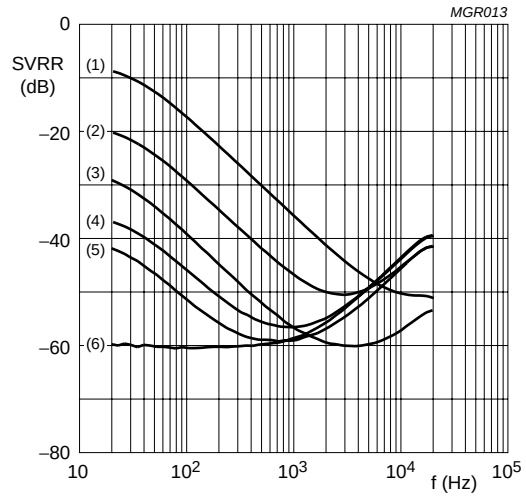
V_{DD} = 5 V; R_L = 8 Ω; P_o = 0.1 W; G_v = 20 dB (max.).
(1) G_v = 0 dB.
(2) G_v = 7 dB.
(3) G_v = 20 dB.

Fig.12 THD as a function of frequency.



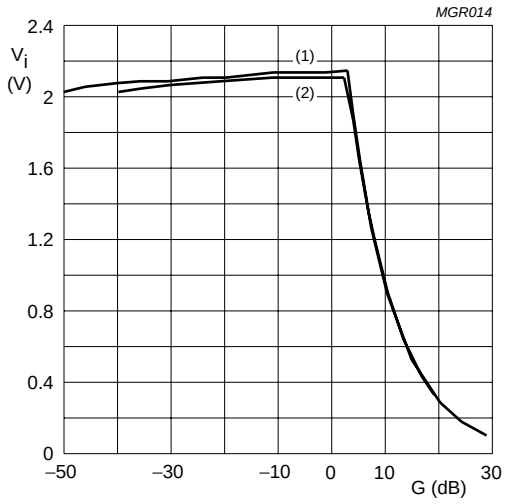
V_{DD} = 5 V; R_L = 8 Ω; P_o = 0.1 W; G_v = 30 dB (max.).
(1) G_v = 0 dB.
(2) G_v = 7 dB.
(3) G_v = 30 dB.

Fig.13 THD as a function of frequency.



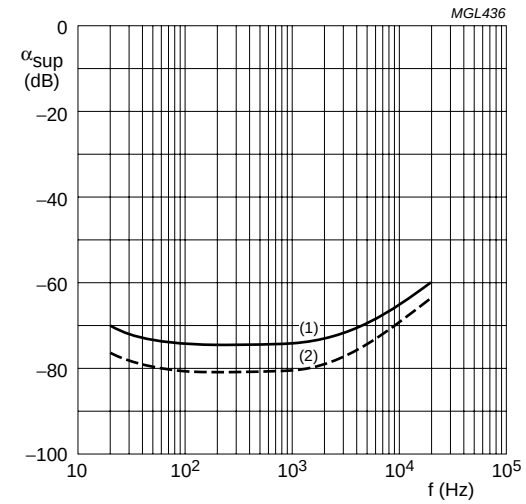
V_{DD} = 5 V; R_L = 8 Ω; V_{ref} = 100 mV.
(1) C3 = 10 μF; G_v = 20 dB.
(2) C3 = 10 μF; G_v = 7 dB.
(3) C3 = 100 μF; G_v = 20 dB.
(4) C3 = 10 μF; G_v = 10 dB.
(5) C3 = 100 μF; G_v = 7 dB.
(6) C3 = 100 μF; G_v = 10 dB.

Fig.14 SVRR as a function of frequency.



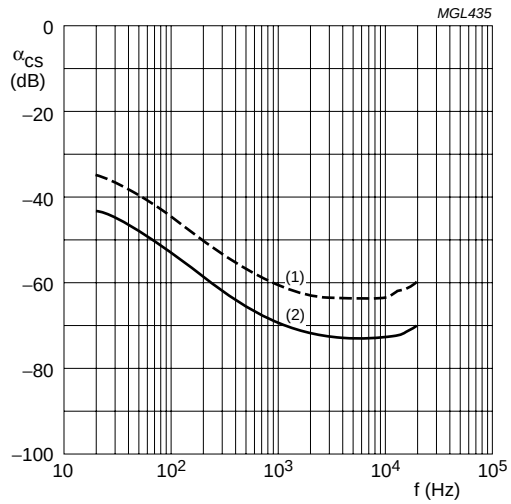
V_{DD} = 5 V; R_L = 8 Ω; f = 1 kHz; THD = 1%.
(1) G_v = 20 dB (max.).
(2) G_v = 30 dB (max.).

Fig.15 Input voltage as a function of gain.



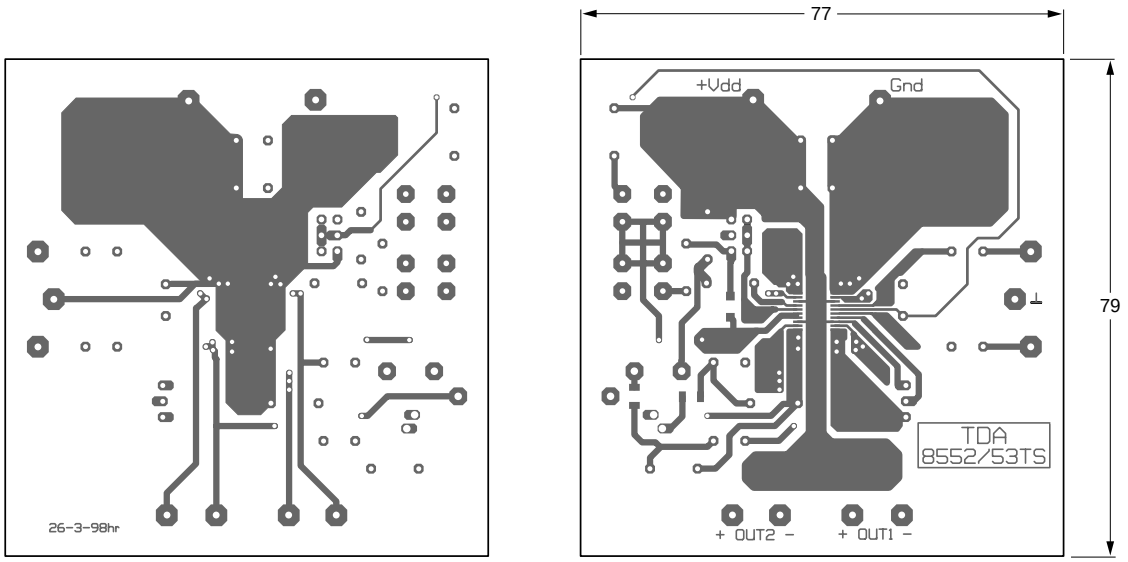
V_P = 5 V; V_o = 1 V; V_{HPS} = V_P.
(1) Channel 1.
(2) Channel 2.

Fig.16 Channel suppression as a function of frequency.



V_P = 5 V; V_o = 1 V.
(1) G_v = 30 dB.
(2) G_v = 20 dB.

Fig.17 Channel separation as a function of frequency.



top view bottom view

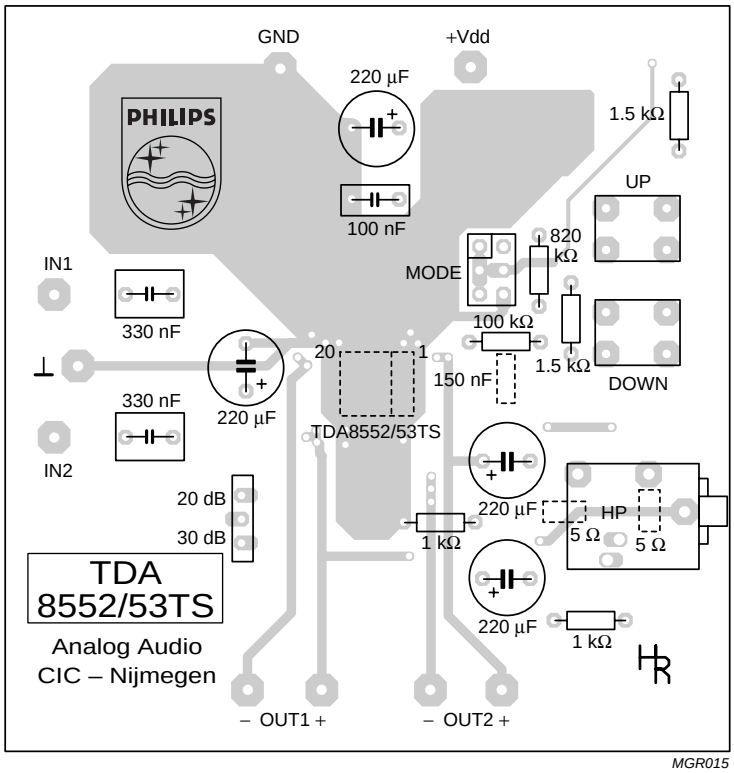
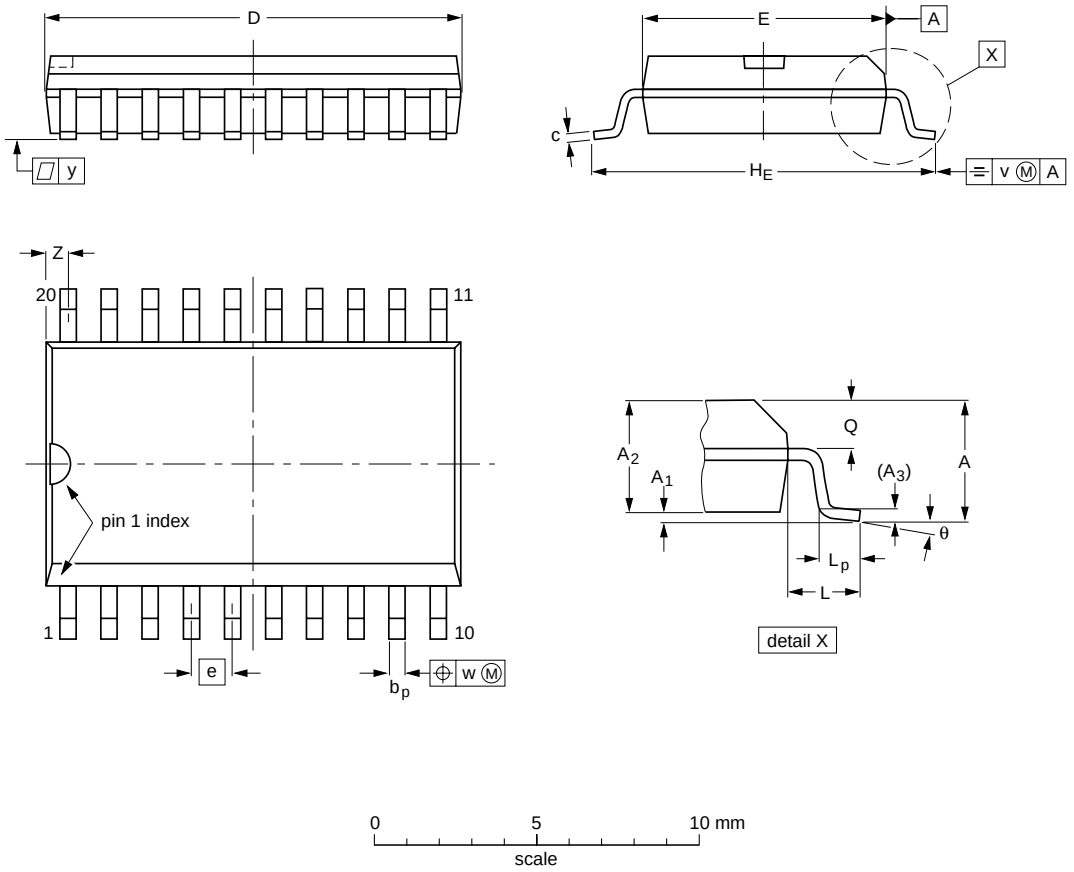


Fig.18 Printed-circuit board layout.

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

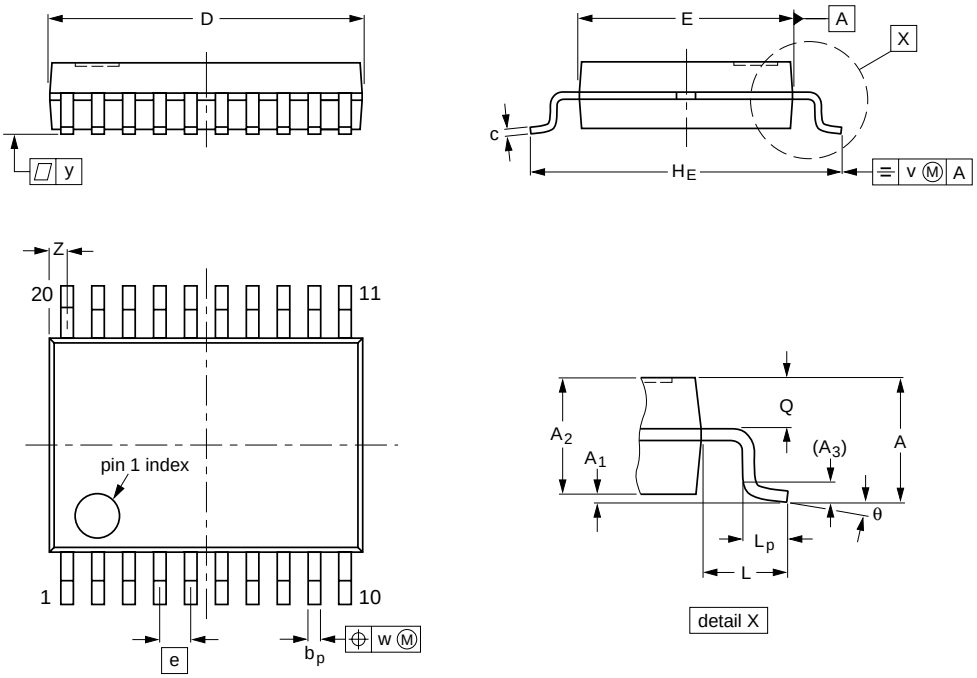
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

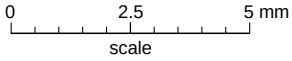
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT266-1		MO-152				~~99-12-27~~ 03-02-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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