

DATA SHEET



TDA8444; TDA8444T; TDA8444AT Octuple 6-bit DACs with I²C-bus

Product specification
Supersedes data of March 1991
File under Integrated Circuits, IC01

1999 Apr 29

Octuple 6-bit DACs with I²C-bus

**TDA8444; TDA8444T;
TDA8444AT**

FEATURES

- Eight DACs with 6-bit resolution
- Adjustable common output swing
- Push-pull outputs
- Outputs short-circuit protected
- Three programmable slave address bits
- Large supply voltage range
- Low temperature coefficient.



GENERAL DESCRIPTION

The interface circuit is a bipolar IC in a DIP16, SO16, or SO20 package made in an I²L-compatible 18 V process.

The TDA8444 contains eight programmable 6-bit DAC outputs, an I²C-bus slave receiver with three (two for SO16) programmable address bits and one input (V_{MAX}) to set the maximum output voltage. Each DAC can be programmed separately by a 6-bit word to 64 values, but V_{MAX} determines the maximum output voltage for all DACs. The resolution will be approximately $\frac{1}{64}V_{MAX}$.

At power-on all DACs are set to their lowest value.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		4.5	12	13.2	V
I_{CC}	supply current	$V_{CC} = 12\text{ V}$	–	14	–	mA
P	power dissipation		–	170	–	mW
V_{VMAX}	input effective voltage		1	–	$V_{CC} - 2.0$	V
$V_{O(DACn)}$	DAC output voltage	$V_{MAX} = V_{CC}$	0.1	–	$V_{CC} - 0.5$	V
$V_{O(DACn)(max)}$	maximum DAC output voltage	$1 < V_{MAX} < V_{CC} - 2.0$	–	$V_{MAX} + 0.3$	–	V
$I_{source(min)}$	minimum DAC source current	data = 1FH	2	–	–	mA
$I_{sink(min)}$	minimum DAC sink current	data = 1FH	2	–	–	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8444	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
TDA8444T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
TDA8444AT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

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BLOCK DIAGRAM

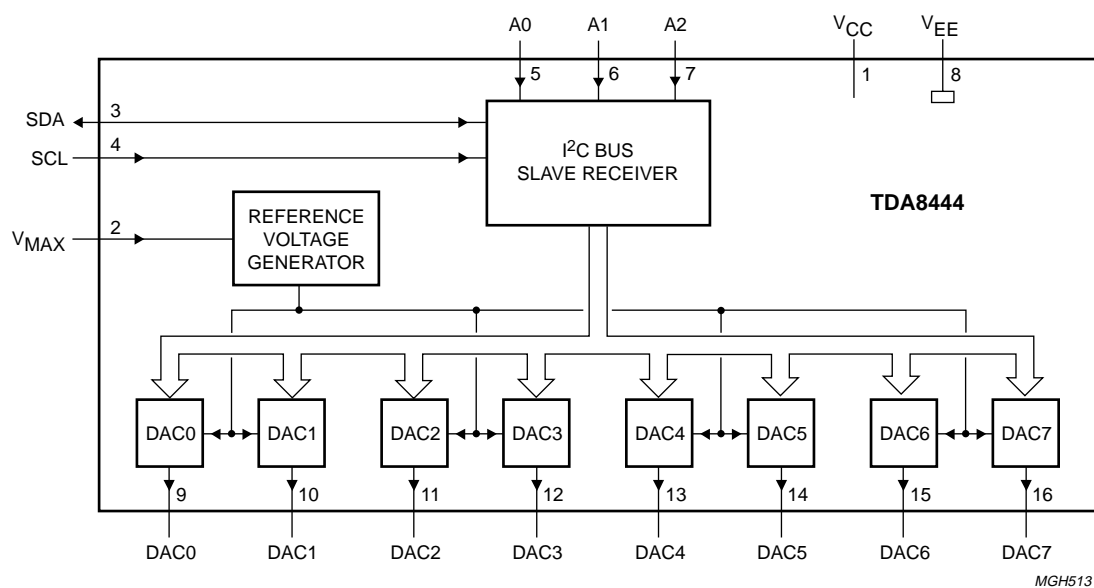


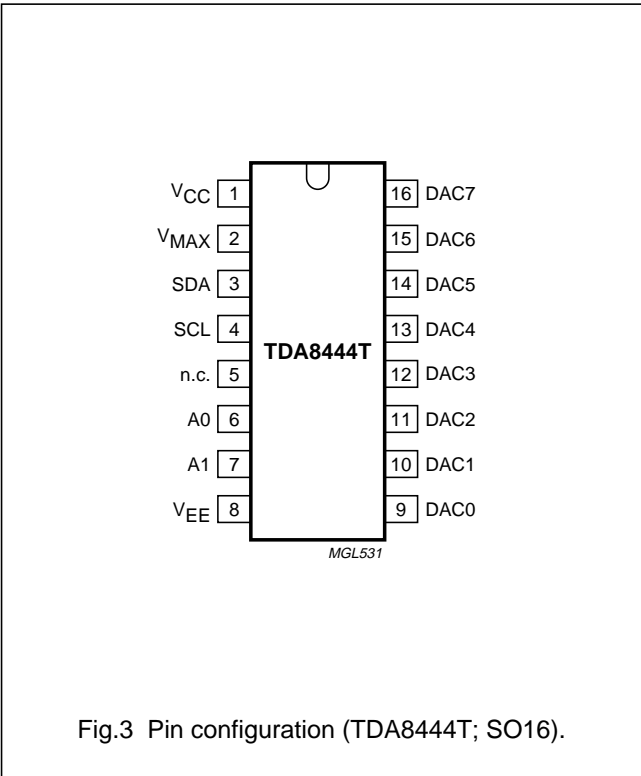
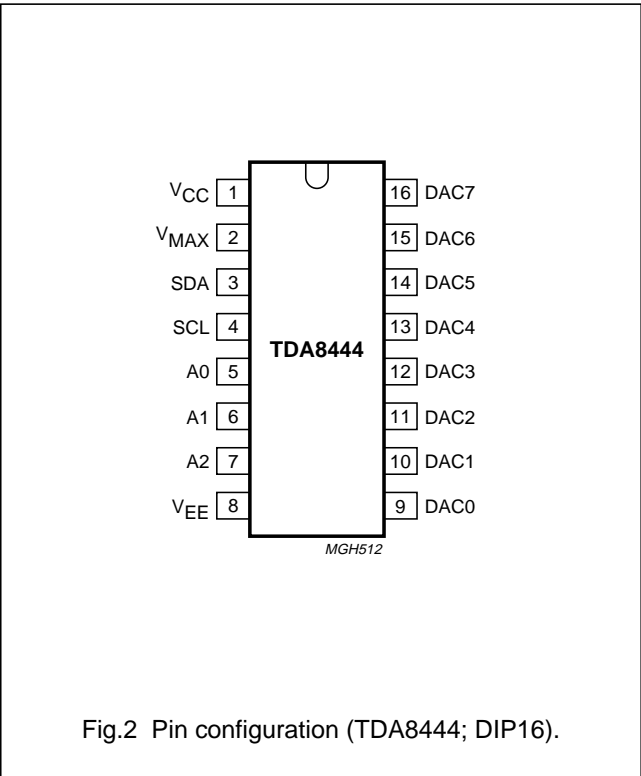
Fig.1 Block diagram.

Octuple 6-bit DACs with I²C-bus

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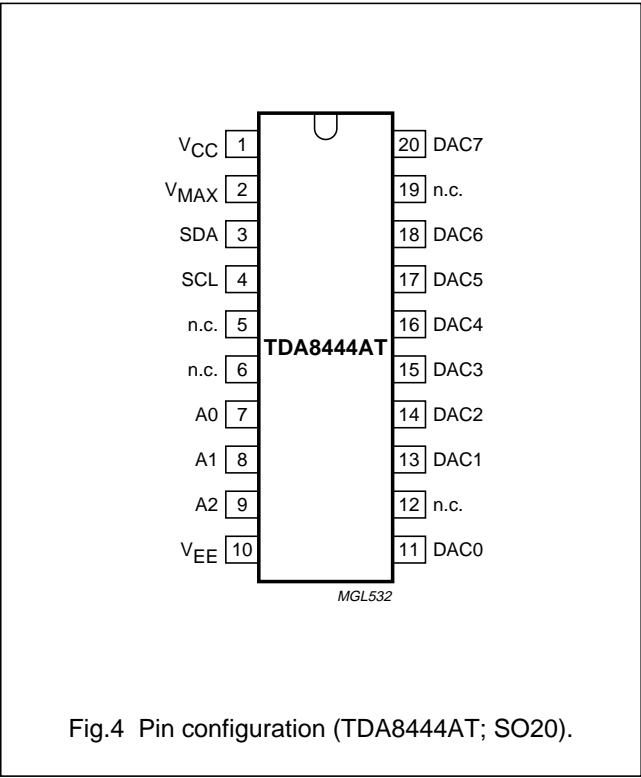
PINNING

SYMBOL	PIN			DESCRIPTION
	TDA8444 (DIP16)	TDA8444T (SO16)	TDA8444AT (SO20)	
V _{CC}	1	1	1	supply voltage
V _{MAX}	2	2	2	control input for DAC maximum output voltage
SDA	3	3	3	I ² C-bus serial data input/output
SCL	4	4	4	I ² C-bus serial clock
A0	5	6	7	programmable address bit 0 for I ² C-bus slave receiver
A1	6	7	8	programmable address bit 1 for I ² C-bus slave receiver
A2	7	–	9	programmable address bit 2 for I ² C-bus slave receiver
V _{EE}	8	8	10	ground
DAC0	9	9	11	analog voltage output 0
DAC1	10	10	13	analog voltage output 1
DAC2	11	11	14	analog voltage output 2
DAC3	12	12	15	analog voltage output 3
DAC4	13	13	16	analog voltage output 4
DAC5	14	14	17	analog voltage output 5
DAC6	15	15	18	analog voltage output 6
DAC7	16	16	20	analog voltage output 7
n.c.	–	5	5, 6, 12, 19	not connected



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FUNCTIONAL DESCRIPTION

I²C-bus interface

The I²C-bus interface is a receive-only slave, which accepts data according the format shown in Table 1.

Table 1 I²C-bus format (see note 1)

S	0 1 0 0 A2 A1 A0 0	A	I3 I2 I1 I0 SD SC SB SA	A	X X D5 D4 D3 D2 D1 D0	A	P
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Note

1. S = START condition; A2 to A0 = programmable address bits; A = Acknowledge; I3 to I0 = Instruction bits; SD to SA = subaddress bits; X = don't care; D5 to D0 = data bits; P = STOP condition.

Valid addresses are:

- TDA8444 and TDA8444AT: 40H, 42H, 44H, 46H, 48H, 4AH, 4CH and 4EH
TDA8444T: 48H, 4AH, 4CH and 4EH (A2 is always logic 1).

All other addresses cannot be acknowledged by the circuit. The actual slave address depends on the programmable address bits A2, A1 and A0. This way up to eight circuits can be used on one I²C-bus.

Valid instructions are: 00H to 0FH; F0H to FFH.

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The circuit will not react to other combinations of the 4 instruction bits I3 to I0 than 0 or F, but will still generate an acknowledge. The difference between instruction 0 and F is only important when more than one data byte is sent within one transmission. Instruction 0 causes the data bytes to be written into the DAC-latches with consecutive subaddresses starting with the subaddress given in the instruction byte (auto-increment of subaddress), while instruction F will cause a consecutive writing of the data bytes into the same DAC-latch whose subaddress was given in the instruction byte. In case of only one data byte the DAC-latch with the subaddress equal to the subaddress in the instruction byte will receive the data.

Valid subaddresses are: 0H to 7H.

The subaddresses correspond to DAC0 to DAC7. The Auto-Increment (AI) function of instruction 0, however, works on all possible subaddresses 0 to F in such a way that next to subaddress F, subaddress 0 will follow, and so on.

The data will be latched into the DAC-latch on the positive-going edge of the acknowledge related clock pulse.

The specification of the SCL and SDA I/O meets the I²C-bus specification. For protection against positive voltage pulses on pins 3 and 4, zener diodes are

connected between these pins and V_{EE}. This means that normal bus line voltage should not exceed 5.5 V.

The address inputs A0, A1 and A2 can be easily programmed by either a connection to V_{EE} (A_n = 0) or V_{CC} (A_n = 1). If the inputs are left floating the result will be A_n = 1.

V_{MAX}

The V_{MAX} input gives a means of compressing the DAC output voltage swing. The maximum DAC output voltage will be equal to V_{MAX} + V_{DAC(min)}, while the 6-bit resolution is maintained. This enables a higher voltage resolution for smaller output swings.

DACs

The DACs consist of a 6-bit data-latch, current switches and an opamp. The current sources connected to the switches have values with weights 2⁰ to 2⁵. The sum of the switched on currents is converted by the opamp into a voltage between approximately 0.5 and 10.5 V if V_{MAX} = V_{CC} = 12 V. The DAC outputs are short-circuit protected against V_{CC} and V_{EE}. Capacitive load on the DAC outputs should not exceed 2 nF in order to prevent possible oscillations at certain levels. The temperature coefficient for each of the outputs remains in all possible conditions well below 0.1 LSB per Kelvin.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{CC}	supply voltage	−0.5	+18	V
I _{CC}	supply current	−10	+40	mA
P _(max)	maximum power dissipation	—	500	mW
V _{i(n)}	input voltage	−0.5	+5.9	V
	pins SDA and SCL	−0.5	+5.9	V
	pins V _{MAX} , A0 to A2 and DAC0 to DAC7	−0.5	V _{CC} + 0.5	V
I _n	current in all pins except V _{CC} and V _{EE}	—	±10	mA
T _{stg}	storage temperature	−65	+150	°C
T _{amb}	operating ambient temperature	−20	+70	°C

QUALITY SPECIFICATION

In accordance with “SNW-FQ-611-E”.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-a)}	thermal resistance from junction to ambient	in free air		
	TDA8444		75	K/W
	TDA8444T	note 1	100	K/W
	TDA8444AT	note 1	85	K/W

Note

1. When mounted on a Printed-Circuit Board (PCB).

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V _{CC}	supply voltage		4.5	12	13.2	V
I _{CC}	supply current	V _{MAX} = V _{CC} = 12 V; data = 00H	12	14	19	mA
P	power dissipation		–	170	250	mW
V _{rst}	power reset voltage		1	–	4	V
Pin V _{MAX}						
V _{i(VMAX)}	input effective voltage		1	–	V _{CC} – 2.0	V
I _i	input current	V _{MAX} = V _{CC}	–	–	10	μA
		V _{MAX} = 1 V	–	–	10	μA
Pins SDA and SCL						
V _I	input voltage		0	–	5.5	V
V _{IL}	LOW-level input voltage		–	–	1.0	V
V _{IH}	HIGH-level input voltage		3.0	–	–	V
I _{IL}	LOW-level input current	V _{SDA} = V _{SCL} = –0.3 V	–	–	–10	μA
I _{IH}	HIGH-level input current	V _{SDA} = V _{SCL} = 6 V	–	–	±10	μA
PIN SDA						
V _{OL}	LOW-level output voltage	I _L = 3 mA	–	–	0.4	V
I _{o(sink)}	output sink current		3	8	–	mA
Address bits (A0 to A2)						
V _I	input voltage		0	–	V _{CC}	V
V _{IL}	LOW-level input voltage		–	–	1.0	V
V _{IH}	HIGH-level input voltage		2.2	–	–	V
I _{IL}	LOW-level input current	V _{An} = V _{EE}	–10	–15	–	μA
I _{IH}	HIGH-level input current	V _{An} = V _{CC}	–	–	1	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DACs (DAC0 to DAC7)						
V _o	DAC output voltage	V _{MAX} = V _{CC}	0.1	–	V _{CC} – 0.5	V
V _{o(min)}	minimum output voltage	data = 00H; I _L = –2 mA	0.1	0.28	0.5	V
V _{o(max)}	maximum output voltage	data = 3FH; I _L = –2 mA V _{MAX} = V _{CC} 1 < V _{MAX} < 10 V	10.0 –	10.5 note 1	11.5 –	V V
I _{o(sink)}	output sink current	V _{DAC} = V _{CC} ; data = 1FH	2	8	15	mA
I _{o(source)}	output source current	V _{DAC} = V _{EE} ; data = 1FH	–2	–	–6	mA
Z _o	output impedance	–2 ≤ I _L ≤ +2 mA; data = 1FH	–	4	50	Ω
DNL	differential non-linearity	V _{MAX} = V _{CC} ; I _L = –2 mA	–	–	±0.5	LSB
INL	integral non-linearity	V _{MAX} = V _{CC} ; I _L = –2 mA	–	–	±0.5	LSB
ΔG _{FS}	DC gain match at full-scale	data = 3FH; I _L = –2 mA	–	–	5	%
ΔG/Δdata	DC gain versus other DAC data change	data = 3FH; I _L = –2 mA	–	<±0.5	–	LSB
TC	temperature coefficient	data = 3FH; I _L = –2 mA	–	<±0.1	–	LSB/K

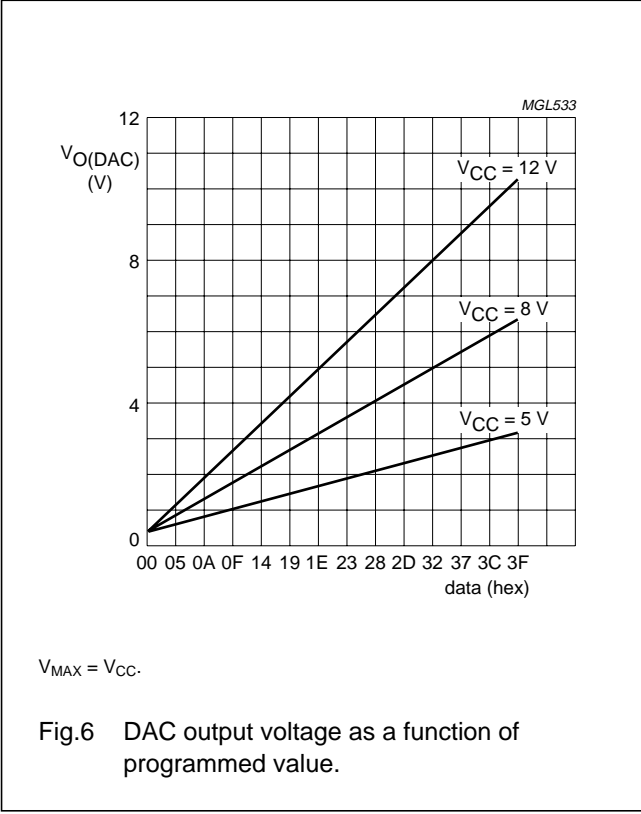
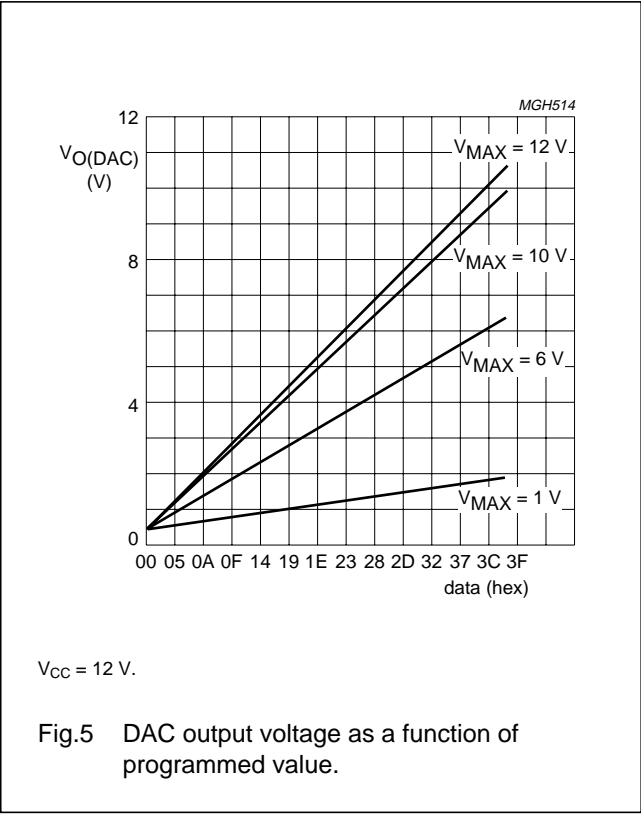
Note

1. The output voltage is typically: $\frac{V_{\text{swing}}}{(V_{\text{CC}} - 2.0)} \times V_{\text{MAX}} + V_{o(00H)}$ with $V_{\text{swing}} = V_{o(3FH)} - V_{o(00H)}$ for $V_{\text{MAX}} = V_{\text{CC}}$.

Octuple 6-bit DACs with I²C-bus

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TEST AND APPLICATION INFORMATION



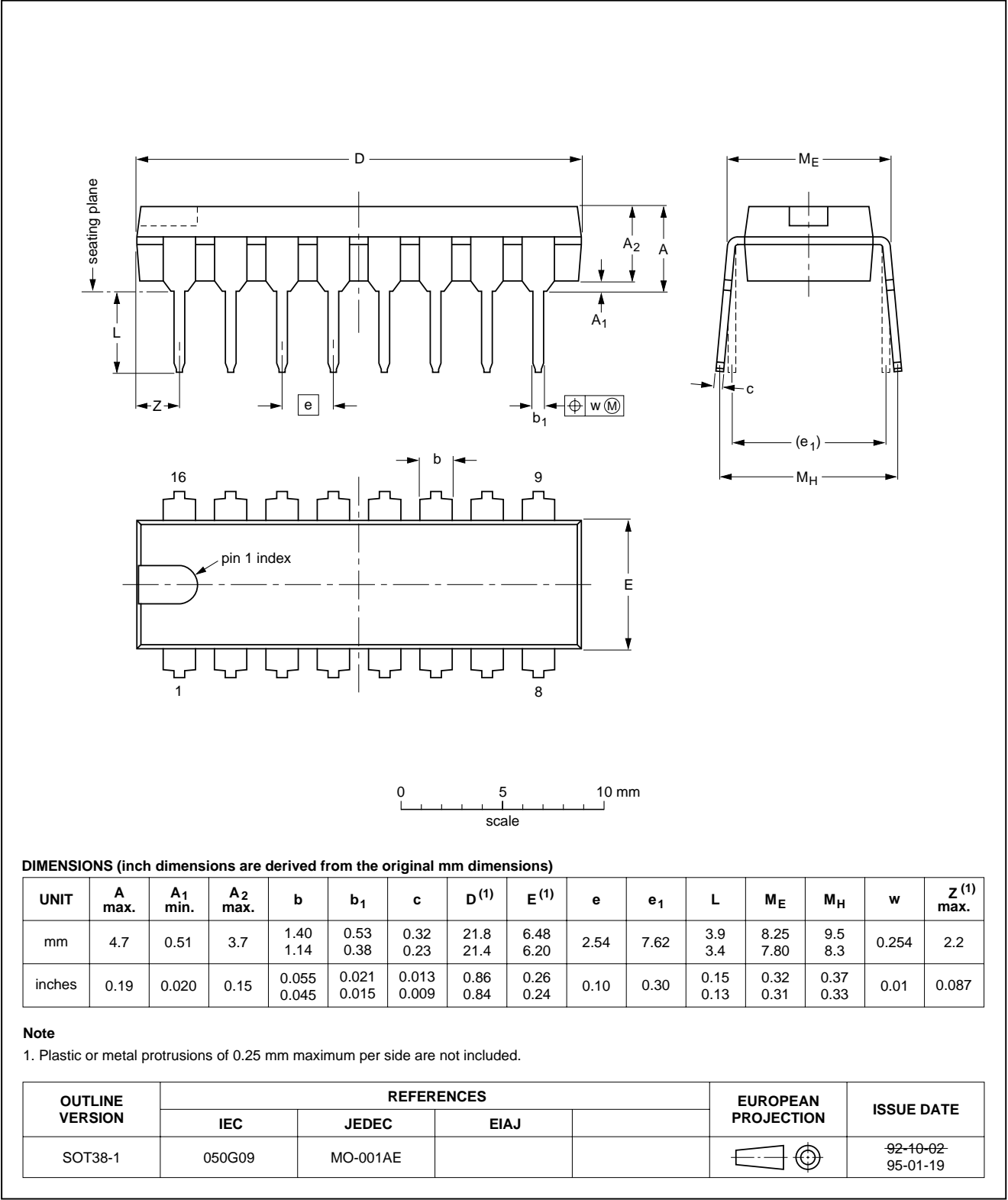
Octuple 6-bit DACs with I²C-bus

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PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1

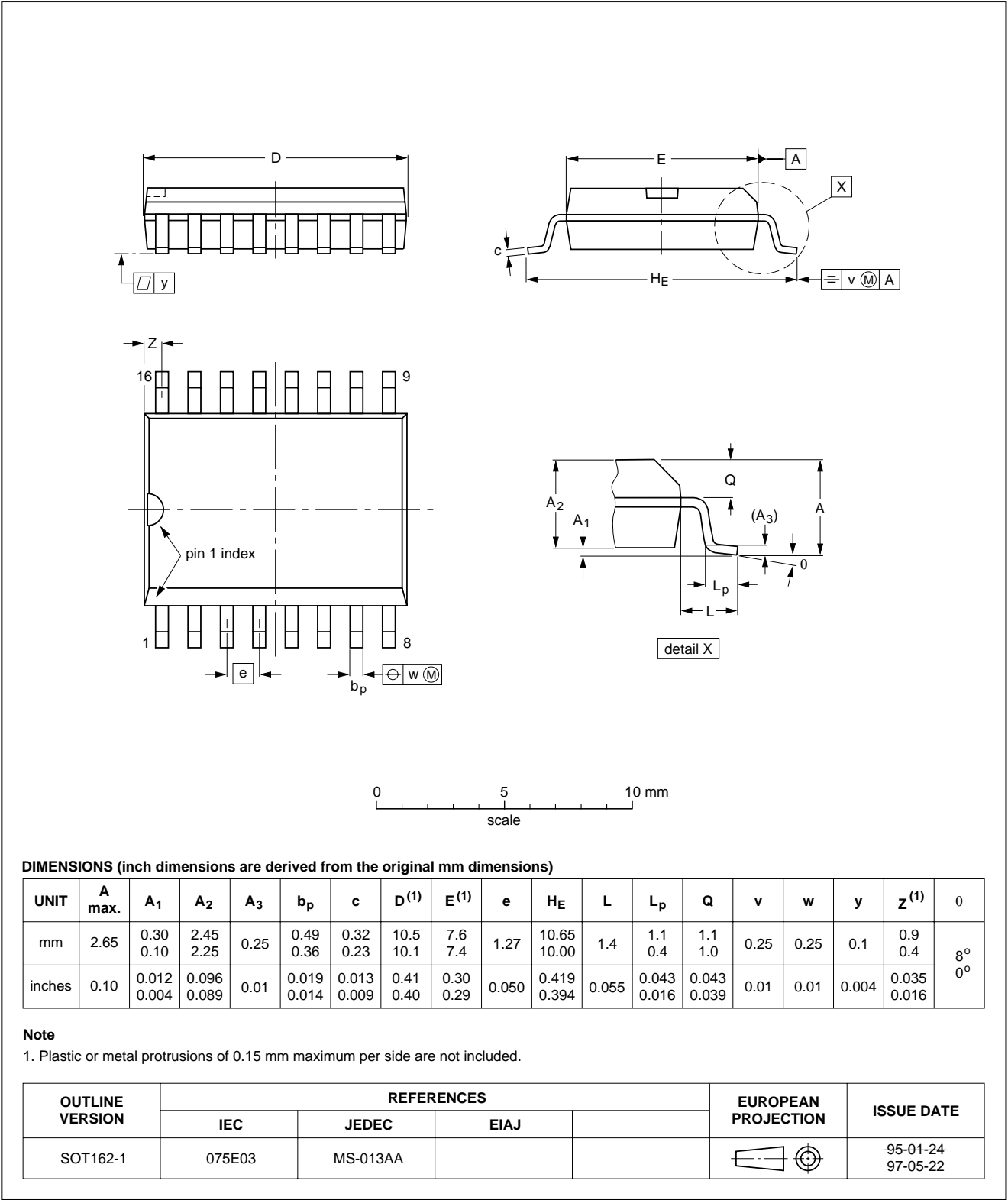


Octuple 6-bit DACs with I²C-bus

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SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1

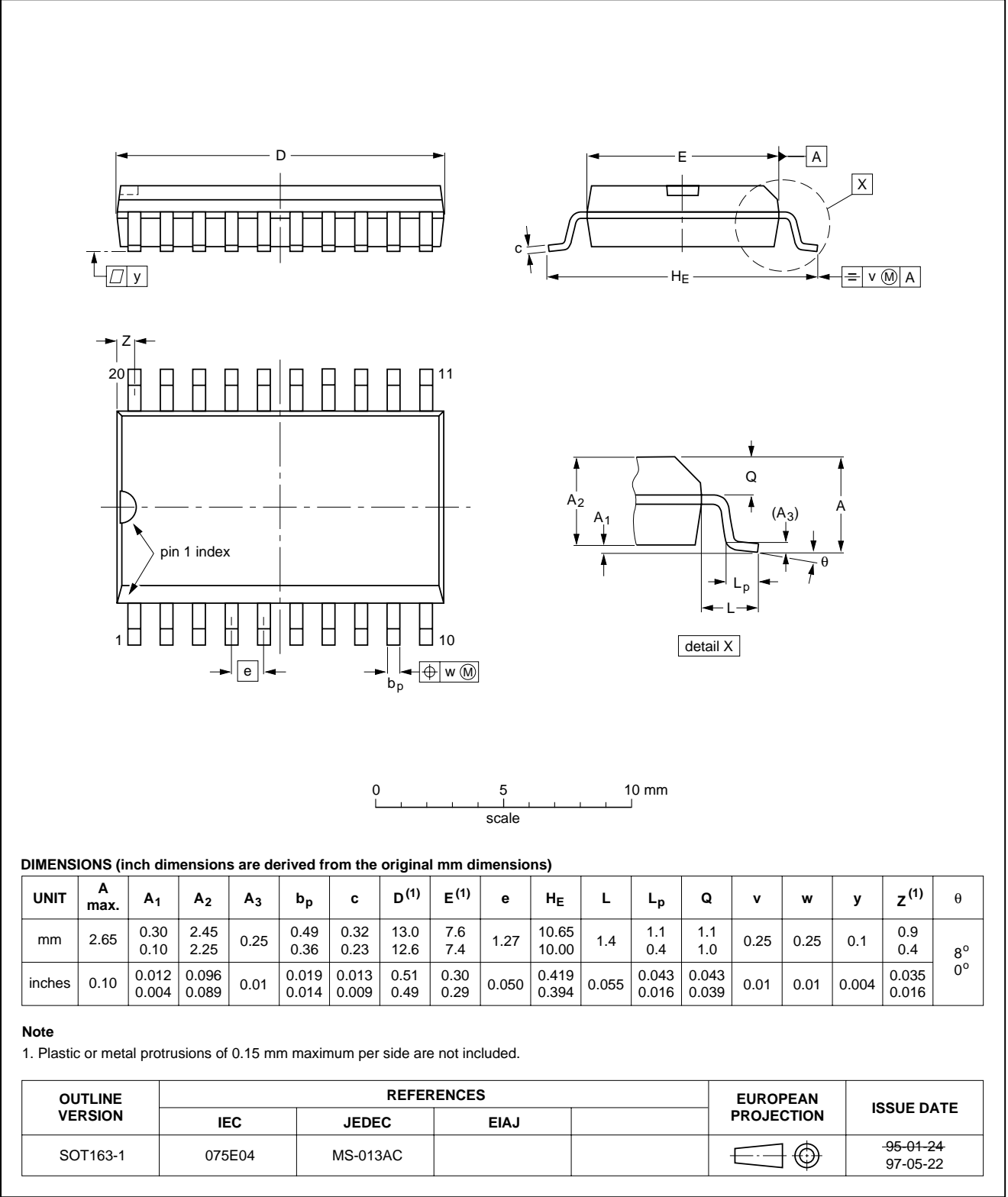


Octuple 6-bit DACs with I²C-bus

TDA8444; TDA8444T;
TDA8444AT

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Octuple 6-bit DACs with I²C-bus

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax. +381 11 63 5777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
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