

N-channel TrenchMOS™ transistor

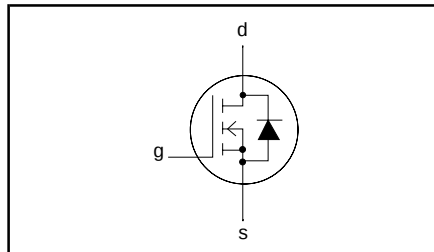
Logic level FET

PHP21N06LT, PHB21N06LT
PHD21N06LT

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Logic level compatible

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 55 \text{ V}$
$I_D = 19 \text{ A}$
$R_{DS(ON)} \leq 75 \text{ m}\Omega \text{ (} V_{GS} = 5 \text{ V)}$
$R_{DS(ON)} \leq 70 \text{ m}\Omega \text{ (} V_{GS} = 10 \text{ V)}$

GENERAL DESCRIPTION

N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using 'trench' technology.

Applications:-

- d.c. to d.c. converters
- switched mode power supplies

The PHP21N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.

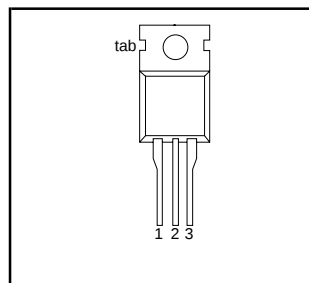
The PHB21N06LT is supplied in the SOT404 (D²PAK) surface mounting package.

The PHD21N06LT is supplied in the SOT428 (DPAK) surface mounting package.

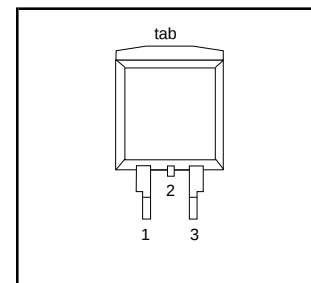
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

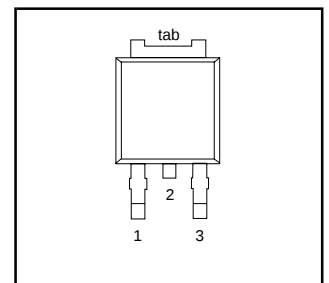
SOT78 (TO220AB)



SOT404 (D²PAK)



SOT428 (DPAK)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25^\circ\text{C}$ to 175°C	-	55	V
V_{DGR}	Drain-gate voltage	$T_j = 25^\circ\text{C}$ to 175°C ; $R_{GS} = 20 \text{ k}\Omega$	-	55	V
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq 150^\circ\text{C}$	-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25^\circ\text{C}$	-	19	A
		$T_{mb} = 100^\circ\text{C}$	-	13	A
I_{DM}	Pulsed drain current	$T_{mb} = 25^\circ\text{C}$	-	76	A
P_D	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	56	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin:2 of the SOT404 or SOT428 packages.

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 9.7$ A; $t_p = 100$ μ s; T_j prior to avalanche = 25°C; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 5$ V; refer to fig:15	-	34	mJ
I_{AS}	Peak non-repetitive avalanche current		-	19	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	2.7	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT428 and SOT404 package, pcb mounted, minimum footprint	60 50	- -	K/W K/W

ELECTRICAL CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA; $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1.0 0.5 -	1.5 - -	2.0 - 2.3	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A $V_{GS} = 5$ V; $I_D = 10$ A $T_j = 175^\circ\text{C}$	- - -	55 60 -	70 75 158	m Ω m Ω m Ω
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 10$ A	5	13	-	S
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5$ V; $V_{DS} = 0$ V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55$ V; $V_{GS} = 0$ V; $T_j = 175^\circ\text{C}$	-	0.05 -	10 500	μ A μ A
$Q_{g(tot)}$	Total gate charge	$I_D = 20$ A; $V_{DD} = 44$ V; $V_{GS} = 5$ V	-	9.4	-	nC
Q_{gs}	Gate-source charge		-	2.2	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	5.4	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30$ V; $R_D = 1.2$ Ω ; $R_G = 10$ Ω ; $V_{GS} = 5$ V	-	7	15	ns
t_r	Turn-on rise time	Resistive load	-	88	120	ns
$t_{d\ off}$	Turn-off delay time		-	25	40	ns
t_f	Turn-off fall time		-	25	45	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	466	650	pF
C_{oss}	Output capacitance		-	95	135	pF
C_{rss}	Feedback capacitance		-	71	85	pF

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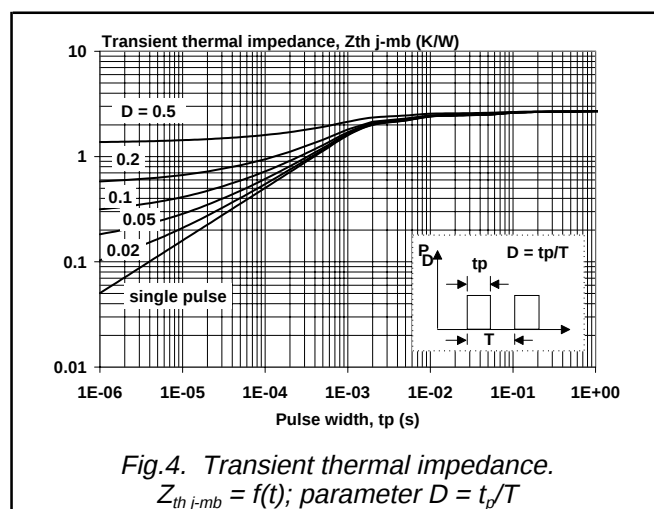
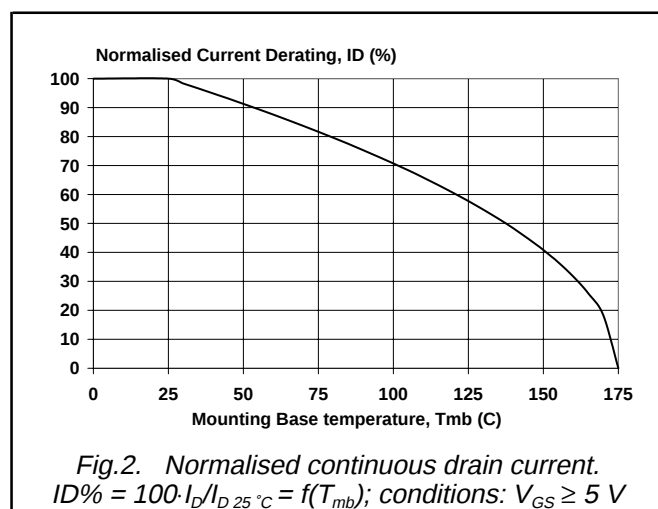
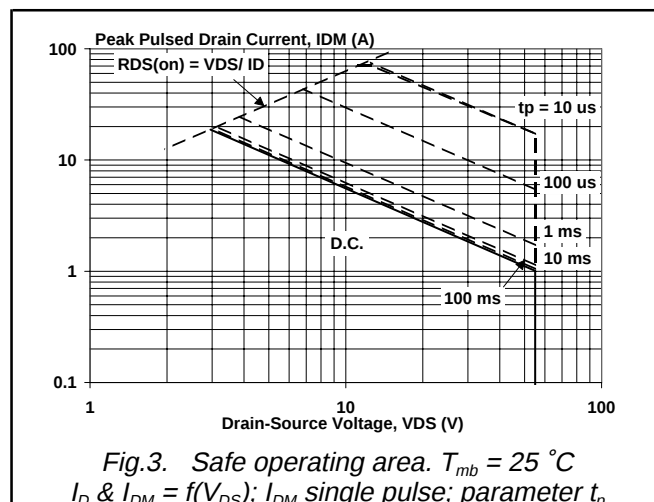
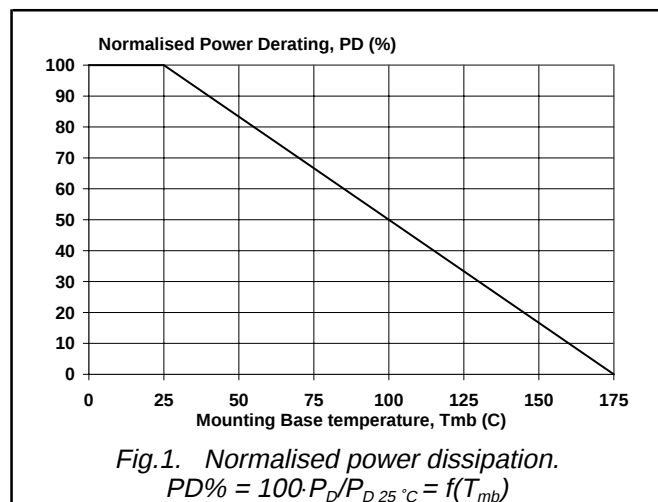
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REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified

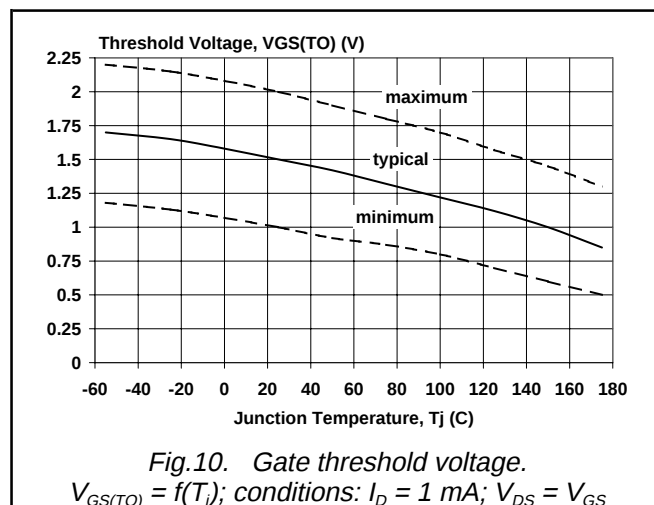
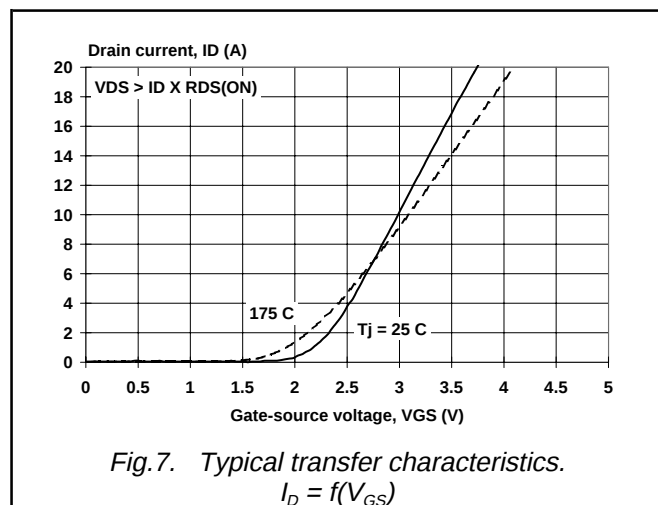
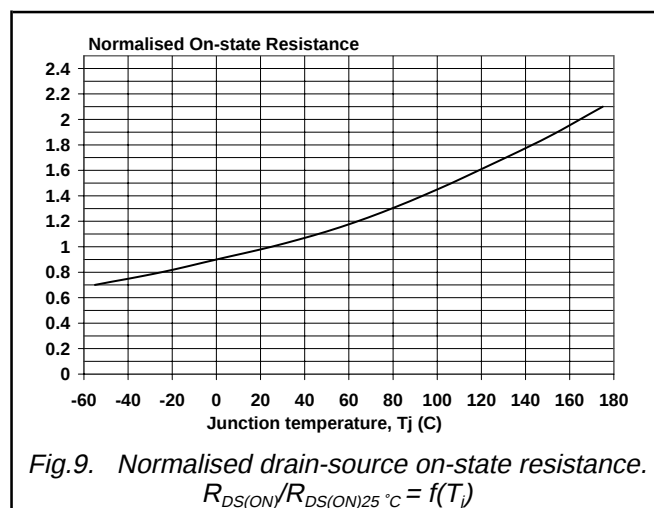
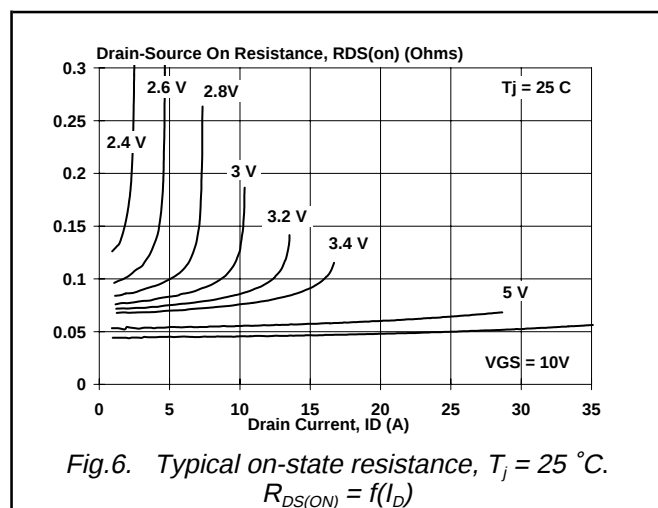
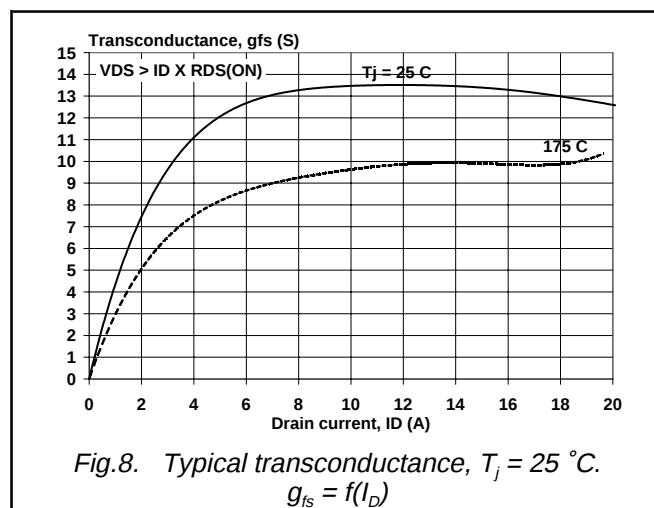
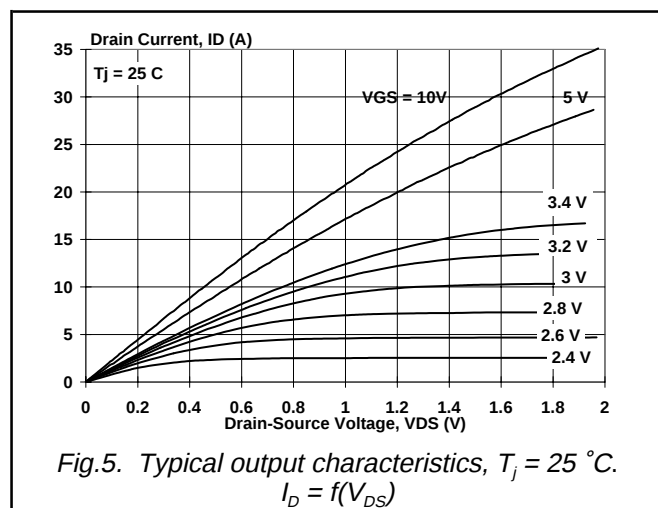
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	19	A
I_{SM}	Pulsed source current (body diode)		-	-	76	A
V_{SD}	Diode forward voltage	$I_F = 20\text{ A}; V_{GS} = 0\text{ V}$	-	1.2	1.5	V
t_{rr}	Reverse recovery time	$I_F = 20\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	43	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	94	-	nC



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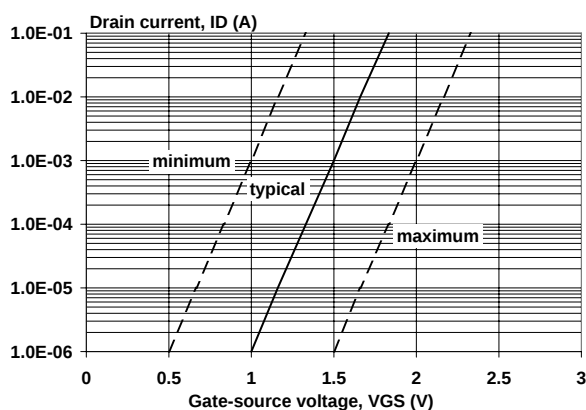


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

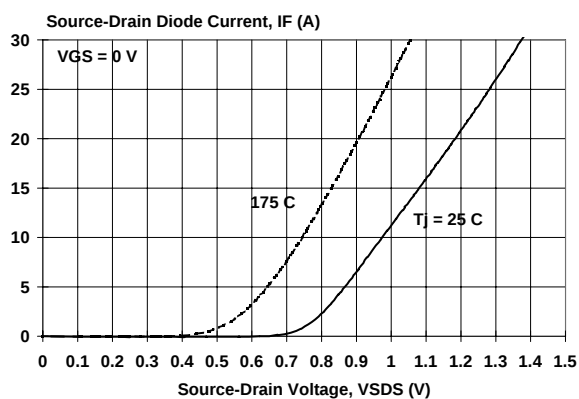


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

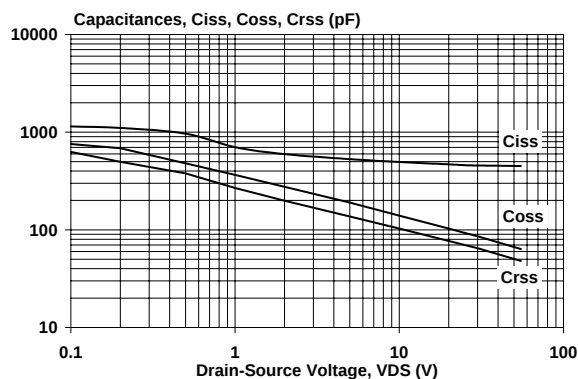


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

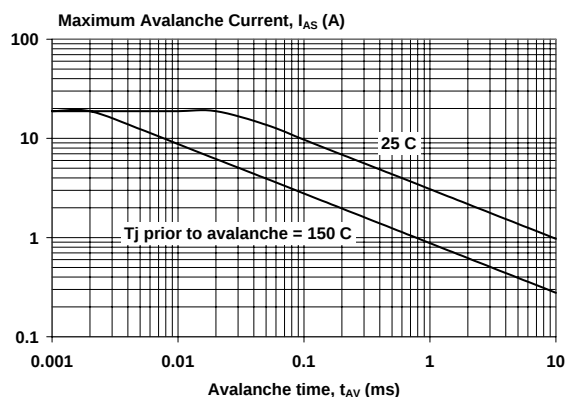


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_{AV}); unclamped inductive load

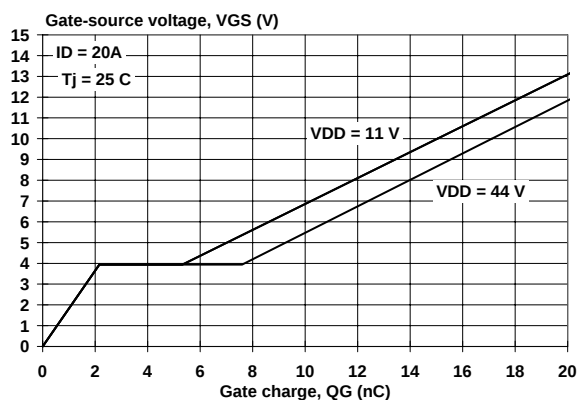
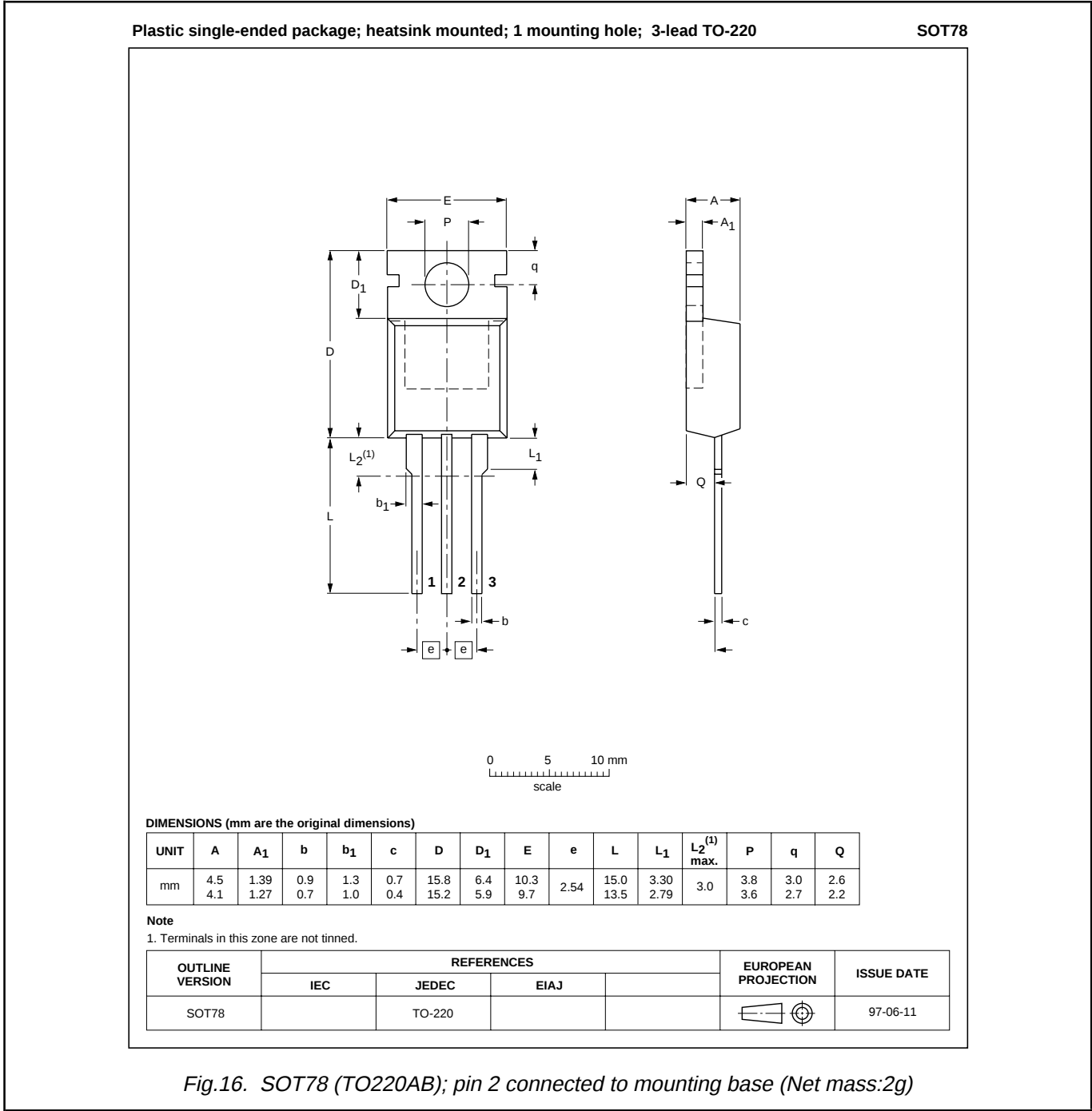


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$

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MECHANICAL DATA



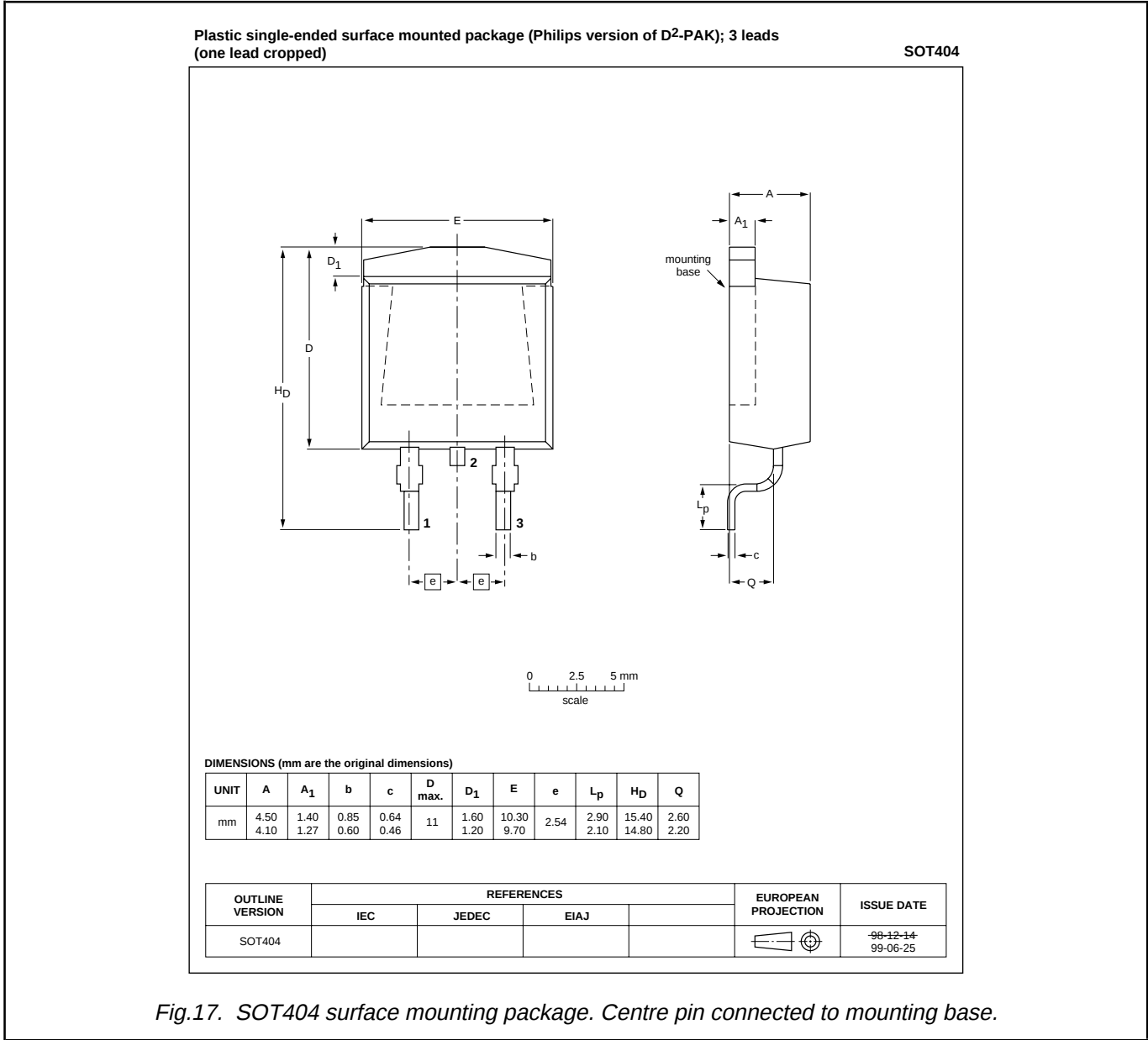
Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

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PHD21N06LT

MECHANICAL DATA



- Notes**
1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
 2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
 3. Epoxy meets UL94 V0 at 1/8".

N-channel TrenchMOSTM transistor
Logic level FET

PHP21N06LT, PHB21N06LT
PHD21N06LT

MOUNTING INSTRUCTIONS

Dimensions in mm

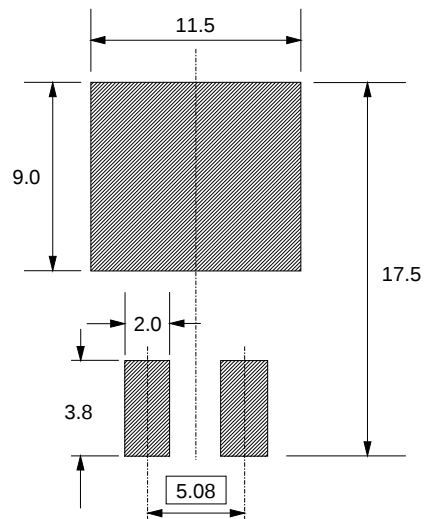
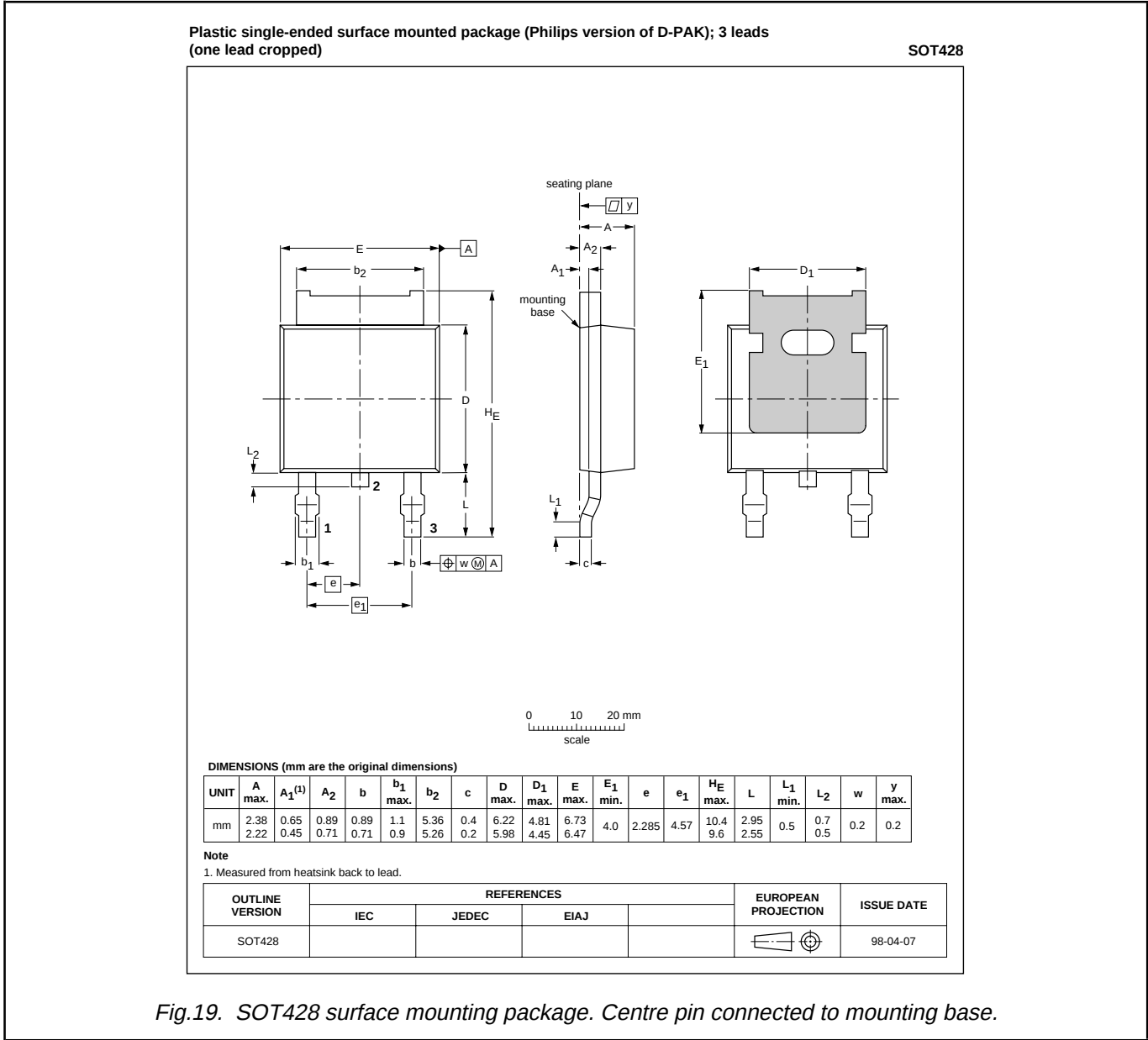


Fig.18. SOT404 : soldering pattern for surface mounting.

N-channel TrenchMOS™ transistor
Logic level FET

PHP21N06LT, PHB21N06LT
PHD21N06LT

MECHANICAL DATA



Notes

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2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

MOUNTING INSTRUCTIONS

N-channel TrenchMOS™ transistor
Logic level FET

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PHD21N06LT

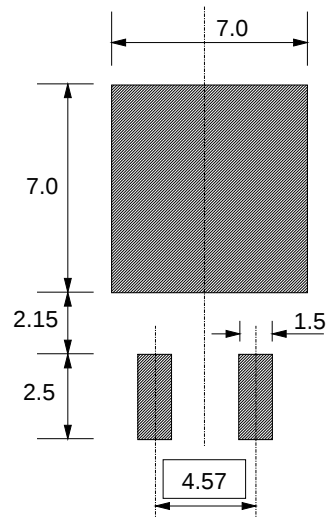
Dimensions in mm

Fig.20. SOT428 : soldering pattern for surface mounting.

N-channel TrenchMOSTM transistor Logic level FET

PHP21N06LT, PHB21N06LT
PHD21N06LT

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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