

DATA SHEET

74ABT540

Octal buffer, inverting (3-State)

Product specification

Supersedes data of 1996 Oct 08

IC23 Data Handbook

1998 Jan 16

Octal buffer, inverting (3-State)

74ABT540

FEATURES

- Octal bus interface
- 3-State buffers
- Live insertion/extraction permitted
- Efficient pinout to facilitate PC board layout
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State

DESCRIPTION

The 74ABT540 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT540 device is an octal inverting buffer that is ideal for driving bus lines. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

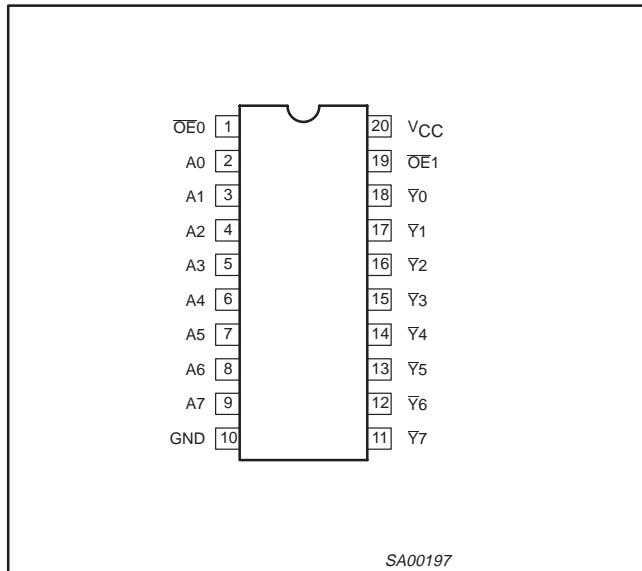
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}$; $\text{GND} = 0\text{V}$	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to \bar{Y}_n	$C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$	3.1	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3	pF
C_{OUT}	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	50	μA

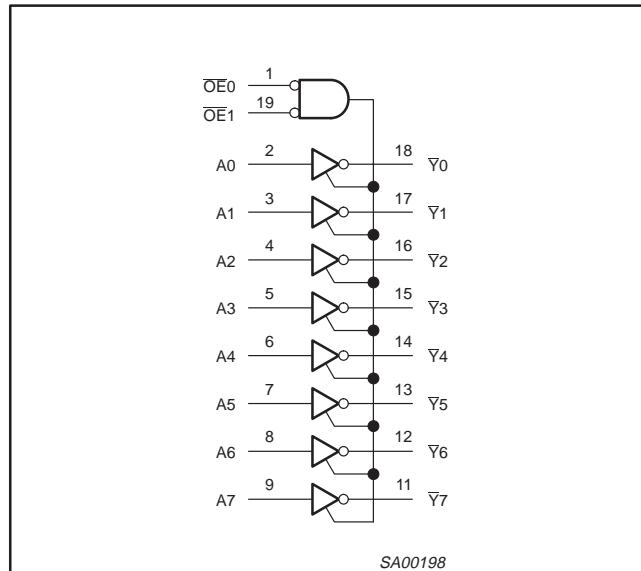
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	-40°C to +85°C	74ABT540 N	74ABT540 N	SOT146-1
20-Pin plastic SO	-40°C to +85°C	74ABT540 D	74ABT540 D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to +85°C	74ABT540 DB	74ABT540 DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40°C to +85°C	74ABT540 PW	74ABT540PW DH	SOT360-1

PIN CONFIGURATION



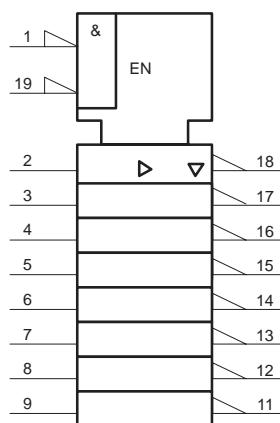
LOGIC SYMBOL



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74ABT540

LOGIC SYMBOL (IEEE/IEC)



SA00199

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	Y0 – Y7	Data outputs
1, 19	OE0, OE1	Output enables
10	GND	Ground (0V)
20	Vcc	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS	
OE0	OE1	An	Yn
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

H = High voltage level

L = Low voltage level

X = Don't care

Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT	
			$T_{amb} = +25^{\circ}\text{C}$			$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		
			Min	Typ	Max	Min		
V_{IK}	Input clamp voltage	$V_{CC} = 4.5\text{V}$; $I_{IK} = -18\text{mA}$		-0.9	-1.2		-1.2	V
V_{OH}	High-level output voltage	$V_{CC} = 4.5\text{V}$; $I_{OH} = -3\text{mA}$; $V_I = V_{IL}$ or V_{IH}	2.5	2.9		2.5		V
		$V_{CC} = 5.0\text{V}$; $I_{OH} = -3\text{mA}$; $V_I = V_{IL}$ or V_{IH}	3.0	3.4		3.0		V
		$V_{CC} = 4.5\text{V}$; $I_{OH} = -32\text{mA}$; $V_I = V_{IL}$ or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.5\text{V}$; $I_{OL} = 64\text{mA}$; $V_I = V_{IL}$ or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	$V_{CC} = 5.5\text{V}$; $V_I = \text{GND}$ or 5.5V		± 0.01	± 1.0		± 1.0	μA
I_{OFF}	Power-off leakage current	$V_{CC} = 0.0\text{V}$; V_I or $V_O \leq 4.5\text{V}$		± 5.0	± 100		± 100	μA
I_{PU}/I_{PD}	Power-up/down 3-State output current ³	$V_{CC} = 2.1\text{V}$; $V_O = 0.5\text{V}$; $V_I = \text{GND}$ or V_{CC} ; V_{OE} = Don't care		± 5.0	± 50		± 50	μA
I_{OZH}	3-State output High current	$V_{CC} = 5.5\text{V}$; $V_O = 2.7\text{V}$; $V_I = V_{IL}$ or V_{IH}		5.0	50		50	μA
I_{OZL}	3-State output Low current	$V_{CC} = 5.5\text{V}$; $V_O = 0.5\text{V}$; $V_I = V_{IL}$ or V_{IH}		-5.0	-50		-50	μA
I_{CEX}	Output High leakage current	$V_{CC} = 5.5\text{V}$; $V_O = 5.5\text{V}$; $V_I = \text{GND}$ or V_{CC}		5.0	50		50	mA
I_O	Output current ¹	$V_{CC} = 5.5\text{V}$; $V_O = 2.5\text{V}$	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	$V_{CC} = 5.5\text{V}$; Outputs High, $V_I = \text{GND}$ or V_{CC}		50	250		250	μA
I_{CCL}		$V_{CC} = 5.5\text{V}$; Outputs Low, $V_I = \text{GND}$ or V_{CC}		24	30		30	mA
I_{CCZ}		$V_{CC} = 5.5\text{V}$; Outputs 3-State; $V_I = \text{GND}$ or V_{CC}		50	250		250	μA
ΔI_{CC}	Additional supply current per input pin ²	Outputs enabled, one input at 3.4V , other inputs at V_{CC} or GND ; $V_{CC} = 5.5\text{V}$		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V , other inputs at V_{CC} or GND ; $V_{CC} = 5.5\text{V}$		0.5	50		50	μA
		Outputs 3-State, one enable input at 3.4V , other inputs at V_{CC} or GND ; $V_{CC} = 5.5\text{V}$		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V .
3. This parameter is valid for any V_{CC} between 0V and 2.1V , with a transition time of up to 10msec . From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$ a transition time of up to $100\mu\text{sec}$ is permitted.

Octal buffer, inverting (3-State)

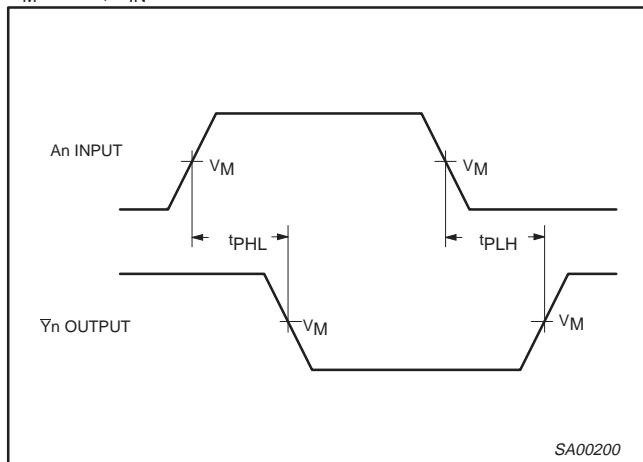
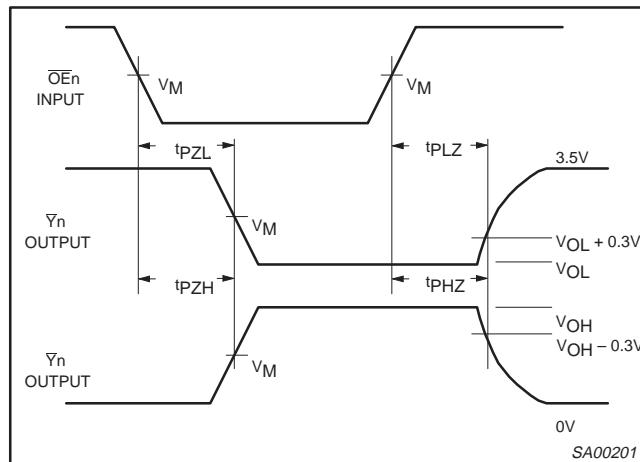
74ABT540

AC CHARACTERISTICS

 $V_{IN} = 0V$; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

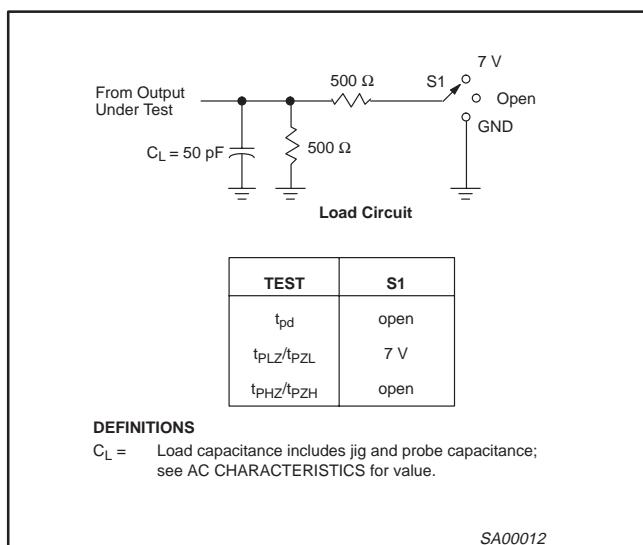
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT	
			$T_{amb} = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$			$T_{amb} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$			
			Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation delay An to \bar{Y}_n	1	1.0 1.0	2.9 3.1	4.1 4.3	1.0 1.0	4.8 4.8	ns	
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.1	4.1 4.6	4.9 5.8	1.1 1.1	5.9 6.4	ns	
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.2	3.6 2.9	6.8 5.7	1.5 1.2	7.3 6.2	ns	

AC WAVEFORMS

 $V_M = 1.5\text{V}$, $V_{IN} = \text{GND to } 3.0\text{V}$ Waveform 1. Waveforms Showing the Input (An) to Output (\bar{Y}_n) Propagation Delays

Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

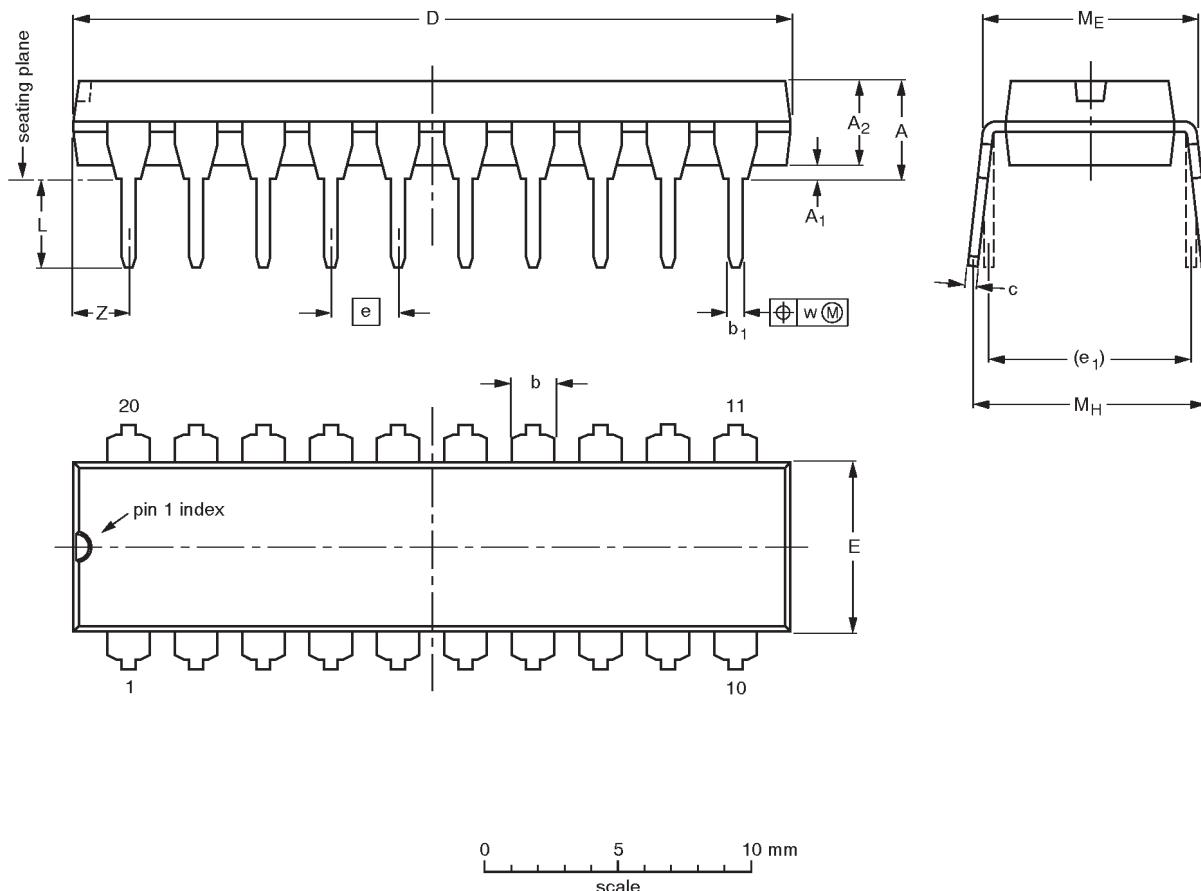


Octal buffer, inverting (3-State)

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

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UNIT	A _{max.}	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

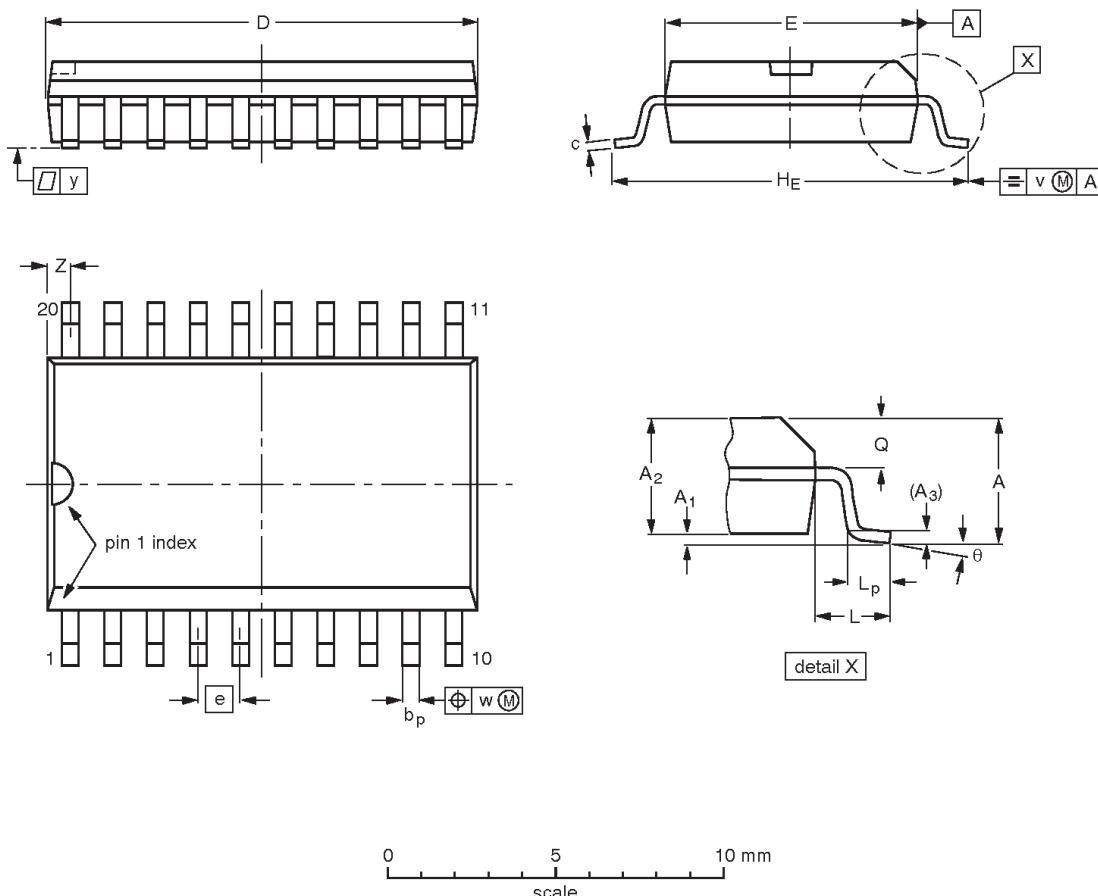
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603		 	92-11-17 95-05-24

Octal buffer, inverting (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65 0.10	0.30 2.25	2.45	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10 0.004	0.012 0.089	0.096	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

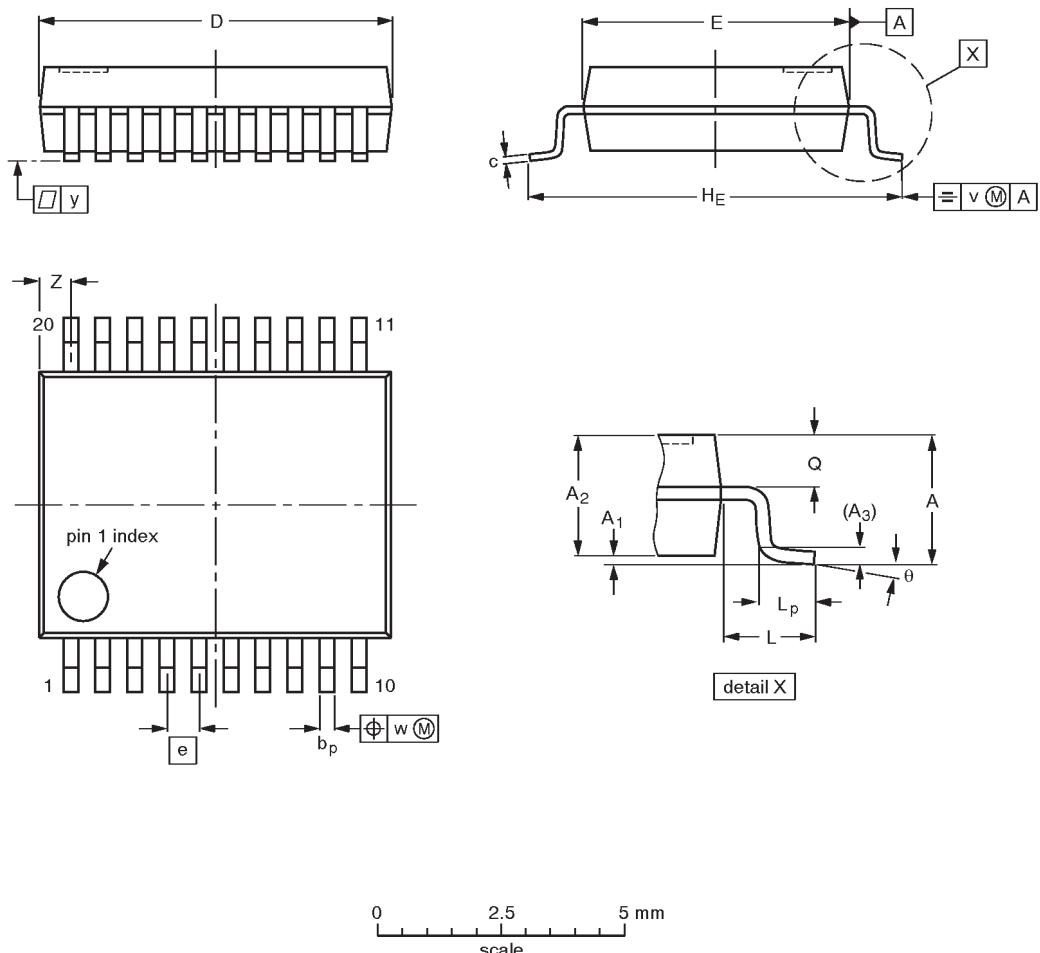
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT163-1	075E04	MS-013AC			92-11-17 95-01-24

Octal buffer, inverting (3-State)

74ABT540

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0 0.05	0.21 1.65	1.80	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

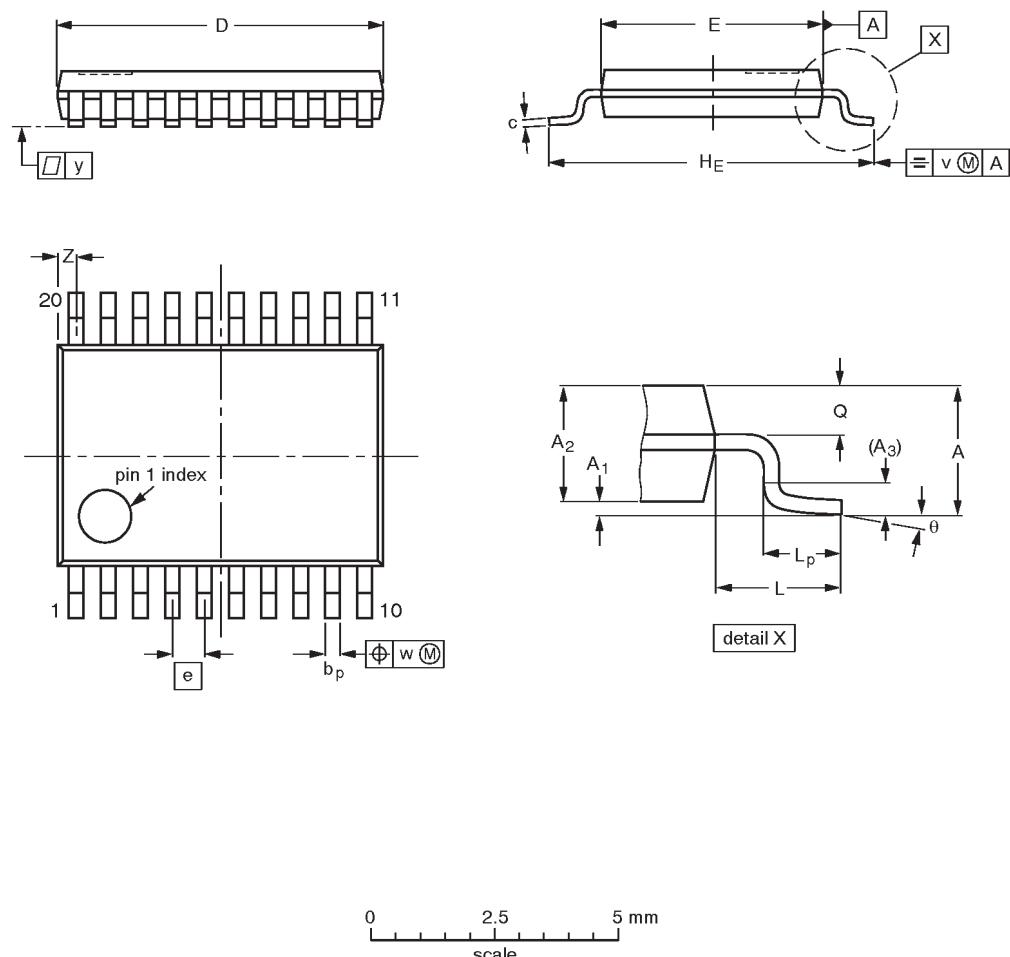
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT339-1		MO-150AE			93-09-08 95-02-04

Octal buffer, inverting (3-State)

74ABT540

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10 0.05	0.15 0.080	0.95	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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