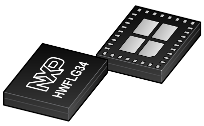


WLAN8101H

2.4 GHz Wi-Fi 6 Front-End Module

Rev. 6 — 11 August 2020 **Product data sheet**

1 General description

The WLAN8101H is a 2.4 GHz 2 x 2 MIMO RFFE for Wi-Fi 6 applications in a 3 mm x 4 mm package.

The WLAN8101H includes two monolithic front-end ICs. Each front-end IC includes a transmit amplifier with directional coupler, a low-noise receive amplifier and a transmit/ receive switch with a Bluetooth channel. The power amplifier supports 3 different TX gain modes to improve power efficiency. The directional coupler improves transmit-power sensing accuracy.

WLAN8101H also includes coexistence filters for both transmit and receive channels.

The device is matched to 50 Ω and integrates harmonic and out of band filtering which minimizes the layout area in the application.

2 Features and benefits

- Small-size 2 x 2 MIMO RFFE for Wi-Fi 6 applications
- Integrated power amplifiers with multiple operation modes for dynamic power efficiency and linearity control
- Full ISM band 2.402 GHz to 2.482 GHz
- 3 TX operation modes enabling flexibility for power efficiency adaptation
- Integrated low-noise amplifiers supporting high gain and bypass modes
- Integrated SPDT switches for single antenna RX and TX operation
- Integrated directional couplers for precise transmit power control
- Requires no external matching components, DC free RF ports, except for the ANT, and BT ports (on-chip ESD coil)
- Integrated RF decoupling capacitors for all V_{CC} and control pins
- Low profile, small-size 3 mm x 4 mm package
- Integrated ESD protection on all pins
  – Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001 exceeds 2 kV
  – Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002 exceeds 500 V except for ANT pins the value is 400 V

3 Applications

- Wi-Fi 6 support
- Smartphones, tablets, netbooks, and other portable computing devices
- Module applications for embedded systems

4 Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = - 30 dBm for RX, P_i = -10 dBm for TX, and BT, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RF performance from ANT to RX						
I_{CC}	supply current	RX_gain	-	10.5	-	mA
		RX_bypass [1]	-	24	-	μA
G_p	power gain	RX_gain	-	16.5	-	dB
		RX_bypass	-	-5.5	-	dB
NF	noise figure	RX_gain	-	2	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression point	RX_gain	-	-6.5	-	dBm
RL_i	input return loss	RX_gain mode, P_i = -20 dBm, looking into ANT pin	-	10.5	-	dB
		RX_bypass mode, looking into ANT pin	-	13.5	-	dB
RL_o	output return loss	RX_gain mode, P_i = -20 dBm, looking into RX pin	-	12	-	dB
		RX_bypass mode, looking into RX pin	-	14	-	dB
RF performance from TX to ANT						
I_{CC}	supply current	TX_gain1, P_o = 20.5 dBm	-	285	-	mA
G_p	power gain	TX_gain1	-	32.5	-	dB
		TX_gain2	-	30	-	dB
		TX_gain3	-	18	-	dB
G_{flat}	gain flatness	all TX_gain modes, 40 MHz bandwidth	-	+/-0.25	-	dB
		all TX_gain modes, for entire frequency range	-	+/-0.75	-	dB
EVM_{dyn}	dynamic error vector magnitude	11ax MCS10/11, HE40, TX_gain1, P_o = 14.5 dBm, 180 μs burst, 50 % duty cycle	-	-45	-	dB
RL_i	input return loss	TX_gain1, and TX_gain2 looking into TX pin	-	12	-	dB
		TX_gain3, looking into TX pin	-	10	-	dB
RL_o	output return loss	all TX_gain modes, looking into ANT pin	-	12	-	dB
RF performance from BT to ANT						
I_{CC}	supply current	BT_gain, NO RF	-	70	-	mA
		BT_bypass	-	24	-	μA
G_p	power gain	BT_gain	-	23	-	dB
		BT_bypass	-	-2.1	-	dB
RL_i	input return loss	BT_gain, looking into BT pin	-	7	-	dB
		BT_bypass mode, looking into BT pin	-	15	-	dB
RL_o	output return loss	BT_gain, looking into ANT pin	-	12	-	dB
		BT_bypass, looking into ANT pin	-	15	-	dB

Table 1. Quick reference data...*continued*

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = - 30 dBm for RX, P_i = -10 dBm for TX, and BT, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$EVM_{dif(peak)}$	peak differential error vector magnitude	BT_gain, 8DPSK, P_o = 19 dBm	-	2.5	-	%
$EVM_{diff(RMS)}$	RMS differential error vector magnitude	BT_gain, 8DPSK, P_o = 19 dBm	-	1	-	%
ISL_r	reverse isolation	BT_gain	-	32	-	dB

[1] total leakage of both channels

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
WLAN8101H	WLAN8101H MP	HFCPLGA38	3 mm x 4 mm x 0.65 mm package, 0.35 mm pitch, 38 pins	SOT2022-1

6 Marking

Table 3. Marking

Type number	Marking code
WLAN8101H	8101H

7 Functional diagram

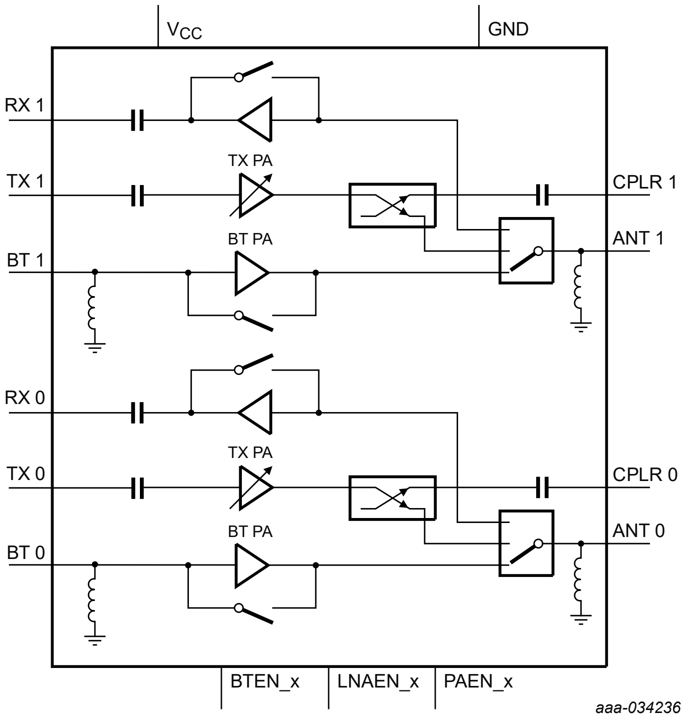


Figure 1. Functional diagram. The x at the control pins stands for port 0 and port 1.

8 Pinning information

8.1 Pinning diagram

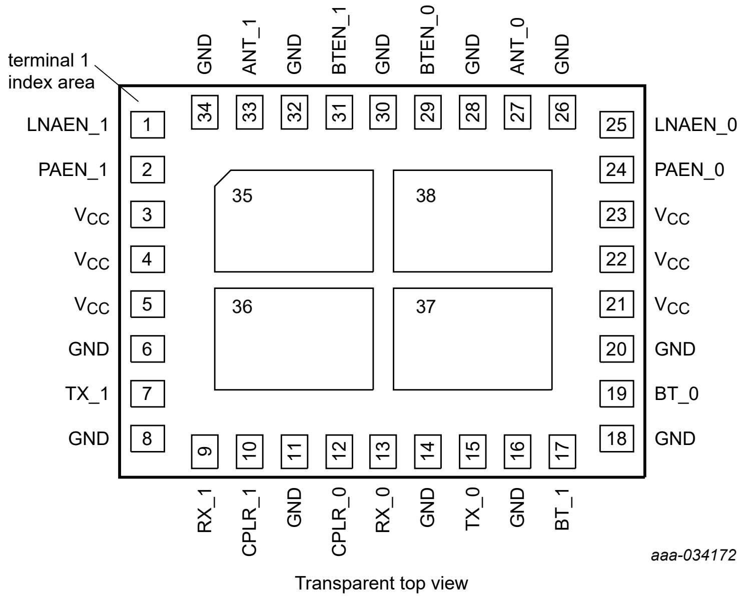


Figure 2. Pinning diagram

8.2 Pin description

Table 4. Pin description

Pin	Symbol	Description
6, 8, 11, 14, 16, 18, 20, 26, 28, 30, 32, 34, 35, 36, 37, and 38	GND	Ground
1	LNAEN_1	LNA enable
2	PAEN_1	PA enable
3, 4, 5, 21, 22, and 23	V_{CC}	supply voltage
7	TX_1	TX port
9	RX_1	RX port
10	CPLR_1	coupler port
12	CPLR_0	coupler port
13	RX_0	RX port
15	TX_0	TX port
17	BT_1	Bluetooth port
19	BT_0	Bluetooth port
24	PAEN_0	PA enable
25	LNAEN_0	LNA enable
27	ANT_0	antenna port

Table 4. Pin description*...continued*

Pin	Symbol	Description
29	BTEN_0	Blue Tooth enable
31	BTEN_1	Blue Tooth enable
33	ANT_1	antenna port

9 Functional description

9.1 Parallel interface control states per MIMO channel

Table 5. Parallel interface control states per MIMO channel

Control pins , BTEN_x, LNAEN_x, and PAEN_x, contain internal pull-down resistors. The parallel interface table applies to both _0 and _1 control pins.[1]

BTEN_x	LNAEN_x	PAEN_x	Signal routing	Operating mode	Mode description	LNA	PA
0	0	1	TX to ANT	TX_gain1	high gain, high linearity	off	on
1	0	1	TX to ANT	TX_gain2	3 dB back off	off	on
1	1	1	TX to ANT	TX_gain3	low gain mode	off	on
0	1	0	ANT to RX	RX_gain		on	off
0	0	0	ANT to RX	RX_bypass		off	off
1	0	0	BT to ANT	BT_bypass		off	off
1	1	0	BT to ANT	BT_gain		off	on
0	1	1	n.a.	reserved		-	-
x	x	x	n.a.	reserved		-	-

[1] Binary represented logic levels, where 0 denotes a logic low ($V_i \leq V_{IL}$) and 1 denotes a logic high ($V_i \geq V_{IH}$)

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{cc}	supply voltage		-0.3	-	6	V
V_i	input voltage	on pin BTEN_x, LNAEN_x, and PAEN_x	-0.3	-	3.6	V
P_i	input power	on ANT_x pin, RX_gain, MCS0	-	-	10	dBm
		on ANT_x pin, RX_bypass, MCS0	-	-	15	dBm
		TX_x pin, TX_gain1, MCS0	-	-	10	dBm
		BT_x pin, BT_gain mode GFSK	-	-	10	dBm
		BT_x pin, BT_bypass mode GFSK	-	-	28	dBm
TX_RUG	TX ruggedness (no irreversible damage)	V_{CC} = 4.75 V, applied to TX_gain1 mode, P_o = 26.5 dBm_MCS0, at 50 Ω, the required P_i level is kept constant during ruggedness test, VSWR all phases	-	10:1	-	-
BT_RUG	BT ruggedness (no irreversible damage)	V_{CC} = 4.75 V, applied in BT_gain mode. P_o = 25 dBm_GFSK at 50 Ω, the required P_i level is kept constant during ruggedness test, VSWR all phases	-	10:1	-	-
T_{stg}	storage temperature		-55	-	125	°C
T_j	junction temperature		-	-	175	°C
T_{mb}	mounting base temperature	-	-	-	100	°C
V_{ESD}	Electrostatic Discharge Voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001	-	2	-	kV
		Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002				
		pins ANT_0, and ANT_1	-	400	-	V
		all other pins	-	500	-	V

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{oper}	operating frequency		2.402	-	2.482	GHz
V_{CC}	supply voltage	on pin V_{CC} [1] [2]	2.7	3.85	4.75	V
V_{IH}	HIGH-level input voltage		1.6	-	3.6	V
V_{IL}	LOW-level input voltage		0		0.4	V
T_{amb}	ambient temperature		-40	25	85	°C

[1] Product is functional with reduced performance at supply voltages from 2.5 V to 2.7 V.

[2] Product withstands 30000 charger insert and pull-out events with a duration of 100 ms and a maximum supply voltage of 5.25 V.

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	junction to mounting base thermal resistance		-	25	-	K/W

13 Characteristics

13.1 Switching time performance

Table 9. Switching time performance

T_{amb} = 25 °C; V_{CC1} = V_{CC2} = V_{CC3} = 3.85 V; All ports are terminated with 50 Ω.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{on(LNA)}$	LNA turn-on time	from 10 % of control signal to 90 % LNA output level, RX_bypass to LNA transition	-	150	- -	ns
$t_{off(LNA)}$	LNA turn-off time	from 90 % of control signal to 10 % LNA output level, LNA to RX_bypass transition	-	100	- -	ns
$t_{on(TX)}$	TX turn-on time	from 10 % of control signal to 94 % TX output level, RX_bypass to TX transition				
		TX_gain1, and TX_gain2	-	350	-	ns
		TX_gain3	-	630	-	ns
$t_{off(TX)}$	TX turn-off time	from 90 % of control signal to 10 % TX output level, TX to RX_bypass transition	-	400	-	ns
$t_{on(BT)}$	BT turn-on time	from 10 % of control signal to 90 % of BT output level, RX_bypass to BT_gain transition	-	350	-	ns
$t_{off(BT)}$	BT turn-off time	from 90 % of control signal to 10 % of BT output level, BT_gain to RX_bypass transition	-	400	-	ns

13.2 RF Performance from ANT to RX

Table 10. RF Performance from ANT to RX

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = - 30 dBm for RX, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	RX_gain	-	10.5	-	mA
		RX_bypass [1]	-	24	-	μA
G_p	power gain	RX_gain	-	16.5	-	dB
		RX_bypass	-	-5.5	-	dB
G_{flat}	power gain flatness	RX_gain, peak-to-peak over any 40 MHz band	-	+/-0.25	-	dB
		RX_gain, over full RF bandwidth	-	+/-0.75	-	dB
		RX_bypass, peak-to-peak over any 40 MHz band	-	+/-0.25	-	dB
		RX_bypass, over full RF bandwidth	-	+/-0.75	-	dB
NF	noise figure	RX_gain	-	2	-	dB
RL_i	input return loss	RX_gain, P_i = -20 dBm, looking into ANT pin	-	10.5	-	dB
		RX_bypass, looking into ANT pin	-	13.5	-	dB
RL_o	output return loss	RX_gain, P_i = -20 dBm, looking into RX pin	-	12	-	dB
		RX_bypass, looking into RX pin	-	14	-	dB

Table 10. RF Performance from ANT to RX*...continued*

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = - 30 dBm for RX, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$IP3_i$	input third order intercept point	RX_gain [2]	-	4.5	-	dBm
		RX_bypass [3]	-	35	-	dBm
$P_{i(1dB)}$	input power at 1 dB gain compression point	RX_gain	-	-6.5	-	dBm
		RX_bypass	-	18	-	dBm

[1] total leakage of both channels
[2] P_i = -20 dBm/tone, (20 MHz tone spacing)
[3] P_i = -3 dBm/tone, (20 MHz tone spacing)

13.3 RF Performance from TX to ANT

Table 11. RF Performance from TX to ANT

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L= 50 Ω; P_i = -10 dBm for TX, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured with product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	TX_gain1, no RF	-	195	-	mA
		TX_gain2, no RF	-	140	-	mA
		TX_gain3, no RF	-	60	-	mA
		TX_gain1, P_o = 16.5 dBm HE40	-	230	-	mA
		TX_gain1, P_o = 19 dBm HT20	-	260	-	mA
		TX_gain1, P_o = 20.5 dBm HT40	-	285	-	mA
		TX_gain1, P_o = 22.5 dBm 11g, 6 Mb/s	-	335	-	mA
		TX_gain1, P_o = 24.5 dBm CCK	-	405	-	mA
		TX_gain2, P_o = 16 dBm HT20	-	180	-	mA
		TX_gain2, P_o = 17.5 dBm HT40	-	195	-	mA
		TX_gain2, P_o = 19.5 dBm 11g, 6 Mb/s	-	220	-	mA
		TX_gain3, P_o = 9 dBm HT40	-	65	-	mA
G_p	power gain	TX_gain1	-	32.5	-	dB
		TX_gain2	-	30	-	dB
		TX_gain3	-	18	-	dB
G_{flat}	gain flatness	all TX_gain modes, 40 MHz bandwidth	-	+/-0.25	-	dB
		all TX_gain modes, for entire frequency range	-	+/-0.75	-	dB
RL_i	input return loss	TX_gain1, and TX_gain2 looking into TX pin	-	12	-	dB
		TX_gain3, looking into TX pin	-	10	-	dB
RL_o	output return loss	TX_gain1, looking into ANT pin	-	12	-	dB
		TX_gain2, looking into ANT pin	-	12	-	dB
		TX_gain3, looking into ANT pin	-	12	-	dB
SEM_{margin}	margin to spectrum emission mask	11n, MCS0, 20 MHz, 180 μs burst, 50 % duty cycle				
		TX_gain1, P_o = 21 dBm, ± 11 MHz	-	10	-	dB
		TX_gain1, P_o = 21 dBm, ± 20 MHz	-	9	-	dB
		TX_gain1, P_o = 21 dBm, ± 30 MHz [1]	-	3	-	dB
		11g_6M, 180 μs burst, 50 % duty cycle				
		TX_gain1, P_o = 21.5 dBm, ± 11 MHz	-	12	-	dB
		TX_gain1, P_o = 21.5 dBm, ± 20 MHz	-	9	-	dB
		TX_gain1, P_o = 21.5 dBm, ± 30 MHz	-	3	-	dB
		11b_CCK, 180 μs burst, 50 % duty cycle				
		TX_gain1, P_o = 23 dBm, ± 11 MHz	-	12	-	dB
		TX_gain1, P_o = 23 dBm, ± 22 MHz	-	6	-	dB

Table 11. RF Performance from TX to ANT*...continued*

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L= 50 Ω; P_i = -10 dBm for TX, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured with product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EVM_{dyn}	dynamic error vector magnitude	11n, MCS0, 20 MHz, 180 µs burst, 50 % duty cycle				
		TX_gain1, P_o = 22 dBm	-	-26	-	dB
		TX_gain2, P_o = 19 dBm	-	-33	-	dB
		11n, MCS7, HT20, 180 µs burst, 50 % duty cycle				
		TX_gain1, P_o = 20.5 dBm	-	-31	-	dB
		TX_gain2, P_o = 17.5 dBm	-	-37	-	dB
		11ax, MCS10, and MCS11, HE40, 180 µs burst, 50 % duty cycle				
		TX_gain1, P_o = 16.5 dBm	-	-41.5	-	dB
		TX_gain1, P_o = 14.5 dBm	-	-45	-	dB
		TX_gain2, P_o = 13.5 dBm	-	-42.5	-	dB
		TX_gain2, P_o = 11.5 dBm	-	-44.5	-	dB
		TX_gain3, P_o = 4 dBm	-	-47	-	dB
α2H	second harmonic emission level	TX_gain1, P_o = 22.5 dBm, 11b_CCK	-	-21	-	dBm/MHz
		TX_gain2, P_o = 19.5 dBm, 11b_CCK	-	-23	-	dBm/MHz
α3H	third harmonic emission level	TX_gain1, P_o = 22.5 dBm, 11b_CCK	-	-37	-	dBm/MHz
		TX_gain2, P_o = 19.5 dBm, 11b_CCK	-	-44	-	dBm/MHz

[1] can be improved with optimized matching

13.4 RF Performance from BT to ANT

Table 12. RF Performance from BT to ANT

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = -10 dBm for BT, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	BT_gain				
		No RF	-	70	-	mA
		P_o = 16.5 dBm	-	100	-	mA
		P_o = 18.5 dBm	-	115	-	mA
		P_o = 20.5 dBm	-	130	-	mA
		BT_bypass [1]	-	24	-	µA
G_p	power gain	BT_gain	-	23	-	dB
		BT_bypass	-	-2.1	-	dB
RL_i	input return loss	BT_gain	-	7	-	dB
		BT_bypass	-	15	-	dB

Table 12. RF Performance from BT to ANT*...continued*

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = -10 dBm for BT, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RL_o	output return loss	all BT modes	-	12	-	dB
		BT_bypass	-	15	-	dB
ACP	Adjacent channel power	BT_gain, GFSK P_o = 22 dBm				
		at +/- 2 MHz offset	-	-46	-	dBm
		at +/- 3 MHz offset	-	-52	-	dBm
$e_{sp(ib)}$	Inband spurious emission	BT_gain, 8DPSK, and Pi/4-DQPSK, P_o = 19 dBm				
		at +/- 2 MHz offset	-	-21	-	dBm
		at +/- 3 MHz offset	-	-40	-	dBm
$EVM_{dif(peak)}$	peak differential error vector magnitude	BT_gain, 8DPSK P_o = 19 dBm	-	2.5	-	%
$EVM_{diff(RMS)}$	RMS differential error vector magnitude	BT_gain, 8DPSK P_o = 19 dBm	-	1	-	%
ISL_r	reverse isolation	BT_gain	-	32	-	dB

[1] one channel in BT_bypass, one channel in RX_bypass

13.5 Directional Coupler

Table 13. Power coupler RF Performance

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = - 30 dBm for RX, P_i = -10 dBm for TX, f = 2.402 GHz to 2.482 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12719)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{cpl}	coupling ratio	TX_gain1, and TX_gain2	-	25.5	-	dB
$\Delta R_{cpl(f)}$	variation of coupling ratio over frequency	measured in all TX_gain modes	-	+/-0.3	-	dB
D	directivity	TX_gain1	-	17	-	dB
		TX_gain2	-	19	-	dB
$RL_{i(CPLR)}$	coupler input return loss	looking into CPLR pin	-	9.5	-	dB

14 Graphics

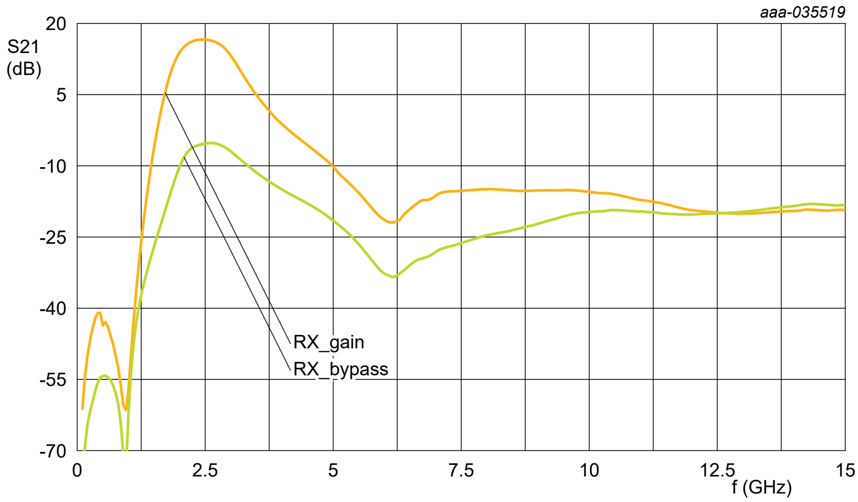


Figure 3. Typical RX_gain and RX_bypass transfer functions (S21)

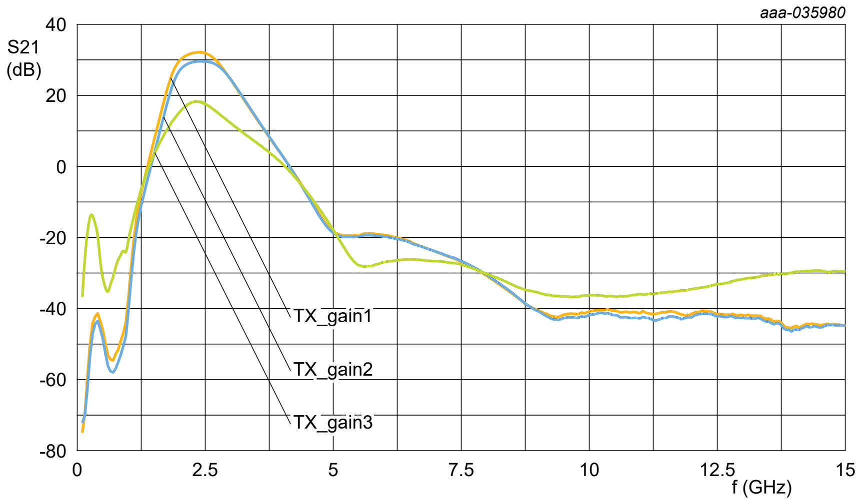


Figure 4. Typical TX modes transfer functions (S21)

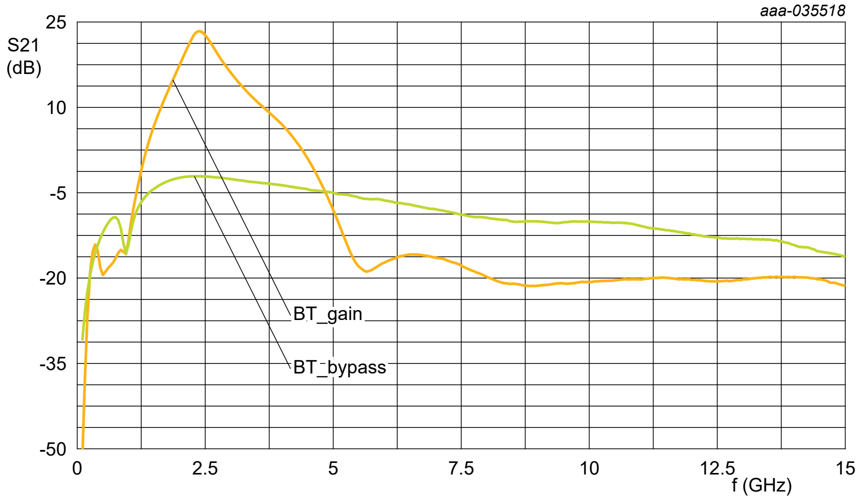


Figure 5. Typical BT_gain and BT_bypass modes transfer functions (S21)

15 Package outline

Table 14. Package outline SOT2022-1

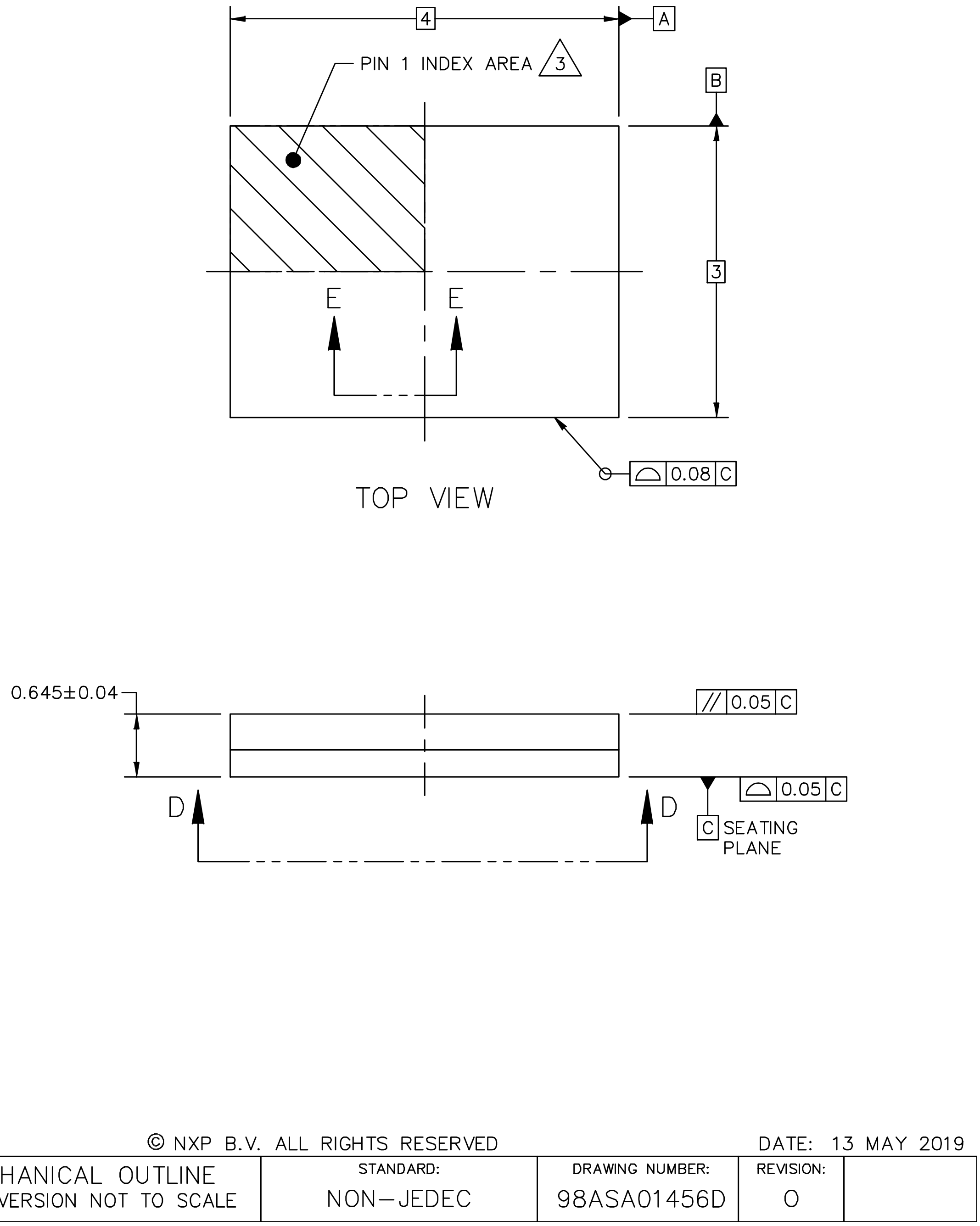
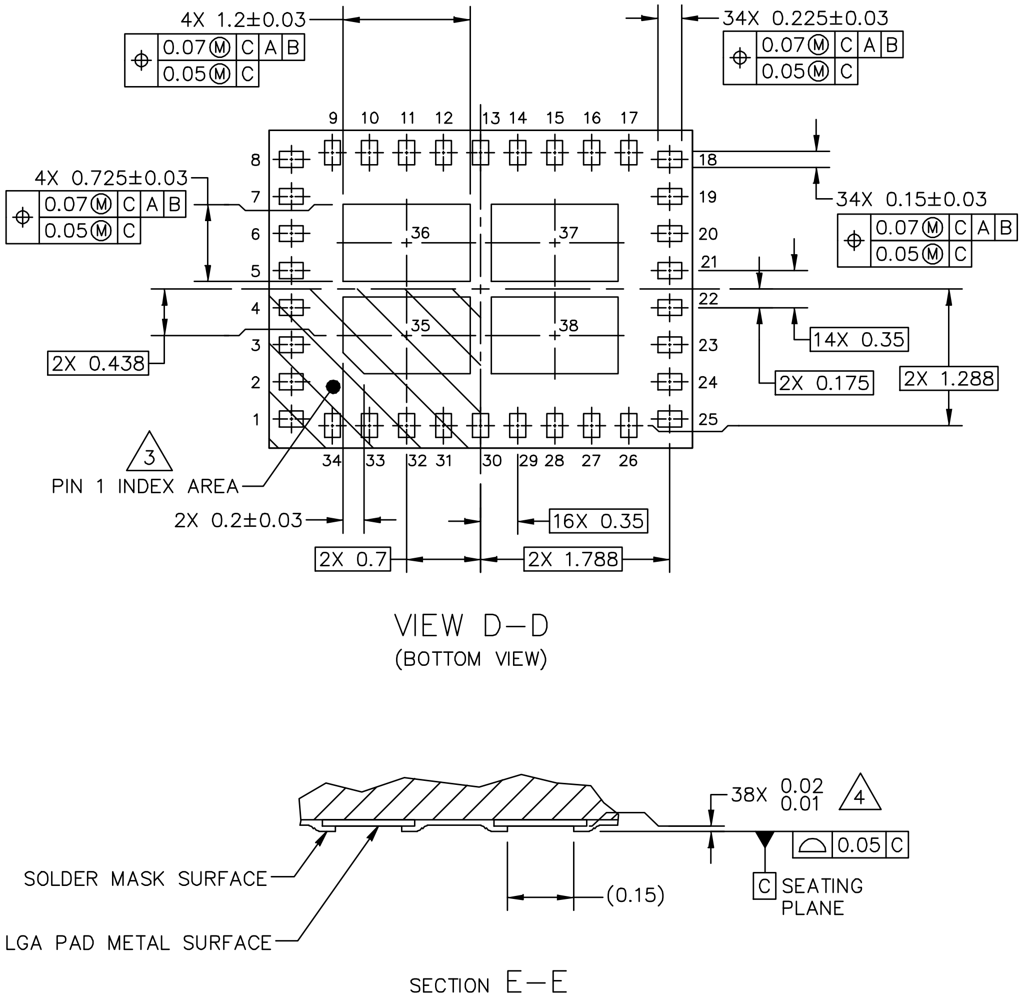


Figure 6. Top view



DATE: 13 MAY 2019

MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON–JEDEC	98ASA01456D	O	

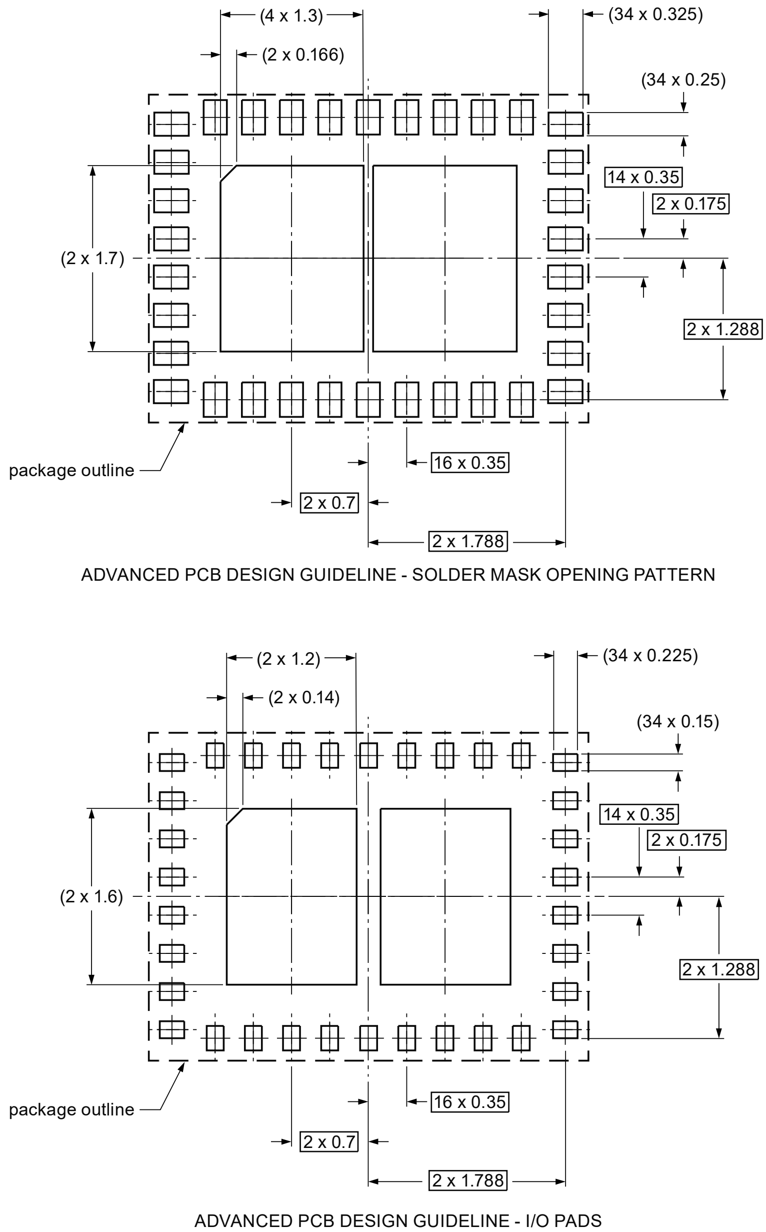
Figure 7. Bottom view

15.1 Advanced solder footprint

NXP recommends by default to apply the soldering and footprint guidelines as are released in POD SOT2022-1.

Advanced PCB design guideline may be used when SOT2022-1 is applied with a non wet-able flank design. However, care should be taken in the design of the stencil to ensure optimal solder deposition.

STANDARD PCB DESIGN GUIDELINE - SEE SOT2022-1 POD.
ADVANCED PCB DESIGN GUIDELINE:



THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL//SPECIFIC REQUIREMENTS
STENCIL TECHNOLOGY SHOULD BE OPTIMIZED FOR OPTIMUM SOLDER DEPOSITION.

aaa-035752

Figure 8. Advanced solder footprint

16 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

17 Abbreviations

Table 15. Abbreviations

Acronym	Description
ANT	antenna
BT	blue tooth
CDM	charge device model
CPLR	coupler
DC	direct current
ESD	electrostatic discharge
EVM	error vector magnitude
HBM	human body model
HFCPLGA	heat sink flip chip power land grid array
ISM	industrial scientific medical
ISL	isolation
LNA	low noise amplifier
LNAEN	low noise amplifier enable
LTE_LAA	LTE licensed assisted access
MCS	modulation code scheme
MIMO	multiple in multiple out
MSL	moisture sensitivity level
NF	noise figure
PA	power amplifier
PAEN	power amplifier enable
RF	radio frequency
RFFE	radio frequency front end
SEL	select
SPDT	single pole double throw
VSWR	voltage standing wave ratio
WLAN	wireless local area network

18 Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
WLAN8101H v.6	20200811	Product data sheet	-	WLAN8101H v.5
modification	• changed status from Company confidential to Public			
WLAN8101H v.5	20200721	Product data sheet	-	WLAN8101H v.4
modification	• changed status to Product data sheet			
WLAN8101H v.4	20200721	Preliminary data sheet	-	WLAN8101H v.3
modification	• changed Typical values on some characteristics • corrected value for BT inband spurious emission • adapted the condition for stability spurious levels on XT, and BT • adapted the footnotes on RX $IP3_i$, removed 10 MHz, and changed -20 dBm to -3 dBm • added BT to the Features and benefits bullet nr 4 • adjusted conditions on Switching time performance			
WLAN8101H v.3	20200330	Preliminary data sheet	-	WLAN8101H v.2.1
modification	• changed conditions of G_{flat} for ANT to RX from 80 MHz to 40 MHz			
WLAN8101H v.2.1	20200330	Preliminary data sheet	-	WLAN8101H v.2
modification	• Corrected typo in Limiting values MSC0 should be MCS0			
WLAN8101H v.2	20200316		-	WLAN8101H v.1
modification	• Changed name of CONTROL_4 to GND in the pinning diagram and pinning list and removed it from the Parallel interface control states table			
WLAN8101H v.1	20191219	Preliminary data sheet	-	-

19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 11 August 2020