WLAN8101C

5 GHz Wi-Fi 6 Front-End Module

Rev. 3 — 11 August 2020 Product data sheet

1 General description

The WLAN8101C is a 5 GHz 2 x 2 MIMO RFFE for Wi-Fi 6 applications in a 3 mm x 4 mm package.

The WLAN8101C includes two monolithic front-end ICs. Each front-end IC has an integrated power amplifier, a low noise amplifier with bypass functionality, and a single pole double throw (SPDT) switch.

WLAN8101C also includes coexistence filters for both transmit and receive channels.

The device is matched to 50 Ω and integrates harmonic and out of band filtering which minimizes the layout area in the application.

2 Features and benefits

- Small-size 2 x 2 MIMO RFFE module for WiFi 6 applications
- Integrated power amplifiers with multiple operation modes for dynamic power efficiency and linearity control
- Full high band 5.150 GHz to 5.925 GHz
- 3 TX operation modes enabling flexibility for power efficiency adaptation
- Integrated low-noise amplifiers supporting high gain and bypass modes
- Integrated SPDT switches for single antenna RX and TX operation
- Integrated directional couplers for precise transmit power control
- Requires no external matching components, DC free input/output ports
- Integrated RF decoupling capacitors for all V_{CC} and control pins
- Low profile, small-size 3 mm x 4 mm package
- Integrated ESD protection on all pins
  – Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001 exceeds 2 kV
  – Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002 exceeds 500 V

3 Applications

- Wi-Fi 6 support
- Smartphones, tablets, netbooks, and other portable computing devices
- Module applications for embedded systems

4 Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = -30 dBm for RX, P_i = -10 dBm for TX, f = 5.150 GHz to 5.925 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12711)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RF performance from ANT to RX						
I_{CC}	supply current	RX_gain	-	11.6	-	mA
		RX_bypass mode	-	7.5	-	µA
G_p	power gain	RX_gain	-	16	-	dB
		RX_bypass mode	-	-5.5	-	dB
NF	noise figure	RX_gain	-	2.5	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression point	RX_gain	-	-9	-	dBm
RL_i	input return loss	RX_gain mode, looking into ANT pin	-	10	-	dB
		RX_bypass mode, looking into ANT pin	-	9	-	dB
RL_o	output return loss	RX_gain mode, looking into RX pin	-	10	-	dB
		RX_bypass mode, looking into RX pin	-	10	-	dB
RF performance from TX to ANT						
I_{CC}	supply current	TX_gain1a (11ax compliant mode), 22dBm_11a, 6 Mbp/s spectral mask compliant	-	325	-	mA
G_p	power gain	TX_gain1a (11ax compliant, high-power mode)	-	30	-	dB
		TX_gain2a (11ax compliant, 3 dB back-off mode)	-	27.5	-	dB
		TX_gain3 (11ax compliant, low-power mode)	-	16	-	dB
G_{flat}	gain flatness	all TX modes, for any 80 MHz bandwidth	-	+/-0.25	-	dB
		all TX modes, for entire frequency range	-	+/-0.75	-	dB
EVM_{dyn}	dynamic error vector magnitude	11ax MCS10/11, TX_gain1a, 14 dBm, 180 µs burst, 50 % duty cycle, HE80	-	-44.5	-	dB
RL_i	input return loss	looking into TX pin	-	10	-	dB
RL_o	output return loss	looking into ANT pin	-	8	-	dB
High Isolation performance from ANT to RX						
I_{CC}	supply current	high isolation (default), dual channel	-	15	-	µA
$ISL_{(ANT-RX)}$	ANT-RX isolation	high isolation (default)	35	-	-	dB

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
WLAN8101C	WLAN8101C MP	HFCPLGA38	3 mm x 4 mm x 0.65 mm package, 0.35 mm pitch, 38 pins	SOT2022-1

6 Marking

Table 3. Marking

Type number	Marking code
WLAN8101C	8101C

7 Functional diagram

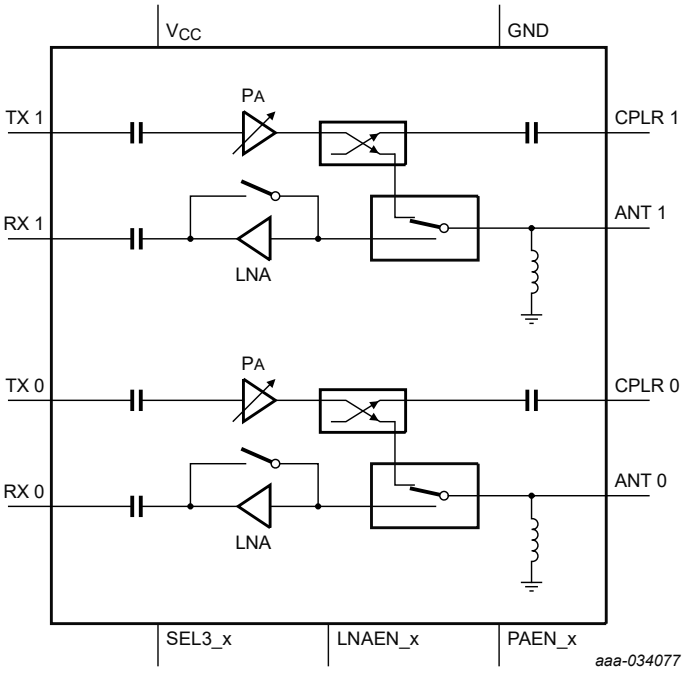
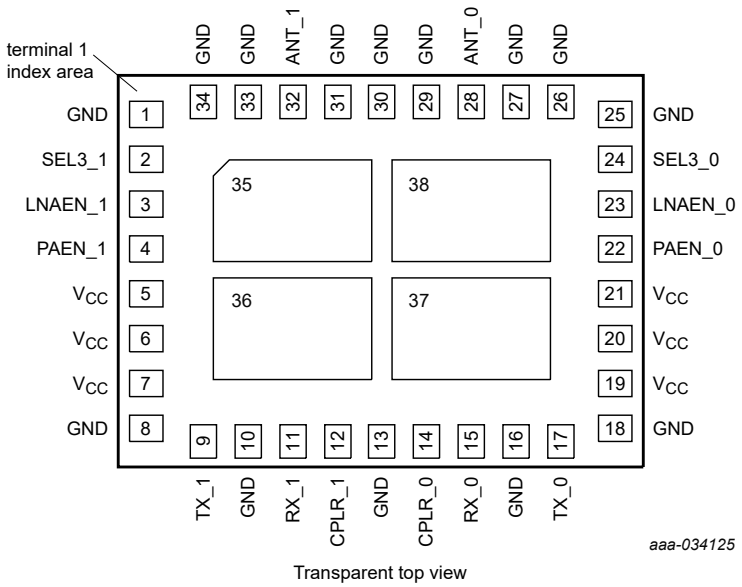


Figure 1. Functional diagram. The x at the control pins stands for port 0 and port1.

8 Pinning information

8.1 Pinning diagram



Transparent top view

Figure 2. Pin diagram

8.2 Pin description

Table 4. Pin description

Pin	Symbol	Description
1, 8, 10, 13, 16, 18, 25, 26, 27, 29, 30, 31, 33, 34, 35, 36, 37, and 38	GND	Ground
2	SEL3_1	select control
24	SEL3_0	select control
3	LNAEN_1	LNA enable
23	LNAEN_0	LNA enable
4	PAEN_1	PA enable
22	PAEN_0	PA enable
5, 6, 7, 19, 20 and 21	V_{CC}	supply voltage
9	TX_1	TX port
17	TX_0	TX port
11	RX_1	RX port
15	RX_0	RX port
12	CPLR_1	coupler port
14	CPLR_0	coupler port
28	ANT_0	antenna port
32	ANT_1	antenna port

9 Functional description

9.1 Parallel interface control states per MIMO channel

Table 5. Parallel interface control states per MIMO channel

Control pin SEL3_x, LNAEN_x, and PAEN_x contain internal pull-down resistors. The parallel interface table applies to both _0 and _1 control pins.[1]

SEL3_x	LNAEN_x	PAEN_x	Signal path	Operating mode	Mode description	LNA bias	PA bias
0	0	0	-	-	high isolation (default)	off	off
0	0	1	TX to ANT	TX_gain1a	high gain, high linearity, 11ax compliant	off	on
1	0	1	TX to ANT	TX_gain2a	high gain, high linearity, 3 dB back off, 11ax compliant	off	on
1	1	1	TX to ANT	TX_gain3	low gain, low power, 11ax compliant	off	on
1	1	0	-	-	reserved	-	-
1	0	0	-	-	reserved	-	-
0	1	0	ANT to RX	RX_gain	normal gain	on	off
0	1	1	ANT to RX	RX_bypass	bypass	off	off

[1] Binary represented logic levels, where 0 denotes a logic low ($V_i \leq V_{IL}$) and 1 denotes a logic high ($V_i \geq V_{IH}$)

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	-0.3	-	6	V
V_i	input voltage	applied to control pins SEL3_x, LNAEN_x, and PAEN_x, digital control signals for RX, TX, and isolation modes	-0.3	-	4.2	V
P_i	input power	on ANT pin, RX LNA mode, MCS0 signal applied	-	-	10	dBm
		on ANT pin, RX Bypass mode, MCS0 signal applied	-	-	18	dBm
		on TX pin, MCS0 signal applied	-	-	10	dBm
TX_RUG	TX ruggedness (no irreversible damage)	V_{CC} = 4.75 V, applied to TX_gain1a modes, P_o = 24 dBm_MCS0 under 50 Ω load condition. The required P_i level is kept constant during ruggedness test, VSWR all phases	-	-	10:1	-
T_{stg}	storage temperature		-55	-	125	°C
T_j	junction temperature		-	-	175	°C
T_{mb}	mounting base temperature		-	-	100	°C
V_{ESD}	Electrostatic Discharge Voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001	-	-	2	kV
		Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002	-	-	500	V

[1] Product withstands 30000 charger insert and pull-out events with a duration of 100 ms and a maximum supply voltage of 6 V

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{oper}	operating frequency		5.150	-	5.925	GHz
V_{CC}	supply voltage	on pin V_{CC} [1]	2.70	3.85	4.75	V
V_{IH}	HIGH-level input voltage		1.6	1.8	3.6	V
V_{IL}	LOW-level input voltage		0.0	-	0.4	V
T_{amb}	ambient temperature		-40	25	85	°C

[1] Product is functional with reduced performance at supply voltages from 2.5 V to 2.7 V.

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	junction to mounting base thermal resistance		-	25	-	K/W

13 Characteristics

13.1 Switching time performance

Table 9. Switching time performance

T_{amb} = 25 °C; V_{CC} = 3.85 V: All ports are terminated with 50 Ω, single channel performance. Unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{on(LNA)}$	LNA turn-on time	from 10 % to 90 % of LNA output level, bypass/LNA transition	-	170	-	ns
$t_{off(LNA)}$	LNA turn-off time	from 90 % to 10 % of LNA output level, bypass/LNA transition	-	230	-	ns
$t_{on(PA)}$	PA turn-on time	from 10 % to 90 % of PA output level, LNA/TX transition	-	250	-	ns
$t_{off(PA)}$	PA turn-off time	from 90 % to 10 % of PA output level, LNA/TX transition	-	250	-	ns

13.2 RF performance from ANT to RX

Table 10. RF performance from ANT to RX

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; P_i = -30 dBm, f = 5.150 GHz to 5.925 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12711)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	RX_gain	-	11.6	-	mA
		RX_bypass	-	7.5	-	µA
G_p	power gain	RX_gain	-	16	-	dB
		RX_bypass	-	-5.5	-	dB
G_{flat}	power gain flatness	RX_gain, peak-to-peak over any 80 MHz band	-	+/-0.25	-	dB
		RX_gain, over full RF bandwidth	-	+/-0.75	-	dB
		RX_bypass, peak-to-peak over any 80 MHz band	-	+/-0.25	-	dB
		RX_bypass, over full RF bandwidth	-	+/-0.75	-	dB
NF	noise figure	RX_gain	-	2.5	-	dB
RL_i	input return loss	RX_gain , looking into ANT pin	-	10	-	dB
		RX_bypass , looking into ANT pin	-	9	-	dB
RL_o	output return loss	RX_gain , looking into RX pin	-	10	-	dB
		RX_bypass , looking into RX pin	-	10	-	dB
$IP3_i$	input third order intercept point	RX_gain [1]	-	1.5	-	dBm
		RX_bypass [2]	-	27	-	dBm
$P_{i(1dB)}$	input power at 1 dB gain compression point	RX_gain	-	-9	-	dBm
		RX_bypass	-	14.0	-	dBm

[1] P_i = -20 dBm/tone, (20 MHz tone spacing)
[2] P_i = -3 dBm/tone, (20 MHz tone spacing)

13.3 RF performance from TX to ANT

Table 11. RF performance from TX to ANT

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; P_i = -30 dBm, f = 5.150 GHz to 5.925 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12711)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{CC}	supply current	TX_gain1a, no RF		-	190	-	mA
		TX_gain2a, no RF		-	145	-	mA
		TX_gain3, no RF		-	60	-	mA
		TX_gain1a, P_o = 17.5 dBm VHT80		-	245	-	mA
		TX_gain1a, P_o = 19 dBm 11n MCS7 HT20		-	265	-	mA
		TX_gain1a, P_o = 22 dBm 11a OFDM6, 20 MHz		-	325	-	mA
		TX_gain2a, P_o = 14.5 dBm, VHT80		-	190	-	mA
		TX_gain2a, P_o = 16 dBm, 11n MCS7 HT20		-	205	-	mA
		TX_gain2a, P_o = 19 dBm, 11a OFDM6, 20 MHz		-	245	-	mA
		TX_gain3, P_o = 4 dBm, 11ax MCS10/11 HE80		-	65	-	mA
G_p	power gain	TX_gain1a mode		-	30	-	dB
		TX_gain2a mode		-	27.5	-	dB
		TX_gain3 mode		-	16	-	dB
G_{flat}	gain flatness	all TX modes, for any 80 MHz bandwidth		-	+/-0.25	-	dB
		all TX modes, for entire frequency range		-	+/-0.75	-	dB
RL_i	input return loss	all TX modes, looking into TX pin		-	10	-	dB
RL_o	output return loss	all TX modes, looking into ANT pin		-	8	-	dB
$ISL_{(ANT-RX)}$	ANT-RX isolation	all TX modes, measured between ANT, and RX pins, measured on the same channel		33	-	-	dB
SEM margin	margin to spectrum emission mask	11a, OFDM6, 20 MHz					
		TX_gain1a, P_o = 22 dBm		-	3.5	-	dB
		11n, MCS0, 20 MHz					
		TX_gain1a, P_o = 21 dBm		-	3	-	dB
EVM_{dyn}	dynamic error vector magnitude	11a, OFDM6, 20 MHz, 180 µs burst, 50 % duty cycle					
		TX_gain1a, P_o = 22 dBm		-	-20	-	dB
		TX_gain2a, P_o = 19 dBm		-	-20	-	dB
		11n, MCS0, 20 MHz, 180 µs burst, 50 % duty cycle					
		TX_gain1a, P_o = 20.5 dBm		-	-26	-	dB
		TX_gain2a, P_o = 17.5 dBm		-	-26	-	dB
		11a, OFDM54, 20 MHz, 180 µs burst, 50 % duty cycle					
		TX_gain1a, P_o = 19.5 dBm		-	-32	-	dB
		TX_gain2a, P_o = 16.5 dBm		-	-32	-	dB

Table 11. RF performance from TX to ANT*...continued*

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; P_i = -30 dBm, f = 5.150 GHz to 5.925 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12711)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		11n, MCS7, HT20, 180 µs burst, 50 % duty cycle					
		TX_gain1a, P_o = 18.5 dBm		-	-34	-	dB
		TX_gain2a, P_o = 15.5 dBm		-	-34	-	dB
		11ac, MCS9, VHT80, 180 µs burst, 50 % duty cycle					
		TX_gain1a, P_o = 17 dBm		-	-40	-	dB
		TX_gain2a, P_o = 14 dBm		-	-40	-	dB
		11ax, MCS10/11, HE80,180 µs burst, 50 % duty cycle					
		TX_gain1a, P_o = 16 dBm		-	-43	-	dB
		TX_gain1a, P_o = 14 dBm		-	-44.5	-	dB
		TX_gain2a, P_o = 13 dBm		-	-43.5	-	dB
		TX_gain2a, P_o = 11 dBm		-	-44.5	-	dB
		TX_gain3, P_o = 4.0 dBm		-	-44	-	dB
α2H	second harmonic emission level	11a, OFDM6					
		TX_gain1a, P_o = 22 dBm		-	-23	-	dBm/MHz
α3H	third harmonic emission level	11a, OFDM6					
		TX_gain1a, P_o = 22 dBm		-	-21	-	dBm/MHz

13.4 High isolation performance from ANT to RX

Table 12. High isolation performance from ANT to RX

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; P_i = -30 dBm, f = 5.150 GHz to 5.925 GHz. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the application schematic. (See application note AN12711)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	high isolation (default), dual channel	-	15	-	µA
$ISL_{(ANT-RX)}$	ANT-RX isolation	high isolation (default)	35	-	-	dB

13.5 Directional coupler

Table 13. Power coupler RF Performance

T_{amb} = 25 °C; V_{CC} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; P_i = -30 dBm, f = 5.150 GHz to 5.925 GHz, single channel performance. Unless otherwise specified. All values are measured at product input/output as reference plane.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{cpl}	coupling ratio	measured in Ch-0,TX_gain1a, and TX_gain2a modes, f = 5.540 GHz	-	23.5	-	dB
		measured in Ch-1,TX_gain1a, and TX_gain2a modes, f = 5.540 GHz	-	24.5	-	dB
$\Delta R_{cpl(f)}$	variation of coupling ratio over frequency	positive slope versus frequency, f = 5.150 GHz to 5.925 GHz	-	+/-0.7	-	dB
D	directivity	measured in all TX modes	-	14	-	dB
$RL_{i(CPLR)}$	coupler input return loss	looking into CPLR pin	-	10	-	dB

14 Graphics

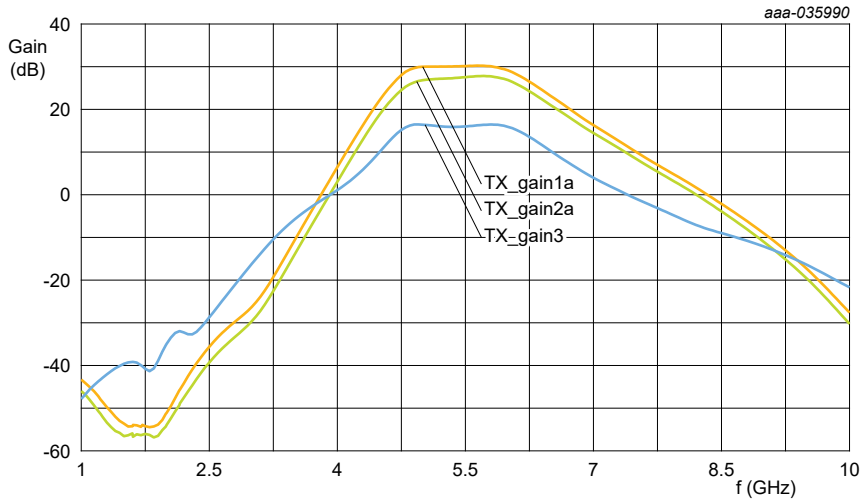


Figure 3. Typical TX transfer function

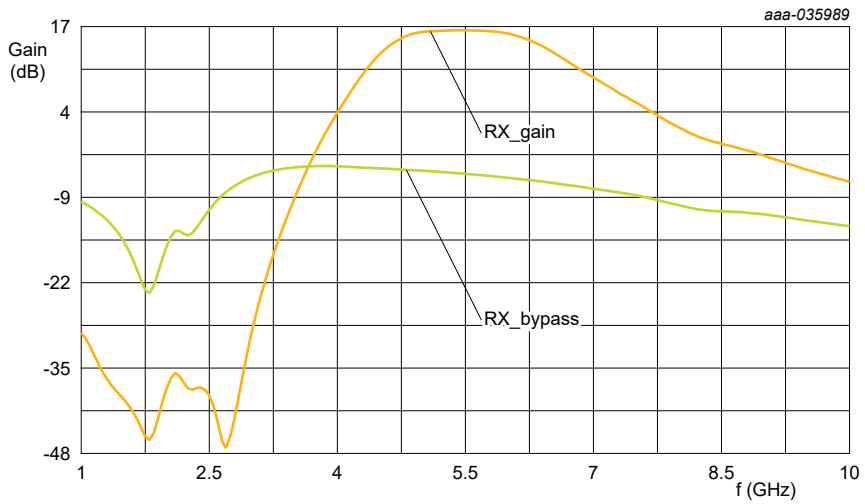
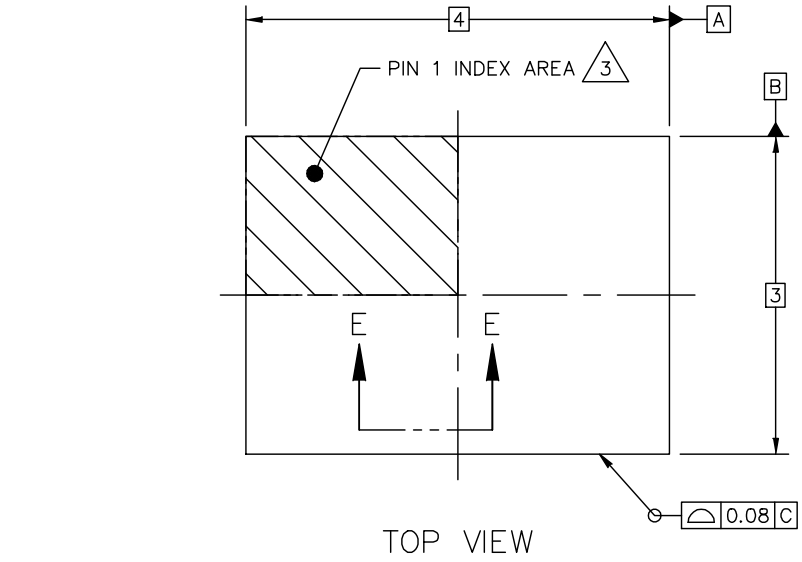


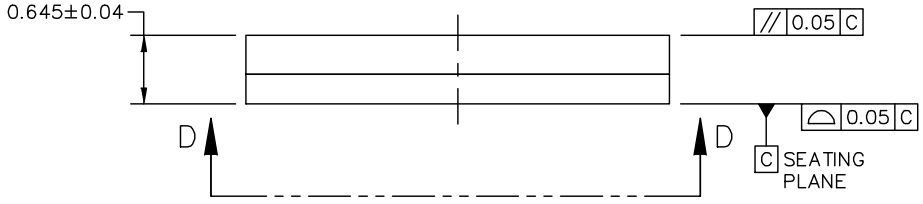
Figure 4. Typical RX transfer function

15 Application information

16 Package outline

Table 14. Package outline SOT2022-1





DATE: 13 MAY 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01456D	REVISION: 0	

Figure 5. Top view

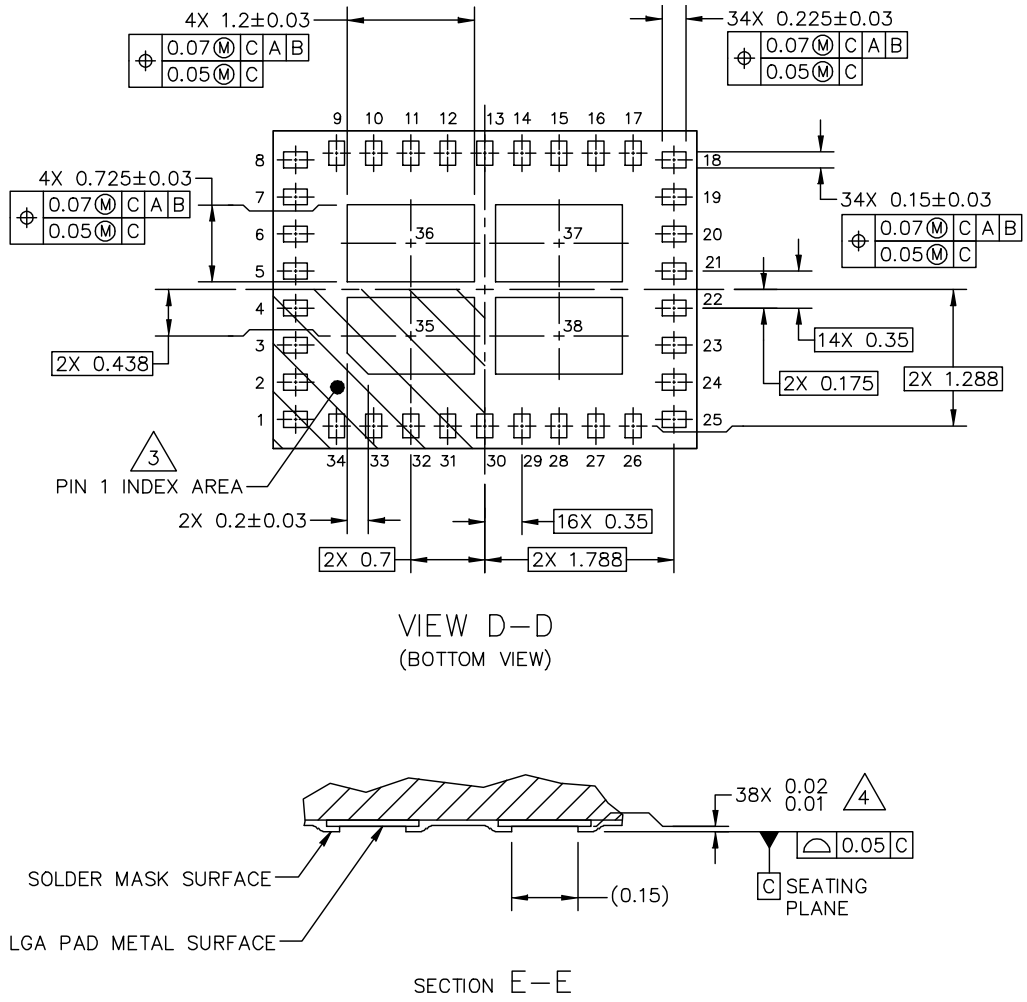


Figure 6. Bottom view

16.1 Advanced solder footprint

NXP recommends by default to apply the soldering and footprint guidelines as are released in POD SOT2022-1.

Advanced PCB design guideline may be used when SOT2022-1 is applied with a non wet-able flank design. However, care should be taken in the design of the stencil to ensure optimal solder deposition.

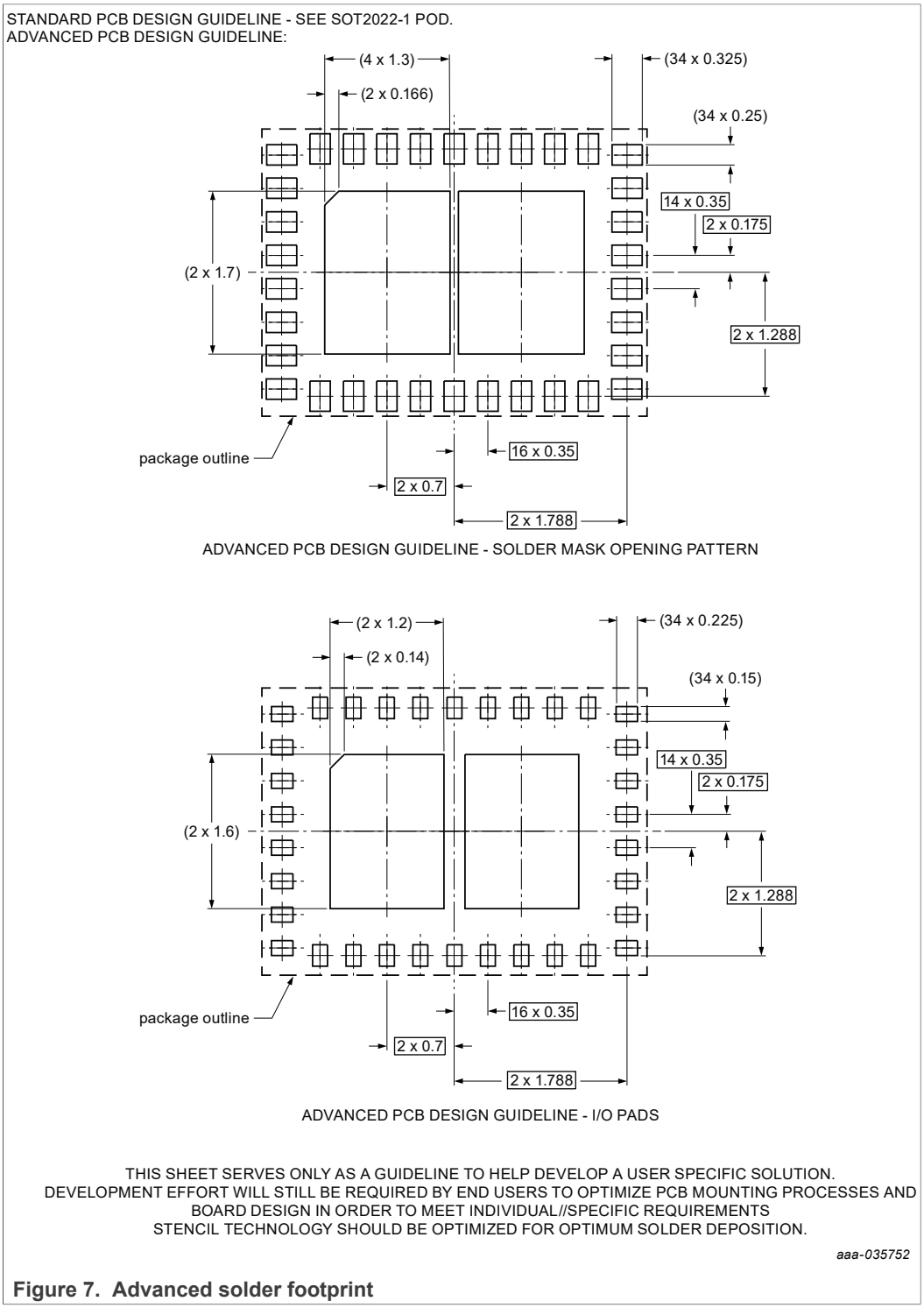


Figure 7. Advanced solder footprint

17 Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

18 Abbreviations

Table 15. Abbreviations

Acronym	Description
ANT	antenna
CDM	charge device model
CPLR	coupler
DC	direct current
ESD	electrostatic discharge
EVM	error vector magnitude
HBM	human body model
HFCPLGA	heat sink flip chip power land grid array
ISM	industrial scientific medical
ISL	isolation
LNA	low noise amplifier
LNAEN	low noise amplifier enable
MCS	modulation code scheme
MIMO	multiple in multiple out
MSL	moisture sensitivity level
NF	noise figure
PA	power amplifier
PAEN	power amplifier enable
RF	radio frequency
RFFE	radio frequency front end
RoHS	restriction of hazardous substances
SEL	select
SPDT	single pole double throw
VSWR	voltage standing wave ratio
WLAN	wireless local area network

19 Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
WLAN8101C v.3	20200811	Product data sheet	-	WLAN8101C v.2
modification	• changed status from Company confidential to Public			
WLAN8101C v.2	20200724	Product data sheet	-	WLAN8101C v.1
modification	• updated the ESD condition on CDM with the correct description of the used ESD standard • adapted the footnotes on RX $IP3_i$, removed 10 MHz, and changed -20 dBm to -3 dBm • changed status to Product data sheet			
WLAN8101C v.1	20191219	Preliminary data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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