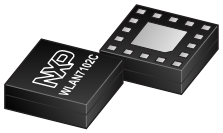


aaa-035577

WLAN7102C

5 GHz Wi-Fi 6 Front-End IC

Rev. 4 — 15 September 2020 **Product data sheet**

1 General description

The WLAN7102C is a WLAN 5 GHz RF front-end IC in a 2 mm x 2 mm HWFLGA16 package.

The WLAN7102C is designed for Wi-Fi 6 applications. It includes a power amplifier with logarithmic power detector, a low noise receive amplifier (LNA) and a single pole double throw (SPDT) switch. The WLAN7102C also includes coexistence filters for both transmit and receive channels.

The device is matched to 50 Ω and integrates harmonic and out of band filtering which minimizes the layout area in the application.

2 Features and benefits

- Fully integrated Wi-Fi 6 RF front-end IC with high linearity and low-power modes
- EVM_{dyn} = -43 dB, 802.11ax MCS 10/11 HE80, P_o = 14 dBm
- Full high band 5150 MHz to 5925 MHz
- High-power efficiency
- Requires no external matching components, DC free input/output ports
- 3 TX operation modes enabling flexibility for power efficiency adaptation
- 2 RX operation modes enabling large gain step between LNA mode and Bypass mode
- Integrated logarithmic power detector
- ESD protection on all pins
  - Human Body Model (HBM) according to ANSI/ ESDA/JEDEC standard JS-001 exceeds 2 kV
  - Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002 exceeds 500 V
- Integrated RF decoupling capacitors for all V_{CC} and control pins

3 Applications

- Wi-Fi 6 support
- Smartphones, tablets, netbooks, and other portable computing devices
- Module applications for embedded systems

4 Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C; V_{CC1} = V_{CC2} = V_{CC3} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; Z_s = Z_L = 50 Ω; P_i = - 30 dBm for RX, P_i = -10 dBm for TX, f = 5150 MHz to 5925 MHz. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the schematic in Figure 5 and the components listed in Table 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RF performance from ANT to RX						
I_{CC}	supply current	RX_gain	-	11.5	-	mA
		RX_bypass mode	-	7.5	-	µA
G_p	power gain	RX_gain	-	16.2	-	dB
		RX_bypass mode	-	-5.4	-	dB
NF	noise figure	RX_gain	-	2.5	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression point	RX_gain	-	-9	-	dBm
RL_{in}	input return loss	RX_gain mode, return loss looking into ANT pin	-	9	-	dB
		RX_bypass mode, return loss looking into ANT pin	-	7.5	-	dB
RL_{out}	output return loss	RX_gain mode, return loss looking into RX pin	-	8.5	-	dB
		RX_bypass mode, return loss looking into RX pin	-	10	-	dB
RF performance from TX to ANT						
I_{CC}	supply current	TX_gain1a (11ax compliant mode), 22dBm_11a, 6 Mbp/s spectral mask compliant	-	335	-	mA
G_p	power gain	TX_gain1a (11ax compliant, high-power mode)	-	30.5	-	dB
		TX_gain2a (11ax compliant, 3 dB back-off mode)	-	27.5	-	dB
		TX_gain3 (11ax compliant, low-power mode)	-	16.5	-	dB
G_{flat}	gain flatness	all TX modes, for any 80 MHz bandwidth	-	+/-0.25	-	dB
		all TX modes, for entire frequency range	-	+/-0.75	-	dB
EVM_{dyn}	dynamic error vector magnitude	11ax MCS10/11 HE80, TX_gain1a, P_o = 14 dBm, 180 µs burst, 50 % duty cycle	-	-43	-	dB
RL_{in}	input return loss	return loss looking into TX pin	-	10	-	dB
RL_{out}	output return loss	return loss looking into ANT pin	-	8	-	dB
High Isolation performance from ANT to RX						
I_{CC}	supply current	high isolation (default)	-	7.5	-	µA
$ISL_{(ANT-RX)}$	ANT-RX isolation	high isolation (default)	35	-	-	dB

5 Ordering information

Table 2. Ordering information

Type number	Orderable part number	Package		
		Name	Description	Version
WLAN7102C	WLAN7102CZ	HWFLGA16	plastic, thermal enhanced ultra thin profile land grid array package; no leads; 16 terminals	SOT2013-2

6 Marking info

Table 3. Marking info

Type number	Marking
WLAN7102C	102

7 Functional diagram

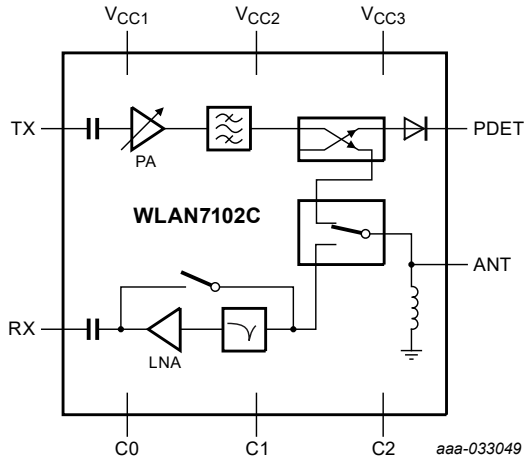
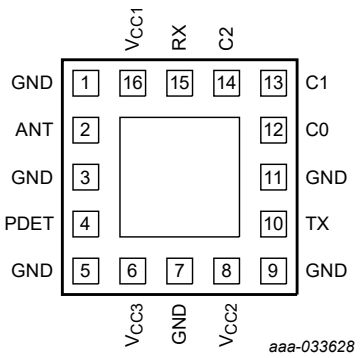


Figure 1. Functional diagram

8 Pinning information

8.1 Pinning diagram



transparent top view

Figure 2. Pin diagram

8.2 Pin description

Table 4. Pin description

Pin	Symbol	Description
1,3,5,7,9, and11	GND	ground
12	CO	control pin
13	C1	control pin
14	C2	control pin
15	RX	RX port
6	V_{CC3}	supply voltage
8	V_{CC2}	supply voltage
16	V_{CC1}	supply voltage
2	ANT	antenna port
4	PDET	power detector
10	TX	TX port

9 Functional description

9.1 Parallel interface control states

Table 5. Parallel interface control states

Control pin C0, C1, and C2 containing internal pull-down resistors.[1]

C2	C1	C0	Signal path	Operating mode	Mode description	LNA bias	PA bias
0	0	0	-	-	high isolation (default)	off	off
0	0	1	TX to ANT	TX_gain1a	high gain, high linearity, 11ax compliant	off	on
1	0	1	TX to ANT	TX_gain2a	high gain, high linearity, 3 dB back off, 11ax compliant	off	on
1	1	1	TX to ANT	TX_gain3	low gain, low power, 11ax compliant	off	on
1	1	0	-	-	reserved	-	-
1	0	0	-	-	reserved	-	-
0	1	0	ANT to RX	RX_gain	normal gain	on	off
0	1	1	ANT to RX	RX_bypass	bypass	off	off

[1] Binary represented logic levels, where 0 denotes a logic low ($V_i \leq V_{IL}$) and 1 denotes a logic high ($V_i \geq V_{IH}$)

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	6 V max 200 ms	-0.3	-	6	V
V_i	input voltage	applied to control pins C0, C1 and C2, digital control signals for RX, TX, and isolation modes	-0.3	-	4.2	V
P_i	input power	on ANT pin, RX LNA mode, MCS7 signal applied	-	-	10	dBm
		on ANT pin, RX Bypass mode, MCS0 signal applied	-	-	20	dBm
		on TX pin, MCS7 signal applied	-	-	10	dBm
		on TX pin, PA off, CW signal applied	-	-	15	dBm
TX_RUG	TX ruggedness (no irreversible damage)	V_{CC}: 3.2 V to 4.8 V, applied to TX_gain1a, and 1b modes, P_o = 24 dBm, MCS0 under 50 Ω load condition. The required P_i level is kept constant during ruggedness test, VSWR all phases	-	-	10:1	-
T_{stg}	storage temperature		-55	-	125	°C
T_j	junction temperature		-	-	175	°C
T_{mb}	mounting base temperature		-	-	100	°C
V_{ESD}	Electrostatic Discharge Voltage	Human Body Model (HBM) according to ANSI/ESDA/JEDEC standard JS-001	-	-	2	kV
		Charged Device Model (CDM) according to ANSI/ESDA/JEDEC standard JS-002	-	-	500	V

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{oper}	operating frequency		5150	-	5925	MHz
V_{CC}	supply voltage	on pin V_{CC1}, V_{CC2}, V_{CC3} [1]	3.2	3.85	4.8	V
V_{IH}	HIGH-level input voltage		1.6	1.8	3.6	V
V_{IL}	LOW-level input voltage		0.0	-	0.4	V
T_{amb}	ambient temperature		-40	25	85	°C

[1] Product is functional with reduced performance at supply voltages from 2.5 V to 3.2 V.

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	junction to mounting base thermal resistance		-	45	-	K/W

13 Characteristics

13.1 Switching time performance

Table 9. Switching time performance

T_{amb} = 25 °C; V_{CC1} = V_{CC2} = V_{CC3} = 3.85 V: All ports are terminated with 50 Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{on(LNA)}$	LNA turn-on time	from 10 % to 90 % of LNA output level, bypass/LNA transition	-	170	500	ns
$t_{off(LNA)}$	LNA turn-off time	from 90 % to 10 % of LNA output level, bypass/LNA transition	-	230	500	ns
$t_{on(PA)}$	PA turn-on time	from 10 % to 90 % of PA output level, LNA/TX transition	-	250	500	ns
$t_{off(PA)}$	PA turn-off time	From 90 % to 10 % of PA output level, LNA/TX transition	-	250	500	ns

13.2 RF performance from ANT to RX

Table 10. RF performance from ANT to RX

T_{amb} = 25 °C; V_{CC1} = V_{CC2} = V_{CC3} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; P_i = -30 dBm, f = 5150 MHz to 5925 MHz. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the schematic in Figure 5 and the components listed in Table 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	RX_gain	-	11.5	13.5	mA
		RX_gain, T_{amb} = -20 °C to 85 °C	-	-	14.5	mA
		RX_bypass	-	7.5	12	µA
		RX_bypass, T_{amb} = -20 °C to 85 °C, V_{CC} = 4.8 V	-	7.5	16	µA
G_p	power gain	RX_gain	13.4	16.2	18.8	dB
		RX_bypass	-7.9	-5.4	-2.4	dB
G_{flat}	power gain flatness	RX_gain, peak-to-peak over any 80 MHz band	-	+/-0.25	-	dB
		RX_gain, over full RF bandwidth	-	+/-0.75	-	dB
		RX_bypass, peak-to-peak over any 80 MHz band	-	+/-0.25	-	dB
		RX_bypass, over full RF bandwidth	-	+/-0.75	-	dB
NF	noise figure	RX_gain	-	2.5	2.8	dB
RL_{in}	input return loss	RX_gain mode, return loss looking into ANT pin	6.5	9	-	dB
		RX_bypass mode, return loss looking into ANT pin	5.5	7.5	-	dB
RL_{out}	output return loss	RX_gain mode, return loss looking into RX pin	7	8.5	-	dB
		RX_bypass mode, return loss looking into RX pin	8	10	-	dB
$IP3_i$	input third intercept point	RX_gain [1]	-	2.5	-	dBm
		RX_bypass [1]	-	20.5	-	dBm
$P_{i(1dB)}$	input power at 1 dB gain compression point	RX_gain	-10.5	-9	-	dBm
		RX_bypass	11.5	14	-	dBm

[1] P_i = -20 dBm/tone, (10 MHz to 20 MHz tone spacing)

13.3 RF performance from TX to ANT

Table 11. RF performance from TX to ANT

T_{amb} = 25 °C; V_{CC1} = V_{CC2} = V_{CC3} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; P_i = -10 dBm, f = 5150 MHz to 5925 MHz. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the schematic in Figure 5 and the components listed in Table 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	TX_gain1a, no RF	-	190	214	mA
		TX_gain1a, no RF, T_{amb} = -20 °C to 85 °C	-	-	227	mA
		TX_gain2a, no RF	-	145	160	mA
		TX_gain2a, no RF, T_{amb} = -20 °C to 85 °C	-	-	170	mA
		TX_gain3, no RF	-	57	67	mA
		TX_gain3, no RF, T_{amb} = -20 °C to 85 °C	-	-	74	mA
		TX_gain1a, P_o = 16 dBm, 11ax MCS10/11 HE80	-	230	250	mA
		TX_gain1a, P_o = 17.5 dBm, 11ac MCS9 VHT80	-	250	270	mA
		TX_gain1a, P_o = 19 dBm, 11n MCS7 HT20	-	270	293	mA
		TX_gain1a, P_o = 22 dBm, 11a OFDM6, 20 MHz	-	339	367	mA
		TX_gain1a, P_o = 22 dBm, 11a OFDM6, 20 MHz, T_{amb} = -20 °C to 85 °C	-	-	382	mA
		TX_gain2a, P_o = 13 dBm, 11ac MCS9 VHT80	-	170	185	mA
		TX_gain2a, P_o = 16 dBm, 11n MCS7 HT20	-	200	218	mA
		TX_gain3, P_o = 4 dBm, 11ax MCS10/11 HE80	-	62	71	mA
		TX_gain3, P_o = 4 dBm, 11ax MCS10/11 HE80, T_{amb} = -20 °C to 85 °C	-	-	75	mA
G_p	power gain	TX_gain1a mode	27.5	30.5	33.5	dB
		TX_gain1a mode, T_{amb} = -20 °C to 85 °C	25.5	-	35	dB
		TX_gain2a mode	25	27.5	30	dB
		TX_gain2a mode, T_{amb} = -20 °C to 85 °C	23	-	31.5	dB
		TX_gain3 mode	14.5	16.5	18.5	dB
		TX_gain3 mode, T_{amb} = -20 °C to 85 °C	13.5	-	19.5	dB
G_{flat}	gain flatness	all TX modes, for any 80 MHz bandwidth	-	+/-0.25	-	dB
		all TX modes, for entire frequency range	-	+/-0.75	-	dB
RL_{in}	input return loss	all TX modes, return loss looking into TX pin	8	10	-	dB
RL_{out}	output return loss	all TX modes, return loss looking into ANT pin	6	8	-	dB
$ISL_{(ANT-RX)}$	ANT-RX isolation	all TX modes, measured between ANT, and RX pins	33	-	-	dB
SEM margin	margin to spectrum emission mask	11a OFDM6, 20 MHz				
		TX_gain1a, P_o = 22 dBm	1	3.5	-	dB
		11n MCS0, 20 MHz				
		TX_gain1a, P_o = 21 dBm	1	3	-	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EVM_{dyn}	dynamic error vector magnitude	11a OFDM6, 20 MHz, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 22 dBm	-	-20	-18	dB
		TX_gain1a, P_o = 22 dBm, T_{amb} = -20 °C to 85 °C	-	-	-16.5	dB
		11n MCS0, 20 MHz, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 20.6 dBm	-	-25	-23	dB
		TX_gain1a, P_o = 20.6 dBm, T_{amb} = -20 °C to 85 °C	-	-	-20.5	dB
		11a OFDM54, 20 MHz, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 19.5 dBm	-	-31	-29	dB
		TX_gain1a, P_o = 19 dBm, T_{amb} = -20 °C to 85 °C	-	-	-26	dB
		11n MCS7 HT20, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 18.5 dBm	-	-36	-33.5	dB
		TX_gain1a, P_o = 18.5 dBm, T_{amb} = -20 °C to 85 °C	-	-	-28	dB
		TX_gain2a, P_o = 15.5 dBm	-	-33	-28.5	dB
		TX_gain2a, P_o = 15.5 dBm, T_{amb} = -20 °C to 85 °C	-	-	-27	dB
		11n MCS7 HT40, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 18.5 dBm	-	-36	-33.5	dB
		TX_gain2a, P_o = 15.5 dBm	-	-33	-28.5	dB
		11ac MCS9 VHT80, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 17 dBm	-	-40	-36.5	dB
		TX_gain1a, P_o = 17 dBm, T_{amb} = -20 °C to 85 °C	-	-	-33	dB
		TX_gain2a, P_o = 14 dBm	-	-39	-35	dB
		TX_gain2a, P_o = 14 dBm, T_{amb} = -20 °C to 85 °C	-	-	-32	dB
		11ac MCS9 VHT160, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 17 dBm	-	-38	-34.5	dB
		11ax MCS10/11 HE80, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 16 dBm	-	-42.5	-38.5	dB
		TX_gain1a, P_o = 16 dBm, T_{amb} = -20 °C to 85 °C	-	-	-35.5	dB
		TX_gain1a, P_o = 14 dBm	-	-43	-39	dB
		TX_gain1a, P_o = 14 dBm, T_{amb} = -20 °C to 85 °C	-	-	-36.5	dB
		TX_gain2a, P_o = 11 dBm	-	-42.5	-38	dB
		TX_gain2a, P_o = 11 dBm, T_{amb} = -20 °C to 85 °C	-	-	-36.5	dB
		TX_gain3, P_o = 4 dBm	-	-44	-40.5	dB
		TX_gain3, P_o = 4 dBm, T_{amb} = -20 °C to 85 °C	-	-	-39.5	dB
		11ax MCS10/11 HE160, 180 µs, 50 % duty cycle				
		TX_gain1a, P_o = 13 dBm	-	-42.5	-38.5	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α2H	second harmonic emission level	11a OFDM6				
		TX_gain1a, P_o = 22 dBm	-	-23	-18.5	dBm/MHz
α3H	third harmonic emission level	11a OFDM6				
		TX_gain1a, P_o = 22 dBm	-	-21	-17	dBm/MHz

13.4 High isolation performance from ANT to RX

Table 12. High isolation performance from ANT to RX

T_{amb} = 25 °C; V_{CC1} = V_{CC2} = V_{CC3} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; f = 5150 MHz to 5925 MHz. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the schematic in Figure 5 and the components listed in Table 14.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	high isolation (default)	-	7.5	-	μA
$ISL_{(ANT-RX)}$	ANT-RX isolation	high isolation (default)	35	-	-	dB

13.5 Power detector

Table 13. Power detector performance

T_{amb} = 25 °C; V_{CC1} = V_{CC2} = V_{CC3} = 3.85 V; V_{IH} = 1.8 V; V_{IL} = 0 V; All ports are terminated with 50 Ω; f = 5150 MHz to 5925 MHz. Unless otherwise specified. All values are measured at product input/output as reference plane. Measurements are done using the schematic in Figure 5 and the components listed in Table 14.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{det}	detected voltage	P_o = 0 dBm, f = 5400 MHz	[1]	180	290	340	mV
		P_o = 22 dBm f = 5400 MHz	[1]	760	935	1050	mV
$V_{det(flat)}$	detected voltage flatness across the band	P_o = 0 dBm to 22 dBm		-	-	1.5	dB

[1] Measured at the peak of the preamble of the OFDM signal, 11a 6 Mbp/s applied

14 Graphics

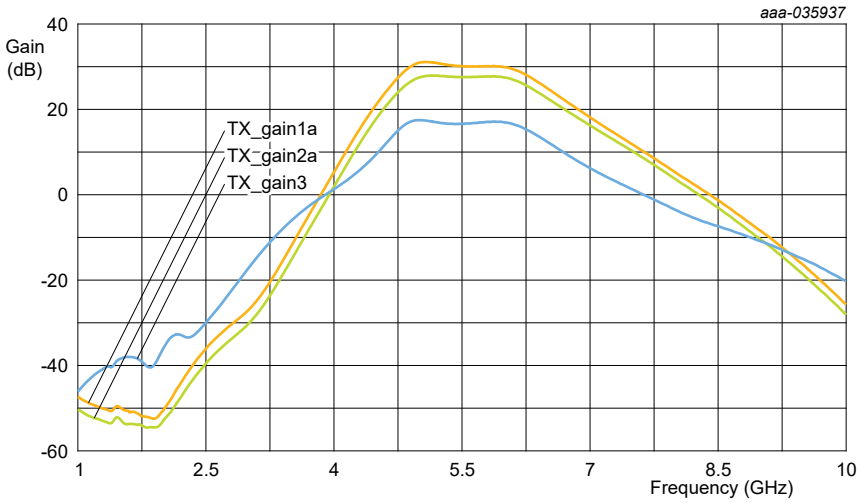


Figure 3. Typical TX transfer function

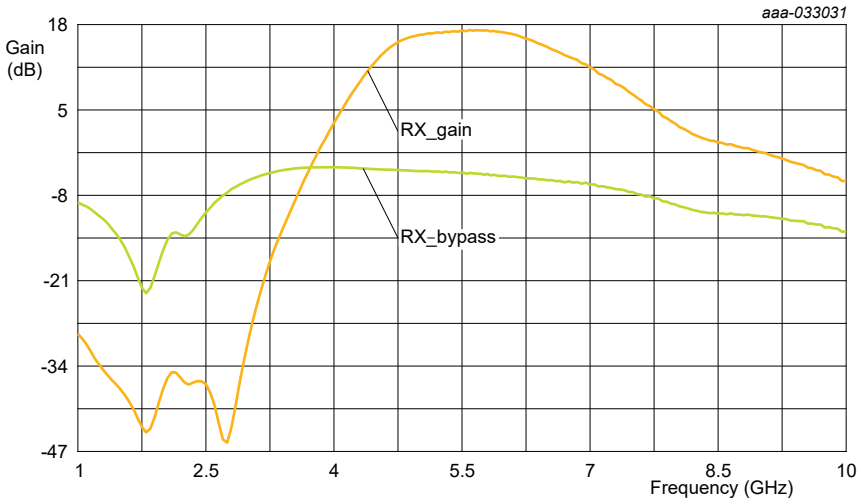


Figure 4. Typical RX transfer function

15 Application information

Application schematic shows a typical application for WLAN7102C. TX output stage can draw 250 mA of total output stage current from Vcc3. Each of RF pins except the antenna port has an internal DC-cut capacitor and tuned to 50 Ohm termination impedance. There is no need for any external DC-cut or matching component in a 50 ohm-to-50 ohm application. All the supply pins are RF decoupled internally, so one capacitor (100 nF) per supply pin is sufficient for WLAN envelope-content filtering in a typical application. Nevertheless, as for precaution, a 6.8 pF RF decoupling capacitor close to Vcc1 pin can improve the supply immunity of WLAN7102C in the final application. A large capacitor (Ce) performs a low frequency filtering (for supply noise or jitter). Control pins (C0, C1, C2) are also RF decoupled internally, so there is no need for external decoupling use, as long as the control lines are not polluted by any aggressor devices in the application.

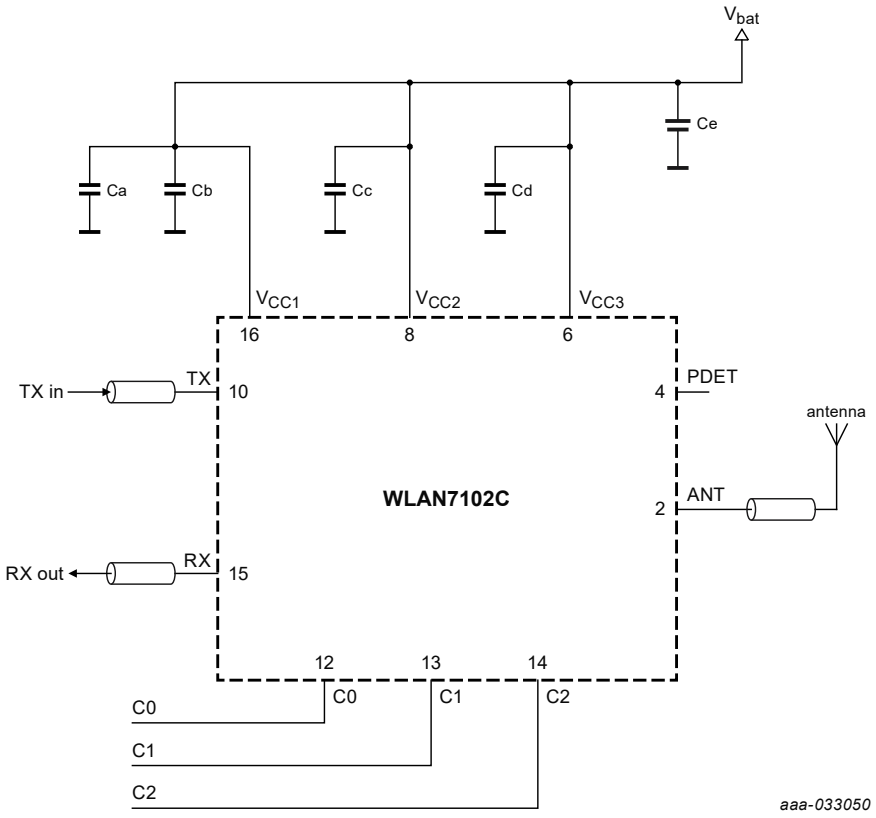


Figure 5. Application schematic

Table 14. List of components

Component	Description	Value	Amount	Remarks
Ca, Cc, Cd.	capacitor	100 nF	3	
Cb	capacitor	6.8 pF	1	
Ce	capacitor	≥ 10 µF	1	

16 Package outline

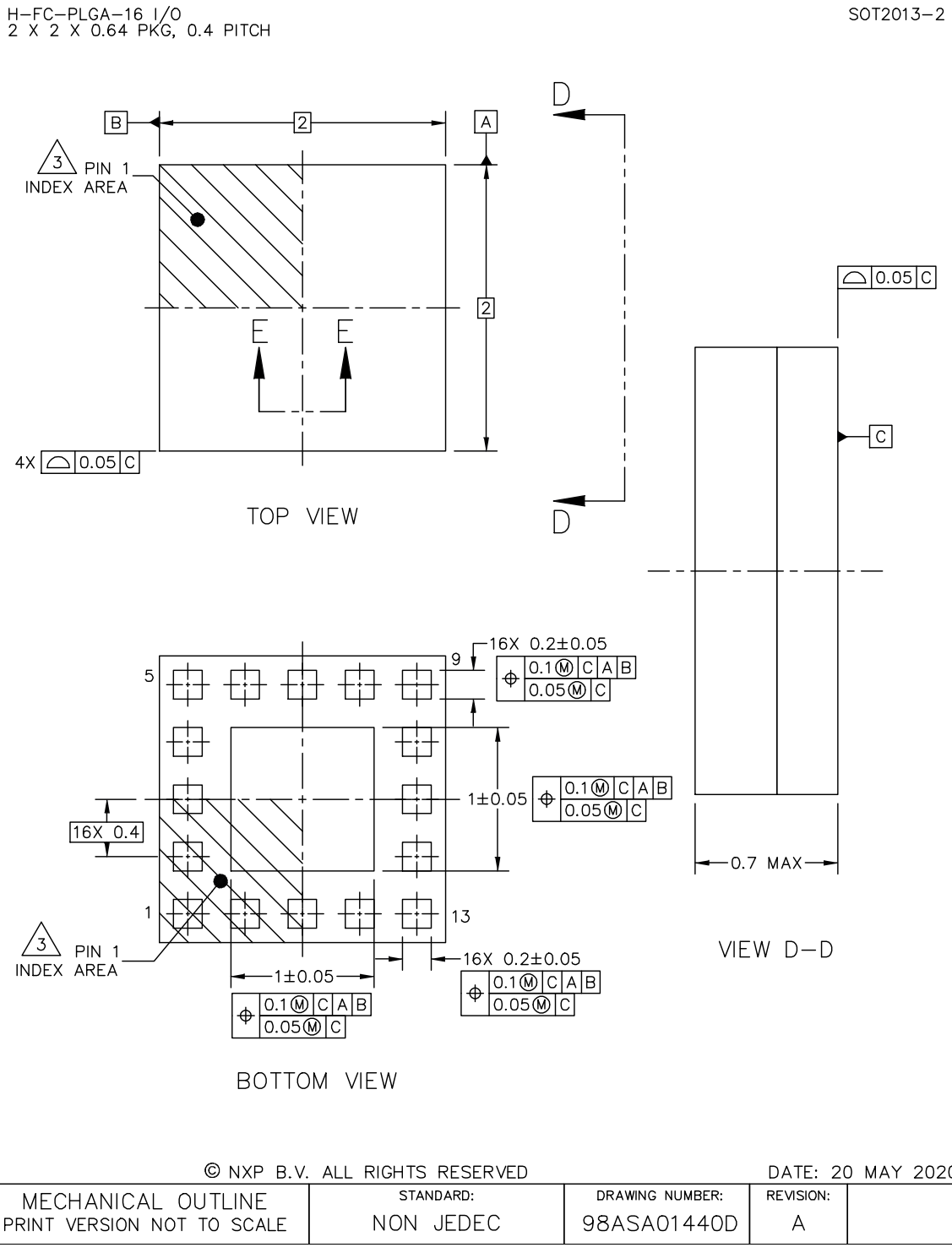


Figure 6. HWFLGA16, SOT2013-2

Note: *See figure Figure 7 below for actual footprint.*

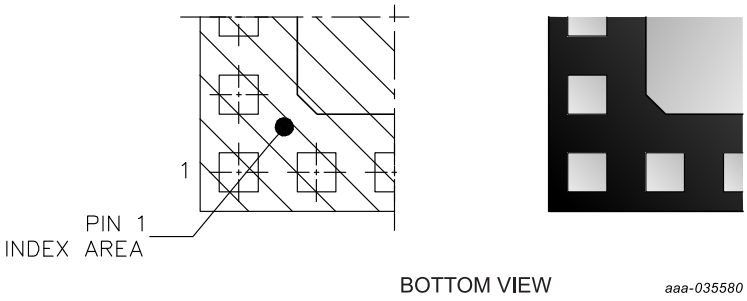


Figure 7. WLAN7102C pin 1 index area

16.1 Footprint and solder information

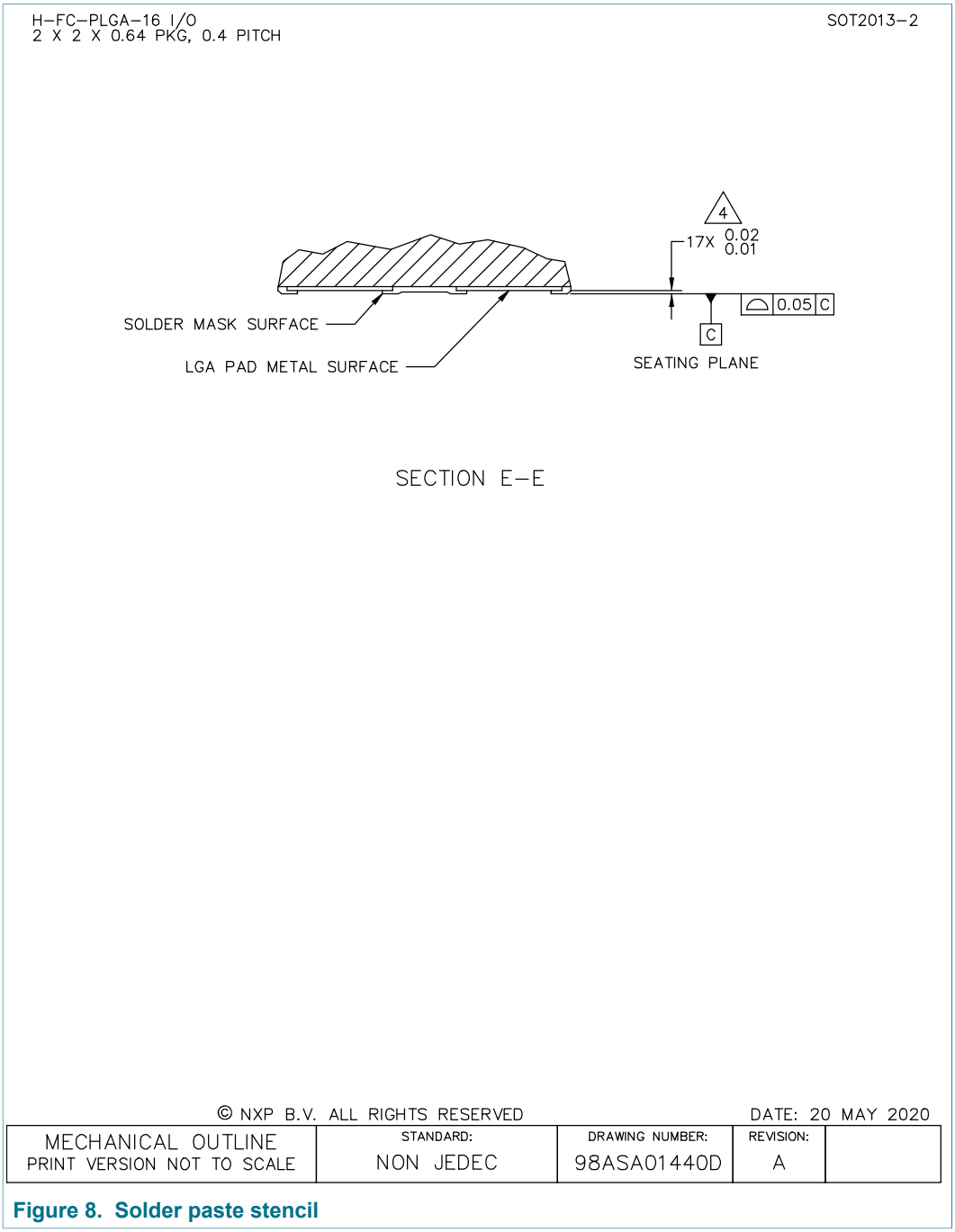


Figure 8. Solder paste stencil

NXP recommends by default to apply the soldering and footprint guidelines as are released in POD SOT2013-2.

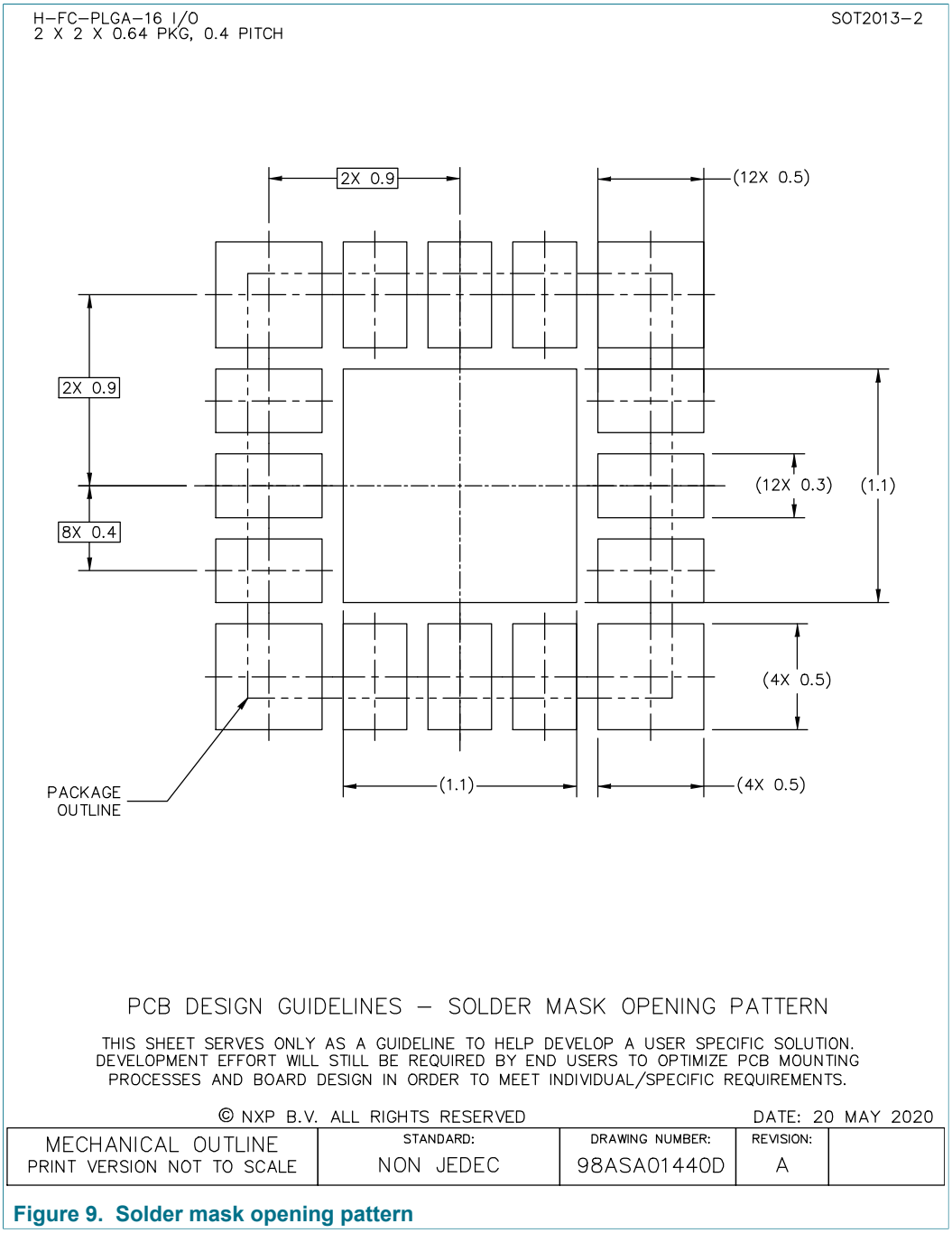


Figure 9. Solder mask opening pattern

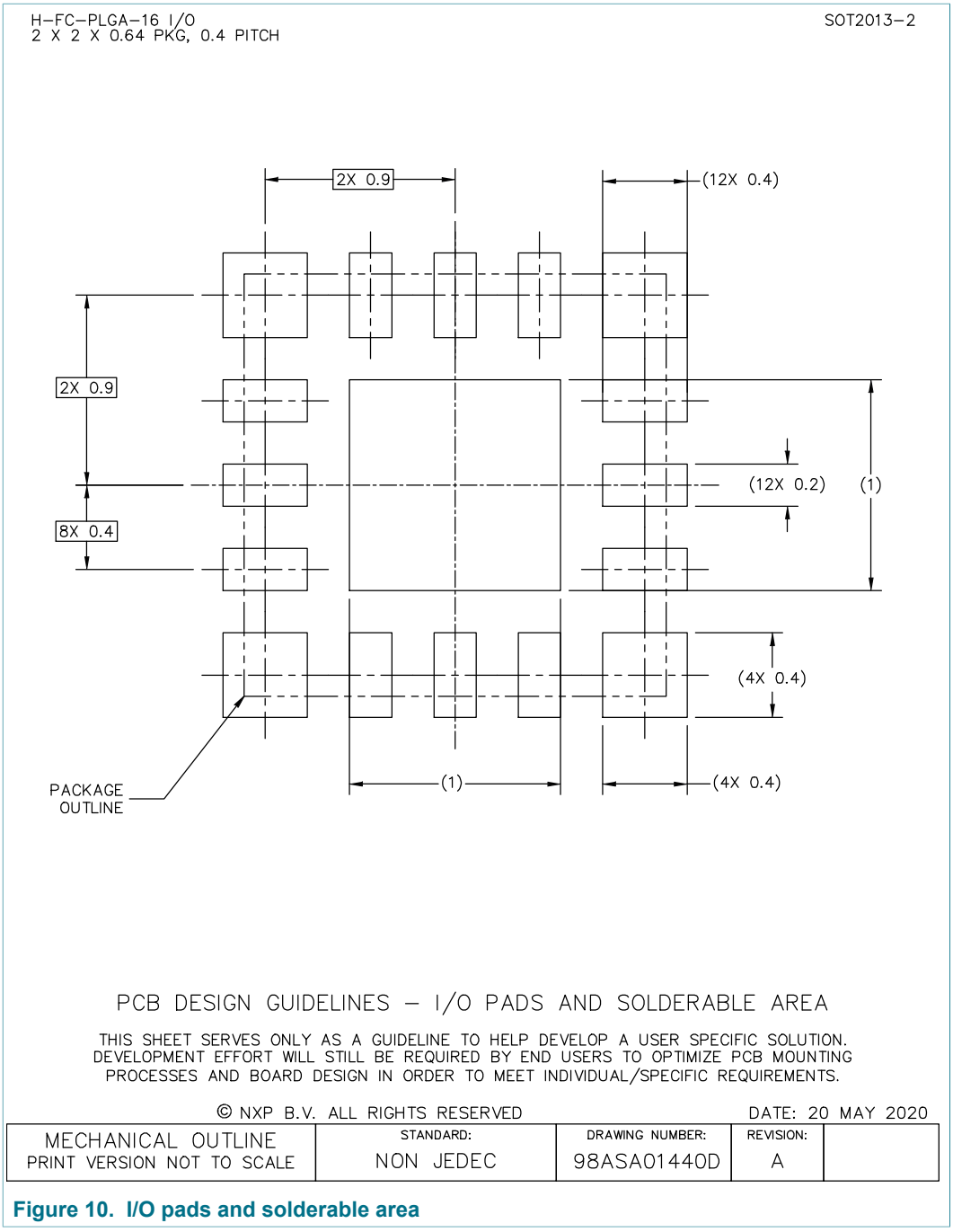


Figure 10. I/O pads and solderable area

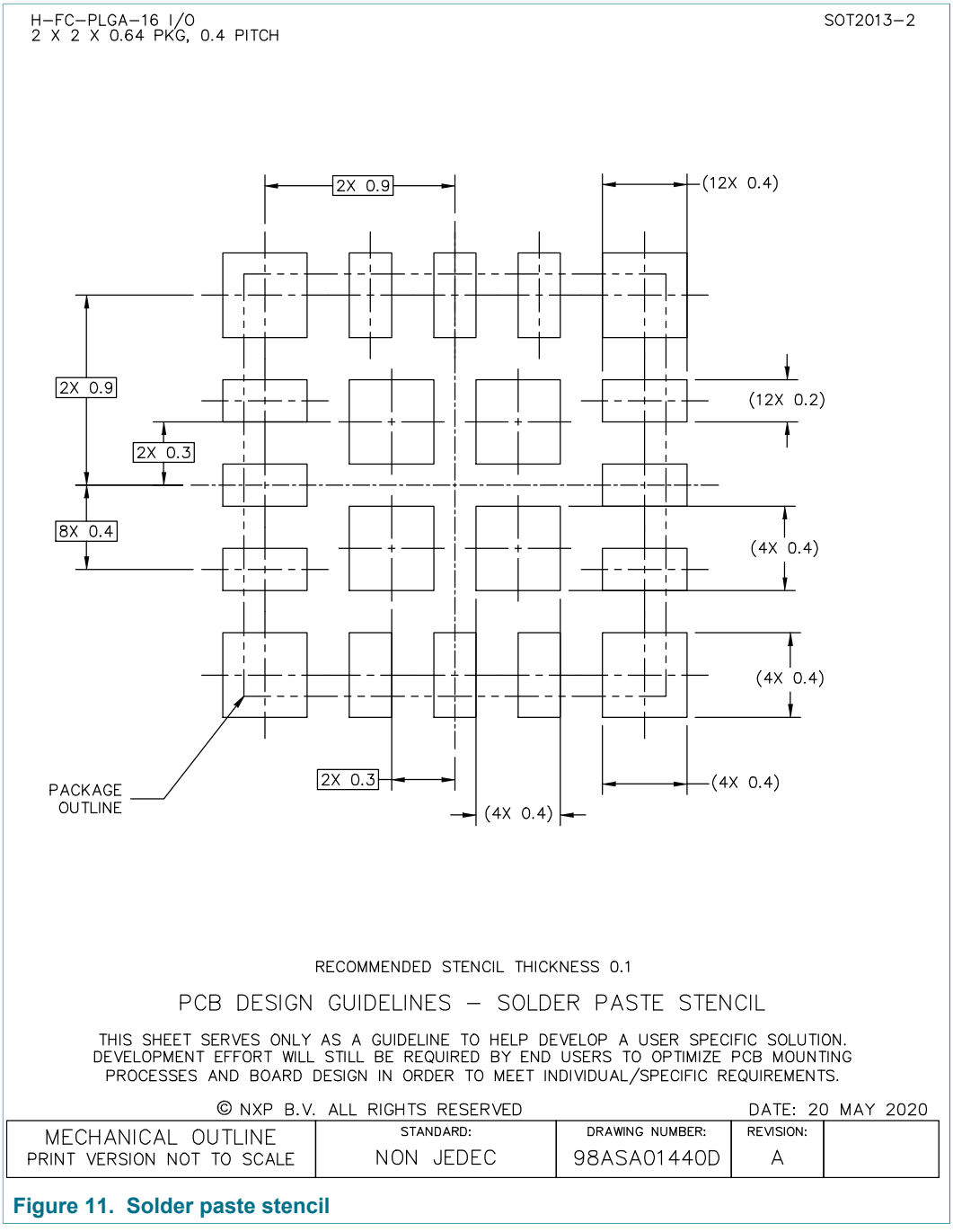


Figure 11. Solder paste stencil

17 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

18 Abbreviations

Table 15. Abbreviations

Acronym	Description
ANT	antenna
CDM	charge device model
CW	continuous wave
DC	direct current
ESD	electrostatic discharge
EVM	error vector magnitude
FEIC	front end-integrated circuit
HBM	human body model
ISM	industrial scientific medical
ISL	isolation
LTE_LAA	LTE licensed assisted access
MCS	modulation code scheme
MIMO	multiple in multiple out
MSL	moisture sensitivity level
NF	noise figure
PA	power amplifier
RF	radio frequency
WLAN	wireless local area network

19 Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
WLAN7102C v.4	20200915	Product data sheet	-	WLAN7102C v.3
modification	• Changed status from Company confidential to Public • updated the ESD condition on CDM with the correct description of the used ESD standard • added solder information to the data sheet			
WLAN7102C v.3	20191210	Product data sheet	-	WLAN7102C v.2
modification	• changed some conditions and values on EVM parameter for TX to ANT, on 11a OFDM54, and 11n MCS7 HT20 • added extra conditions and values on EVM parameter for TX to ANT, 11n MCS7 HT40, 11ac MCS9 VHT160, and 11ax MCS10/11 HE160			
WLAN7102C v.2	20191128	Product data sheet	-	WLAN7102C v.1
modification	• changed minimum value on detected voltage to 760 mV on P_o = 22 dBm f = 5400 MHz condition			
WLAN7102C v.1	20191122	Product data sheet	-	-

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 September 2020
Document identifier: WLAN7102C

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:
WLAN7102CZ