UM11723

KITPF5200FRDMEVM evaluation board

Rev. 1 — 8 December 2021 **User manual**

Document information

Information	Content
Keywords	PF5200, FRDM-KL25Z, PF200 NXP GUI, PMIC, mirror register, One-Time Programming, Try Before Buy
Abstract	The KITPF5200FRDMEVM evaluation board user guide is intended for the engineers involved in the evaluation, design, implementation, and validation of PF5200, Fail-safe system basis chips with multiple SMPS. The main purpose of this board is to run performance test. For device programming, use KITPF5200SKTEVM socket board.

Revision history

Table 1. Revision history

Revision	Date	Description
UM11723 v.1	20211208	Initial release

Important notice

NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

The KITPF5200FRDMEVM evaluation board user guide is intended for the engineers involved in the evaluation, design, implementation, and validation of PF5200, Fail-safe system basis chip with multiple SMPS (Switch Mode Power Supplies).

This board allows to run performance test as the device is soldered on it. For OTP programming in development phase, use KITPF5200SKTEVM.

This document contains all of the information required to evaluate the PF5200 Fail-safe system basis chip with two SMPS connected in single or dual mode.

The document covers connecting the hardware, installing the software and tools, configuring the environment, and using the kit.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for KITPF5200FRDMEVM evaluation board is at http://www.nxp.com/KITPF5200FRDMEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITPF5200FRDMEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the KITPF5200FRDMEVM requires the kit contents, additional hardware, and a Windows PC workstation with software installed.

3.1 Kit contents

The KITPF5200FRDMEVM kit contains the following items:

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag.
- 3.0 ft USB-STD A to USB-B-mini cable
- Jumpers mounted on board
- PF52 part soldered on top
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary when working with this kit.

- Power supply with a range of 3.3 V to 5.0 V. Current limit depends of the use case, but a 4.0 A current limit supports all use cases

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation.

- USB-enabled computer with Windows 7 or Windows 10

3.4 Software

The following software must be installed on the PC workstation prior to using the KITPF5200FRDMEVM evaluation board.

- PF5200 NXP GUI installation package

4 Getting to know the hardware

4.1 Kit overview

The KITPF5200FRDMEVM kit provides an integrated platform for evaluating designs based on NXP's PF5200 dual-channel PMIC. All PF5200 features can be accessed and monitored in a test environment.

The kit hardware consists of the KITPF5200FRDMEVM evaluation board, a FRDM-KL25Z microcontroller board, and the USB cable required to connect the FRDM-KL25Z to the PC.

The KITPF5200FRDMEVM evaluation board features an individual PF5200 soldered on board. Connectors, jumpers, and switches on the board can be used to configure an evaluation environment that meets specific design requirements. The board also contains LEDs and test points that provide a means of monitoring performance in real time.

The FRDM-KL25Z is mounted to Arduino connectors on the bottom of the KITPF5200FRDMEVM board. The role of the FRDM-KL25Z is to manage I^2C communication between the KITPF5200FRDMEVM board and the GUI installed on the PC.

4.2 KITPF5200FRDMEVM features

- Banana 4 mm for power supply input
- Banana 4 mm for switcher 1 and switcher 2
- Selectable OTP or TBB mode
- PGOOD, RESETBMCU and XFAIL pins
- USB to I^2C protocol for easy connection to software GUI
- LEDs, green and red, that indicate signal or regulator status
- LED blue to indicate that VDDOTP pin is set to 8.0 V (OTP burning voltage)

4.3 KITPF5200FRDMEVM featured components

Figure 1 shows the location of key KITPF5200FRDMEVM components.

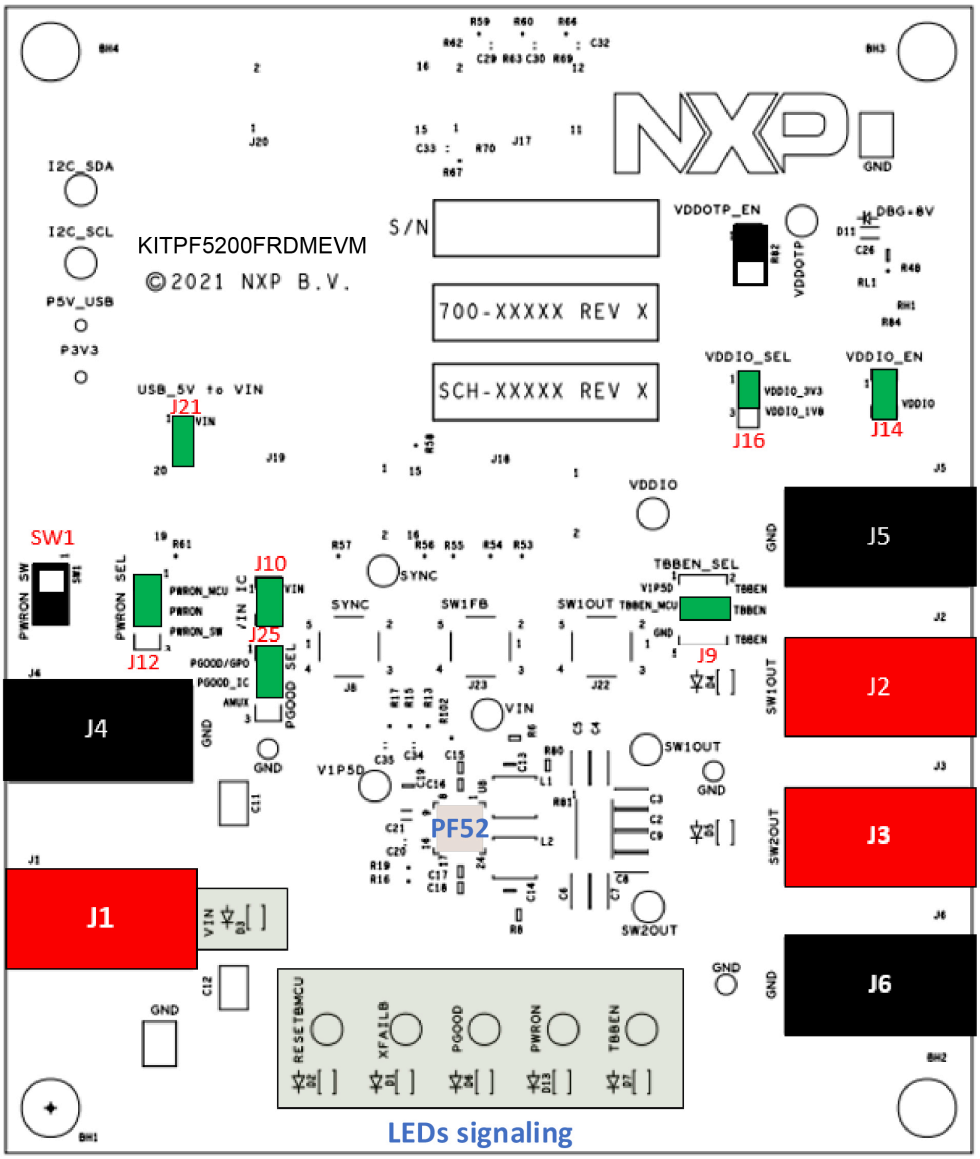


Figure 1. Evaluation board featured component locations

Table 2. Jumper or switch functions

Position	Function	Description
J1 / J4	VIN	Input voltage (3.3 V min / 5.5 V max)
J2 / J5	SW1OUT	Output for SW1
J3 / J6	SW2OUT	Output for SW2
SW1	VIN switch	PWRON manual control (assume J12 on PWRON_SW position)
J9	TBBEN_SEL	Apply either V1P5D or 3.3 V from MCU or GND to TBBEN pin
J10	VIN_IC	Apply VIN to VIN IC pin
J12	PWRON_SEL	PWRON controlled either by the MCU or manually by SW1
J14	VDDIO_EN	Apply VDDIO to VDDIO pin
J16	VDDIO_SEL	VDDIO set to either 1.8 V or 3.3 V

Table 2. Jumper or switch functions*...continued*

Position	Function	Description
J22	PGOOD_SEL	PGOOD setting either PGGO/GPO or output of temperature junction analog voltage

4.3.1 VIN connectors

Nominal VIN voltage is 3.3 V minimum / 5.5 V maximum.

Table 3. VIN connector (J1 / J4)

Schematic label	Signal name	Description
J1	VIN	VIN supply input
J4	GND	Ground

4.3.2 SW1OUT and SW2OUT connectors

Each switch can be controlled between 0.6 V / 1.2 V.

Current capability is up to 8.0 A, assuming current limit is correctly set.

Voltage and current limits are set by OTP.

Table 4. SW1OUT and SW2OUT connectors

Schematic label	Signal name	Description
J5	GND	Ground
J2	SW1OUT	SW1 output power supply
J6	GND	Ground
J3	SW2OUT	SW2 output power supply

4.3.3 SW1 switch

This switch gets control only if the PWRON_SEL jumper is in the PWRON_SW position. Otherwise, SW1 has no effect.

Table 5. PWRON_SEL switch (SW1)

Schematic label	Description
SW1 ON	PWRON set to 1
SW1 OFF	PWRON set to 0

4.3.4 TBBEN_SEL jumper (J9)

This jumper selects the input voltage to the TBBEN pin.

Table 6. TBBEN_SEL jumper (J9)

Schematic label	Signal name	Description
J9-1-2	V1P5D	TBBEN is supplied with V1P5D (TBB mode forced)
J9-3-4	TBBEN_MCU	TBBEN pin is controlled by the MCU in Normal or TBB mode
J9-5-6	GND	TBBEN is tied to Ground (Normal mode forced)

4.3.5 VIN_IC jumper (J10)

This jumper selects the VIN power source. The main purpose is to enable VIN current measurements.

Table 7. VIN_IC jumper (J10)

Schematic label	Signal name	Description
J10-1	VIN	Connected to VIN power input power supply
J10-2	VIN_IC	Connected to VIN of the device

4.3.6 PWRON_SEL jumper (J12)

PWRON can be controlled either by the FRDM-KL25Z MCU, allowing control by script, or manually.

Table 8. PWRON_SEL jumper (J12)

Schematic label	Signal name	Description
J12-1-2	PWRON_MCU	PWRON pin is controlled by the MCU
J12-2-3	PWRON_SW	PWRON pin is controlled manually by SW1

4.3.7 VDDIO_EN jumper (J14)

VDDIO_EN enables VDDIO from the external LDO to the VDDIO pin of the device.

Table 9. VDDIO_EN jumper (J14)

Schematic label	Signal name	Description
J14-1	VDDIO ext	VDDIO voltage from external LDO
J14-2	VDDIO PF5200	VDDIO connected to PF5200

4.3.8 VDDIO_SEL jumper (J16)

VDDIO_SEL selects 1.8 V or 3.3 V for VDDIO.

Table 10. VDDIO_SEL jumper (J16)

Schematic label	Signal name	Description
J16-1-2	VDDIO 3.3 V	Set external LDO to 3.3 V
J16-2-3	VDDIO 1.8 V	Set external LDO to 1.8 V

4.3.9 PGOOD_SEL jumper (J22)

PGOOD_SEL selects either PGOOD/GPO or temperature sensor.

To be effective, the PGOOD pin must be configured correctly through I^2C using the GUI.

Table 11. PGOOD_SEL jumper (J22)

Schematic label	Signal name	Description
J22-1-2	PGOOD/GPO	PGOOD / GPO mode; apply an external pull up to PGOOD pin
J22-2-3	AMUX	Temperature sensor mode; no pull-up connected to PGOOD pin

4.3.10 LED signaling

The LED signaling displays the state of the following signals:

- Signals: PWRON, TBBEN, PGOOD, RESETBMCU and XFAIL
- Regulators: SW1OUT and SW2OUT, LEDs light above 0.6 V
- Power supply: VIN

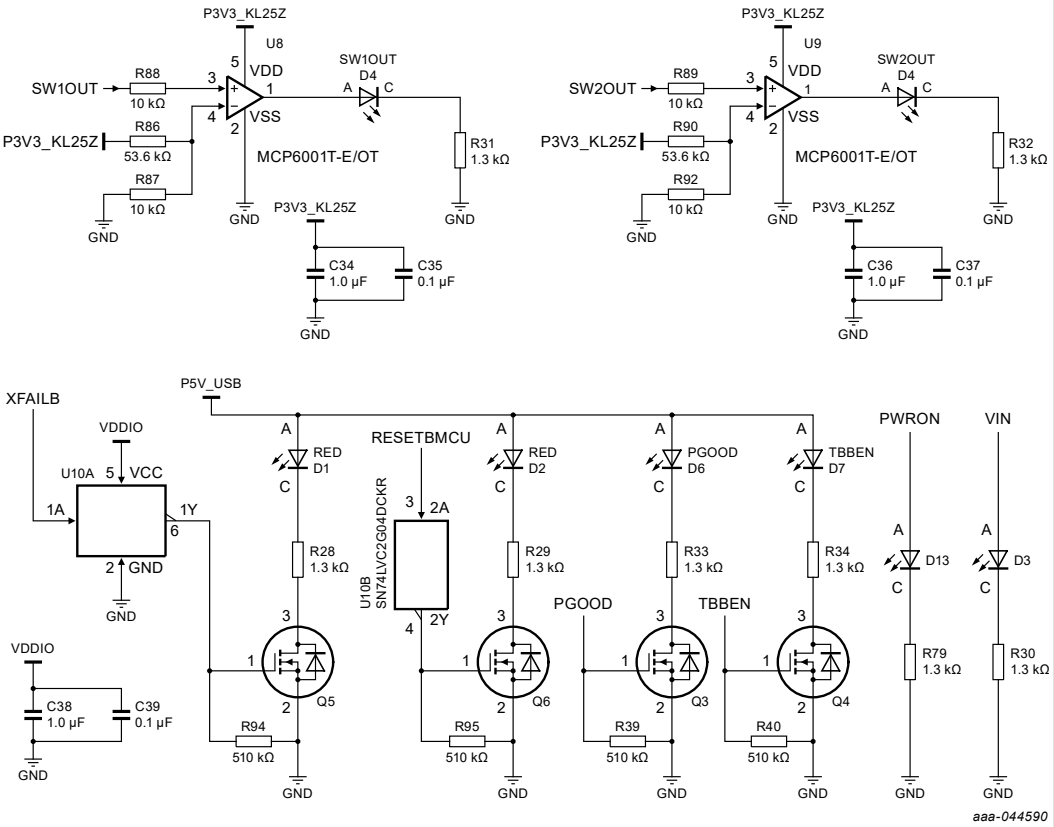


Figure 2. Power and Regulators LED indicators

4.3.11 Test points

The KITPF5200FRDMEVM board has several test points that facilitate access and measurements. This section summarizes the available test points, how they are color coded, and whether they are a test point component with a part number or a through-hole test point with no part number.

Orange: Test loop access to safety outputs and analog signals

Red: Test loop access for power supplies

Black: Test loop access to GND

Blue: Not a part. Through hole small test points on board close to the signal

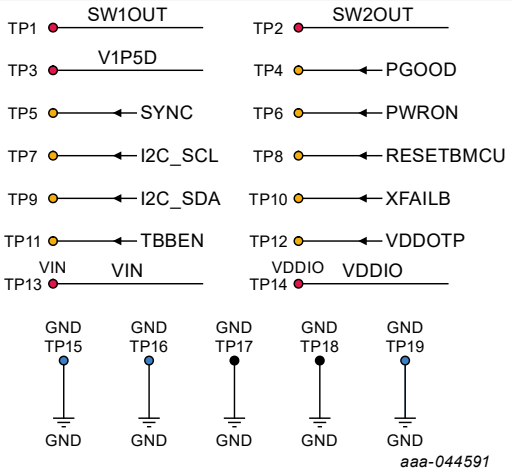


Figure 3. Test points

4.4 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the KITPF5200FRDMEVM evaluation board are available at http://www.nxp.com/KITPF5200FRDMEVM.

5 Installing and configuring software and tools

5.1 Flashing or updating the GUI firmware

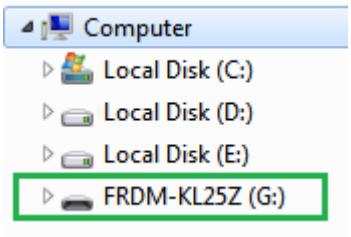
The KITPF5200FRDMEVM is delivered with the GUI firmware already flashed. If your MCU firmware is already flashed, you can ignore this section. If you need to update the firmware or it is malfunctioning, follow the instructions detailed in the following sections.

5.1.1 Flashing the FRDM-KL25Z firmware – Windows 7

If BOOTLOADER is already loaded on the FRDM-KL25Z board, skip Step 1 and Step 2 and start with Step 3.

1. Press the RST push-button and plug the USB cable into the SDA port on the FRDM-KL25Z board.
   - A new “BOOTLOADER” device appears on the left pane of the File explorer.
2. Locate the file **MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA** from the package and drag and drop into the BOOLTLOADER device.
   - Note: Make sure to allow enough time for the firmware to be saved in the bootloader.

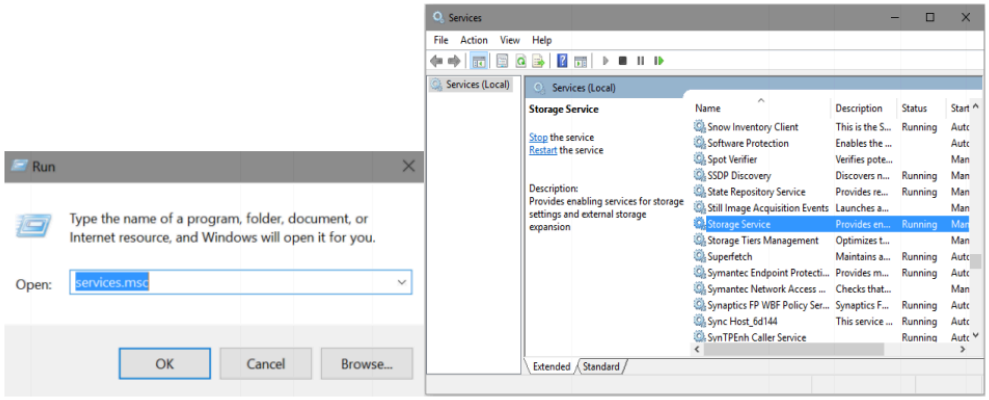
3. Disconnect and reconnect the USB cable into the SDA port.
   - This time without pressing the RST push-button, the FRDM_KL25Z device should appear on the left pane of the File explorer as shown in the following figure.



4. Locate the file "**nxp-gui-fw-frdmkl25z-usb_hid-pf5200_v0.9.bin**" from the package and drag and drop the file into the FRDM_KL25Z device.
   - Note: Make sure to allow enough time for the firmware to be saved.
5. Freedom board firmware is successfully loaded. Disconnect the USB cable from the SDA port and reconnect it to the FRDM-KL25Z USB port.

5.1.2 Flashing the FRDM-KL25Z firmware – Windows 10

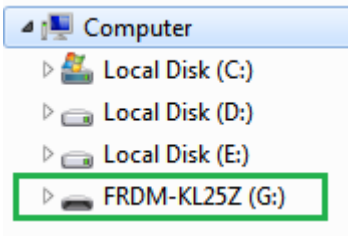
1. Disable the storage services: run the services, double-click on the storage service from the list and press the Stop button.



If BOOTLOADER is already loaded on the FRDM-KL25Z board, skip Step 2 and Step 3 and start with Step 4.

2. Press the RST push-button and plug the USB cable into the SDA port on the Freedom board.
   a. A new "BOOTLOADER" device should appear on the left pane of the File explorer.
3. Drag and drop the file "MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA" into the BOOTLOADER drive.
   a. Note: Make sure to allow enough time for the firmware to be saved in the bootloader.

4. Disconnect and reconnect the USB cable into the SDA port.
   - This time without pressing the RST push-button, the FRDM_KL25Z device should appear on the left pane of the File explorer as shown in the following figure.
   -



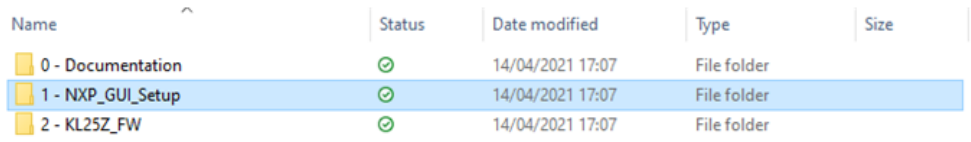
5. Locate the file **nxp-gui-fw-frdmkl25z-usb_hid-pf5200_v0.8.bin** from the package and drag and drop the file into the FRDM_KL25Z device.
   - Note: Make sure to allow enough time for the firmware to be saved.
6. Freedom board firmware is successfully loaded. Disconnect the USB cable from the SDA port and reconnect it into the KL25Z USB port.

5.2 PF52 NXP GUI

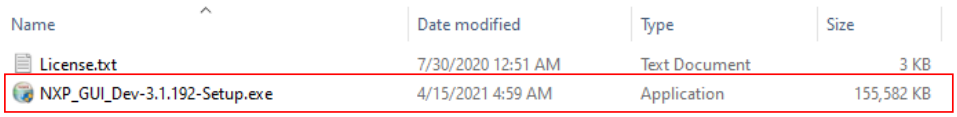
5.2.1 Installing the GUI software package

To install the PF5200 NXP GUI download or obtain the NXP GUI package, unzip an open 1-NXP_GUI_Setup folder:

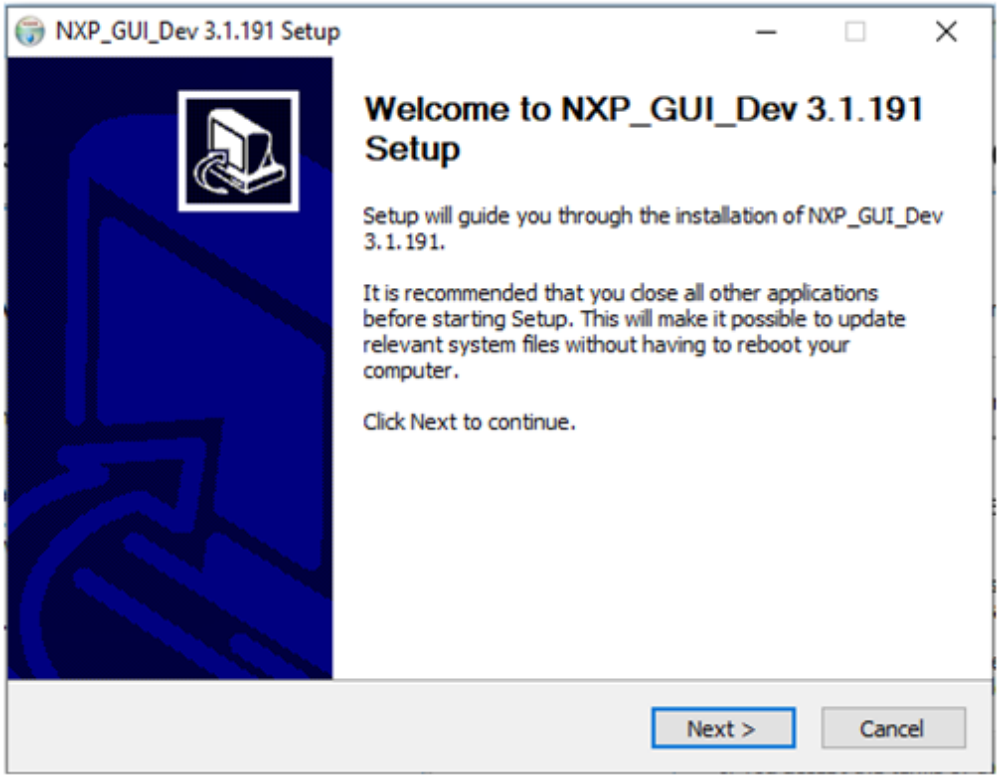
1. Download or obtain the NXP GUI package. Unzip and open the 1-NXP_GUI_Setup folder.



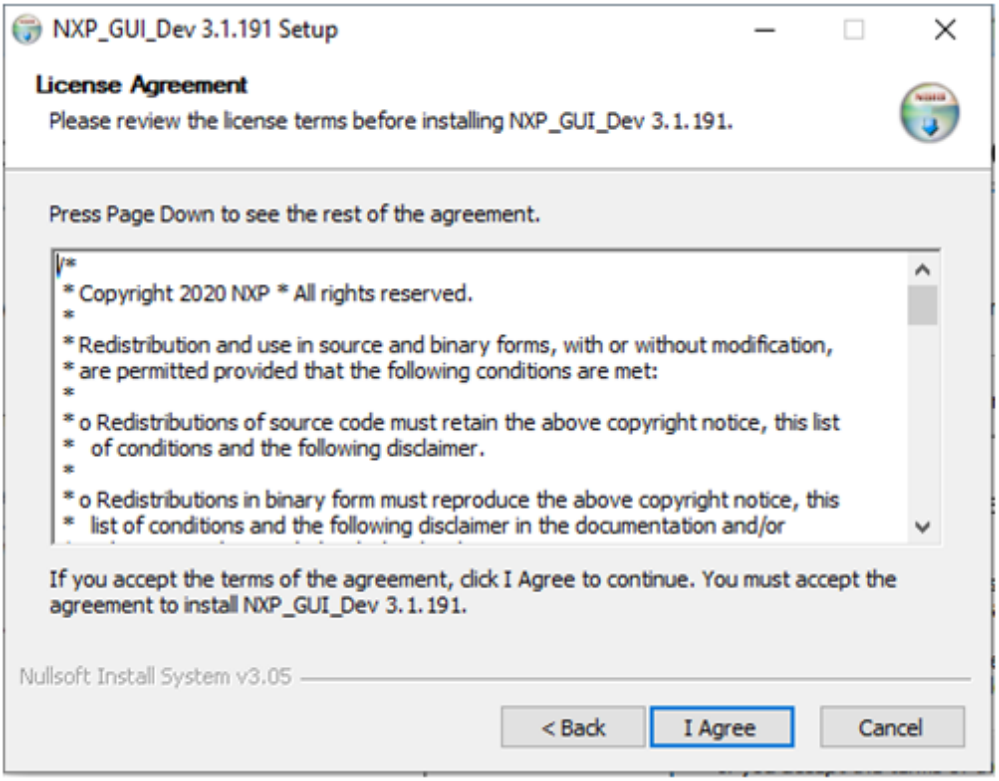
2. Double-click **NXP_GUI_version-Setup.exe** and follow the instructions.



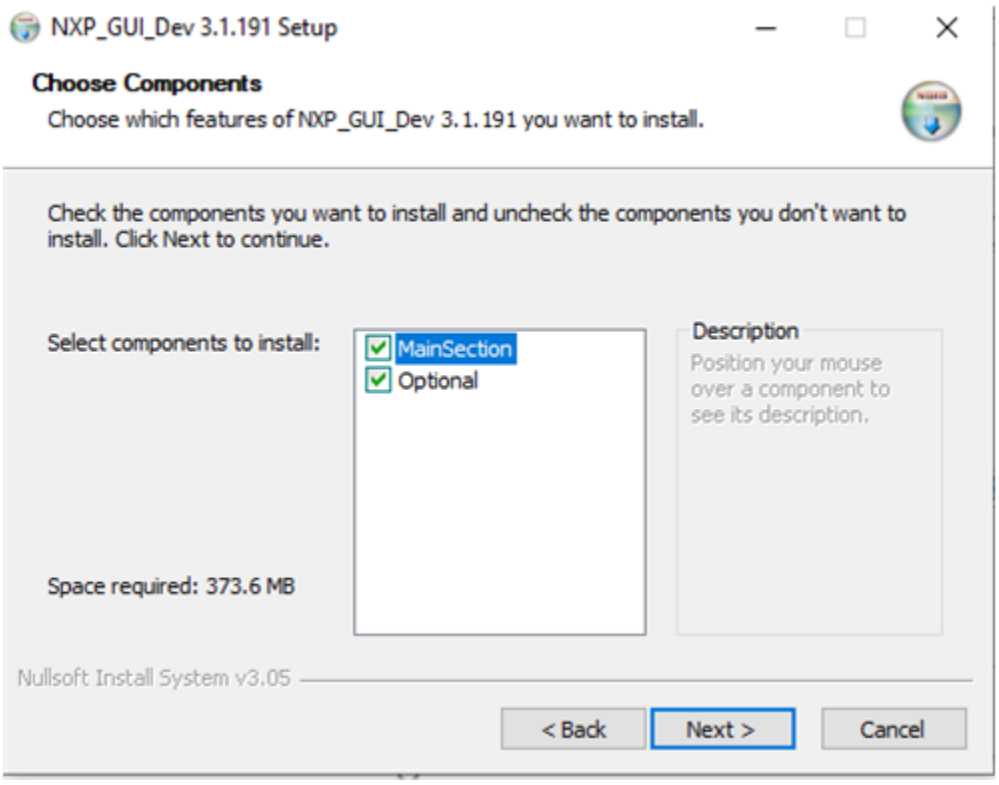
3. Click **Next** when the initial application setup window appears.



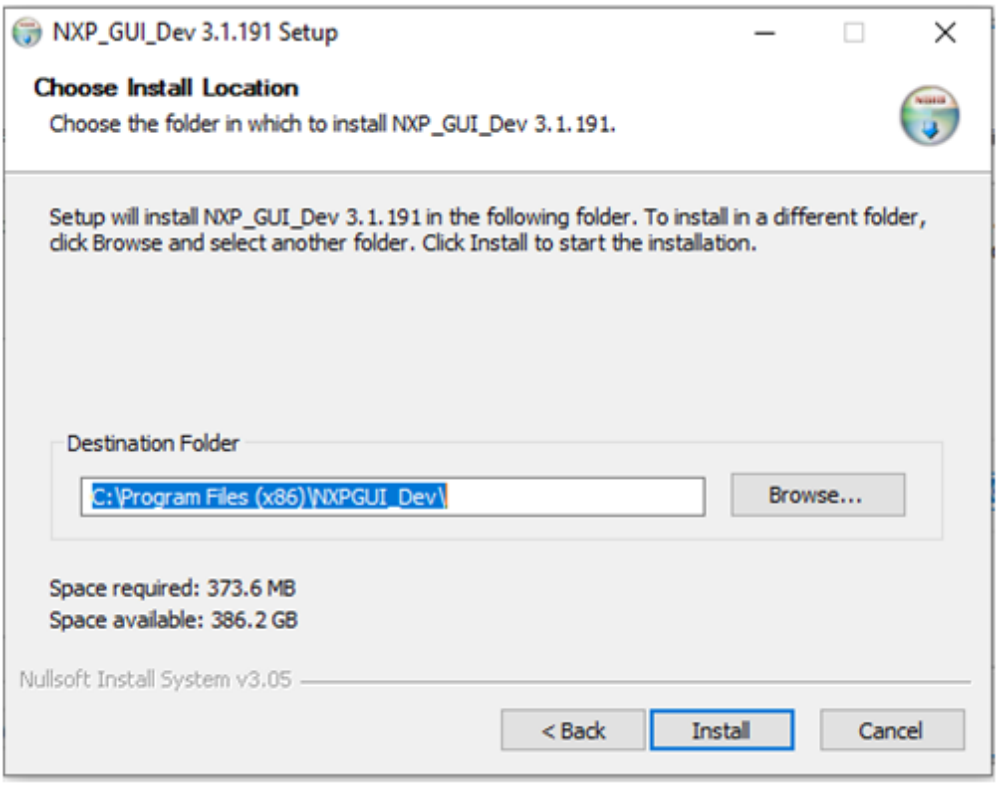
4. On the License Agreement window, read the license information and click **I Agree**.



5. In the Choose Components window, select the GUI components you want to install. Then click **Next**.

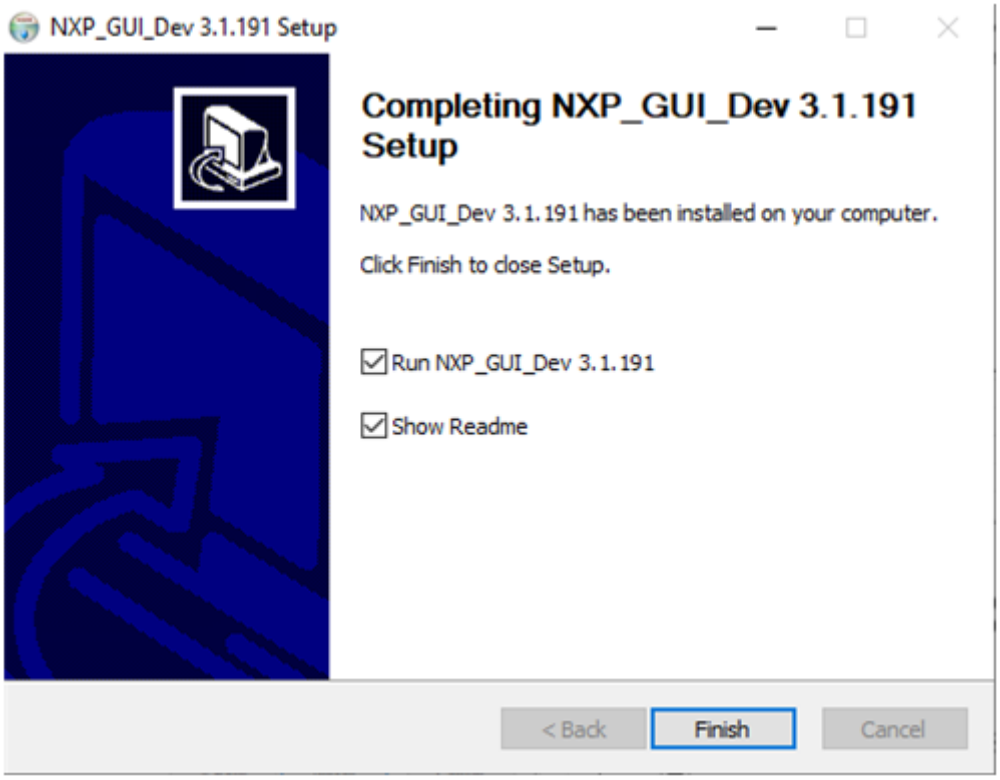


6. In the Choose Install Location window, choose the folder where you want the GUI installed.



7. In the completing setup window, select the following options:
   - **Run NXP_GUI**
   - **Show Readme**

   Click **Finish** to complete the installation.

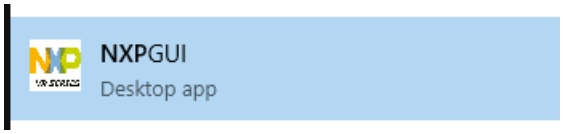


8. When the installation is completed, the GUI opens automatically. Proceed to Step 2 in Section 5.2.2 "Launching the PF52 NXP GUI".

5.2.2 Launching the PF52 NXP GUI

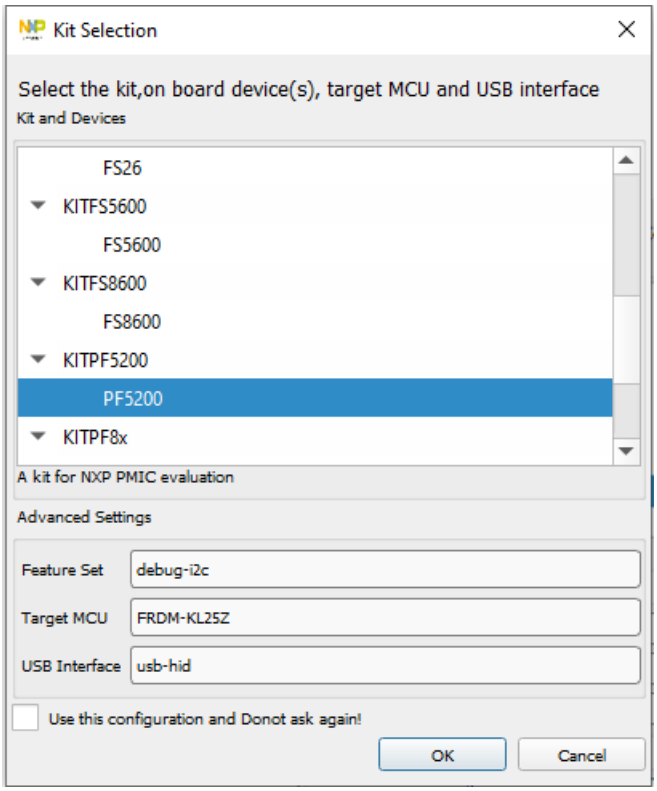
When the KITPF5200FRDMEVM kit is set up and the GUI installed, follow the steps below to launch the GUI:

1. Click on the Windows icon (bottom left corner) and locate the NXP GUI in the Windows All Apps bar, Click the NXPGUI icon to launch the GUI.

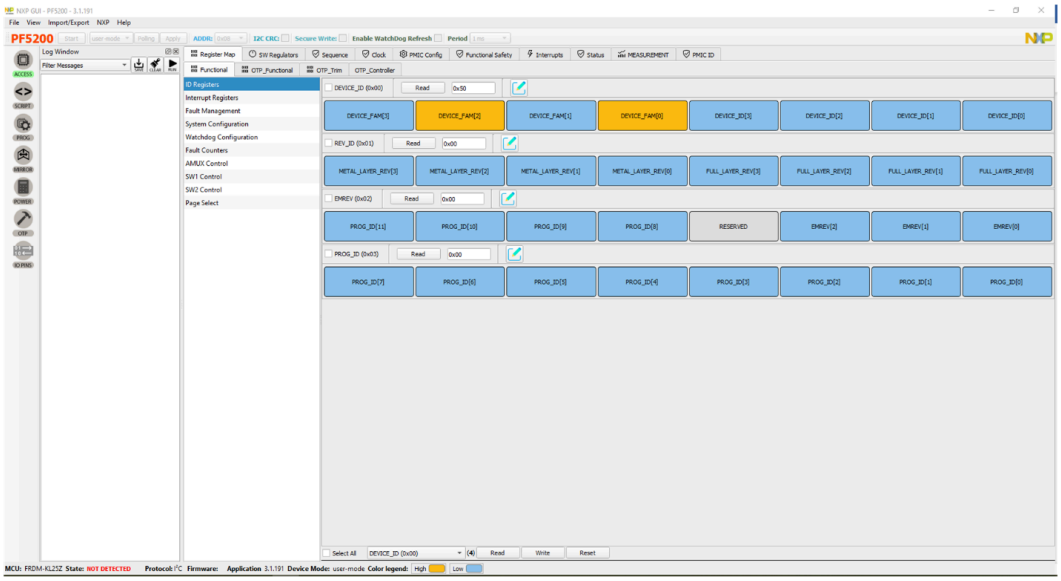


2. When the GUI opens, the first window to appear is the Kit Selection window. In the Kit Selection window, select the settings shown below. To avoid the Kit Selection Window on every launch, check the box “Use this configuration and do not ask again". The Kit

Selection window can also be disabled through the File main menu item. When you finish selecting the settings, click **OK**.



3. The Framework window opens as shown below:



5.2.3 The Framework window

The Framework window consist of the following sections:

- **Device manager:** used to start communication with device, enter or exit test mode, enable I^2C CRC and I^2C secure access, enable watchdog.
- **Framework settings:** manages file import/export and framework configuration.
- **Window log:** reports USB and Device communication events.
- **USB and device status:** indicates if USB or device is connected or disconnected, shows firmware and GUI version, displays current state of FS state machine. Click Display button to refresh.
- **Tools access bar:** provides quick access to the PF52 evaluation tools and features. ***Note:*** *Power tool is currently not available.*
- **Tab content:** shows the content of each tool or tab. There may be more tabs, boxes, or windows inside.

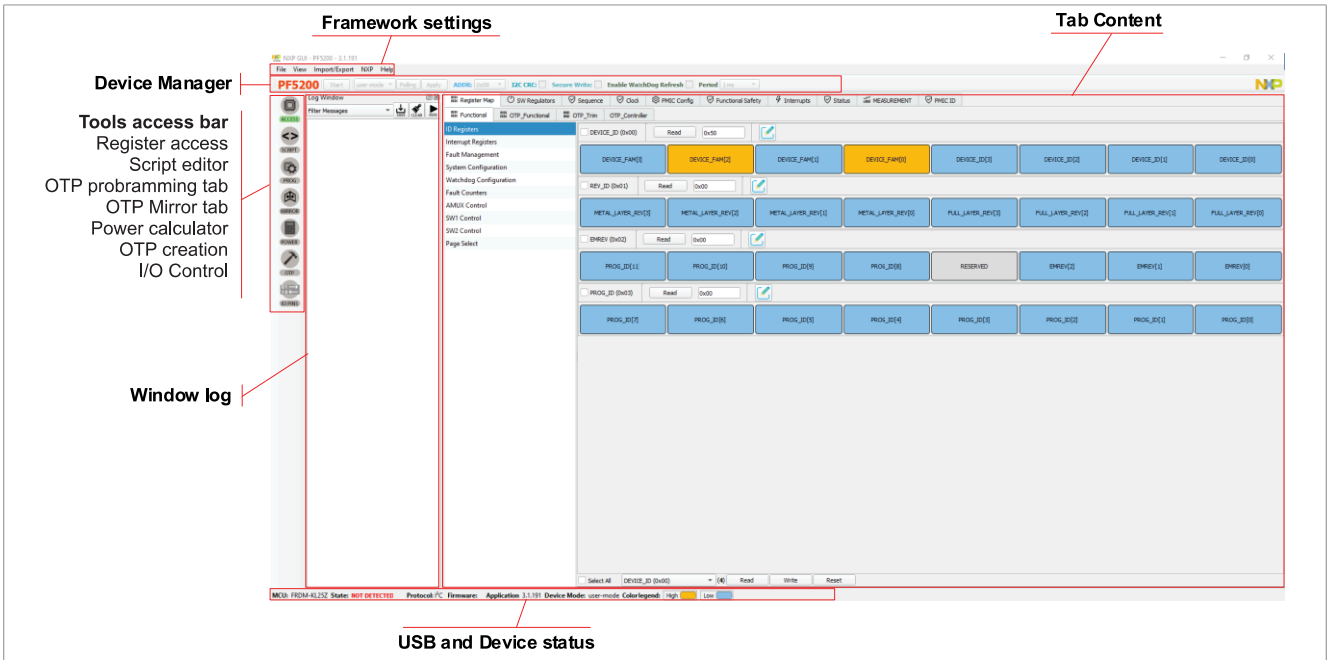
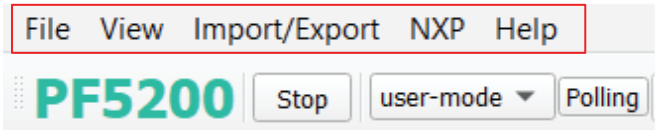


Figure 4. Framework window

5.2.3.1 Framework settings

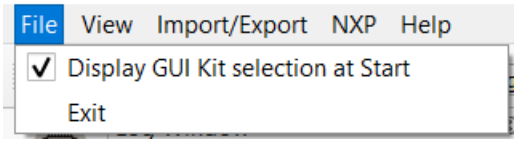
The framework settings section appears at the top left corner of the framework (Figure 4). It consists of five items:

- File
- View
- Import/Export
- NXP
- Help



5.2.3.1.1 File menu item

Load or save a configuration or exit the application. Load and Save are only enabled when OTP tool tab is active.



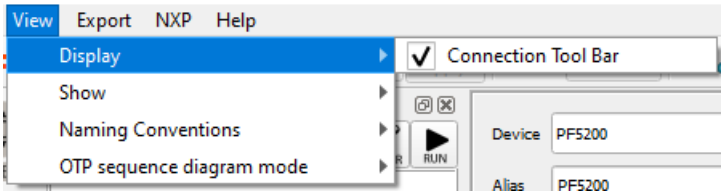
- **Display GUI kit selection at start:** when starting the GUI, allows you to enable/disable the kit selection window.
- **Exit:** exits the NXP GUI application.

5.2.3.1.2 View menu item

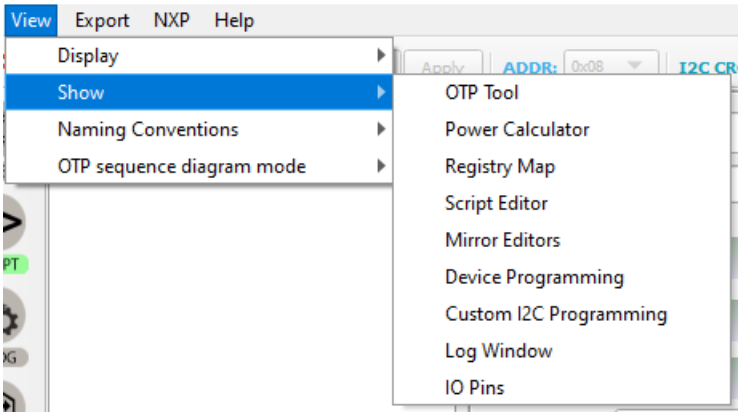
The View menu contains the following options:

1. Display
2. Show
3. Naming conventions
4. OTP sequence diagram mode

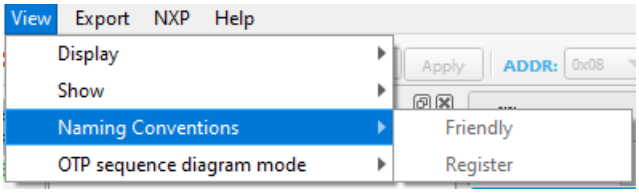
- **Display:** enables and disables the connection tool bar (enabled by default) option.



- **Show:** this option can be used to access various sections of the GUI as shown in the following figure.



- **Naming conventions:** selects Friendly or Register name display for OTP tool. Option enabled only when OTP tool is active.

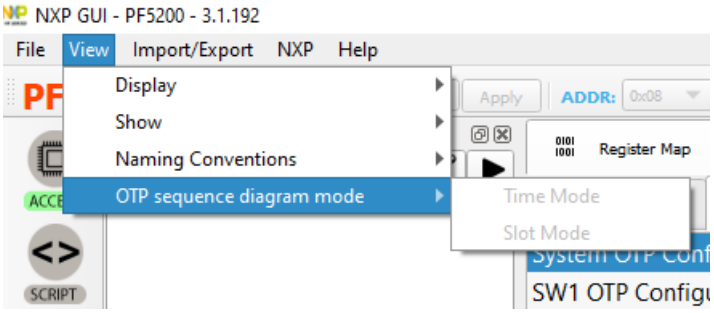


The naming convention options are:

– **Friendly:** causes register names to be displayed as user-friendly names throughout the OTP tool.

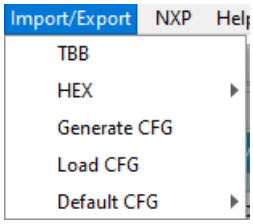
– **Register:** causes register names to be displayed as the register's technical name throughout the OTP tool.

- **OTP sequence diagram mode:** sets the x-axis in the sequence diagram (Sequencer tab) to display in either Time mode (displays the sequence in increments of time) or in Slot mode (displays the sequence in terms of the assigned slots).



5.2.3.1.3 Import/Export menu item

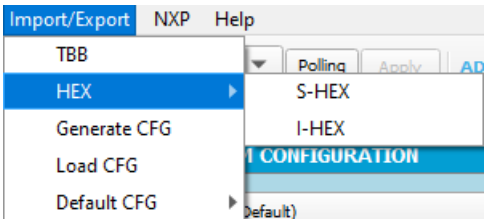
The Import/Export menu item allows you to manage all the files needed for emulation, for use with the OTP PROG tool, and for GUI configuration. This menu item is only active when the OTP tool has been selected. See Section 5.2.3.3.5 "OTP" for details.



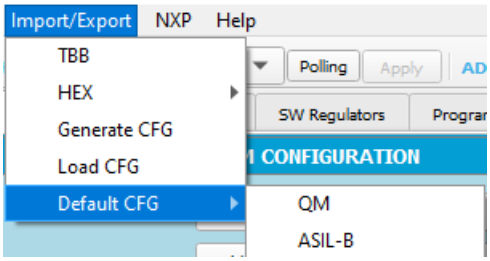
The Import/Export menu consists of the following items:

- **TBB:** exports an OTP configuration into a TBB script file that can be used to load the Mirror registers. The same file can be used by the PROG tool to burn OTP fuses.

- **HEX:** outputs the script in HEX format. A drop-down menu allows you to select the type of HEX format to be exported.

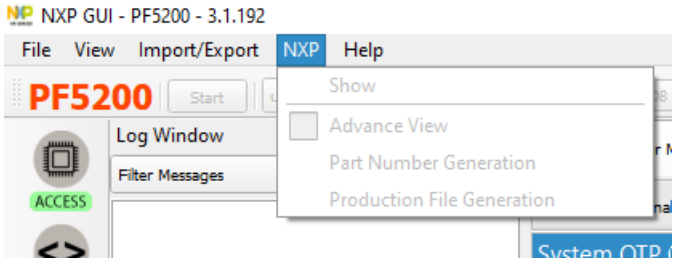


  - **I-HEX:** exports as an Intel Hex script file.
  - **S-HEX:** exports as a Simple Hex script file.
- **Generate CFG:** generates a configuration file (.cfg) used by the GUI.
- **Load CFG:** loads an existing configuration file.
- **Default CFG:** loads a predefined configuration in QM or ASIL-B to use as a starting point.



5.2.3.1.4 NXP menu item

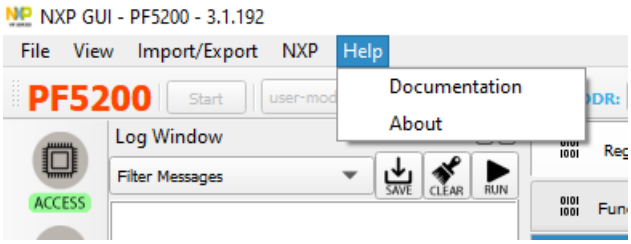
This menu item provides NXP-specific information on the part.



5.2.3.1.5 Help menu item

This menu item contains links to additional information and displays the version number of the installed GUI.

- **Documentation:** lists online NXP documentation related to using the PF5200 GUI.
- **About:** displays the version number of the GUI currently installed.



5.2.3.2 Device manager

The Device Manger menu is located directly below the framework settings menu in the top left corner of the framework window (Figure 4).

Note: *The Device manager does not display if the Connection toolbar is not selected in the Frameworks setting → View → Display menu item.*

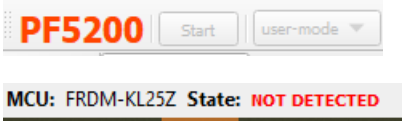
The device manager enables users to start or stop communication with the device, enter or exit the test mode, manage I^2C communications, and enable/disable the watchdog refresh.

The Device manager consists of the following items:

- **Start/Stop**: opens or closes communication with the device.
- **Mode:** selects between TBB and user mode.
- **Polling:** refreshes the current mode.
- **Apply:** applies the selected settings.
- **ADDR:** set the I^2C address assigned to the device.
- **I2C CRC:** indicates whether an extra CRC byte has been enabled by OTP programming.
- **Secure Write:** enables/disables I^2C secure write.
- **Enable Watchdog Refresh:** enables/disables a Watchdog refresh.
- **Period:** sets the Watchdog period.

5.2.3.2.1 Device connection

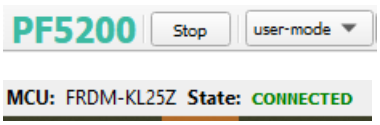
A device connection box appears immediately below the Device manager. When the FRDM-KL25Z is not connected through the USB port, the State indicator in the bottom bar shows **NOT DETECTED**, the PF5200 header text appears red, and the **Start** button is not available.



After the USB cable is connected, the State indicator displays **CONNECTED** and the **Start** button becomes available.

Click the **Start** button to start communication with the PF5200.

At this point, the State indicator displays **CONNECTED** and PF5200 header text changes from red to green.



Usually, when connected, the next step is to load a script that is written to the Mirror register. This must be done in Test mode.

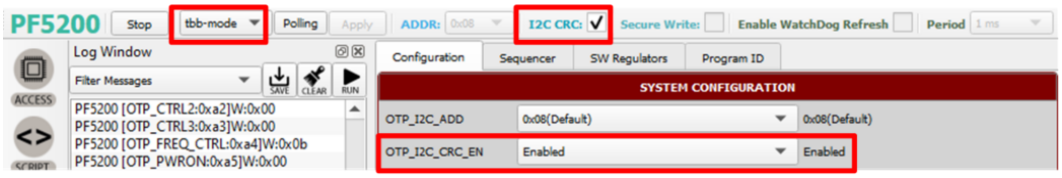
5.2.3.2.2 I^2C CRC enablement

The PF5200 I^2C communication bus can be configured to manage an extra CRC byte. This option is selected during OTP by setting the OTP_I2C_CRC_EN bit. The FRDM-KL25Z must be notified when the OTP_I2C_CRC_EN is enabled in order to correctly manage the I^2C communication. That notification is provided by **I2C CRC** checkbox.

If OTP_I2C_CRC_EN is not enabled in the PF5200, no action is required by the user and the **I2C CRC** box can be left unchecked.

If OTP_I2C_CRC_EN is enabled, the user must select **TBB-MODE** in the Mode box and check the **I2C CRC** box. The GUI then checks if the PF5200 OTP_I2C_CRC_EN bit is enabled. If the GUI verifies that the OTP_I2C_CRC_EN bit is enabled, the selection is valid and the FRDM-KL25Z is able to manage the I^2C CRC.

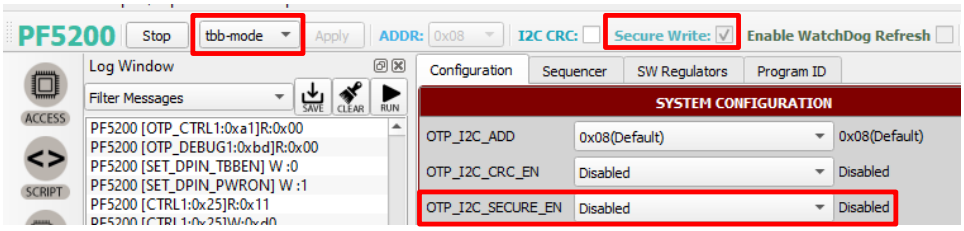
If the check indicates that the OTP_I2C_CRC_EN bit is not enabled, the PF5200 is not able to manage the I^2C CRC and the following error message is displayed: "**WARNING:I2C_CRC is not enabled in PF52**".



5.2.3.2.3 Secure Write Mode enablement

PF5200 provides a Secure Write mechanism for specific bits that are critical to the functional safety of the device.

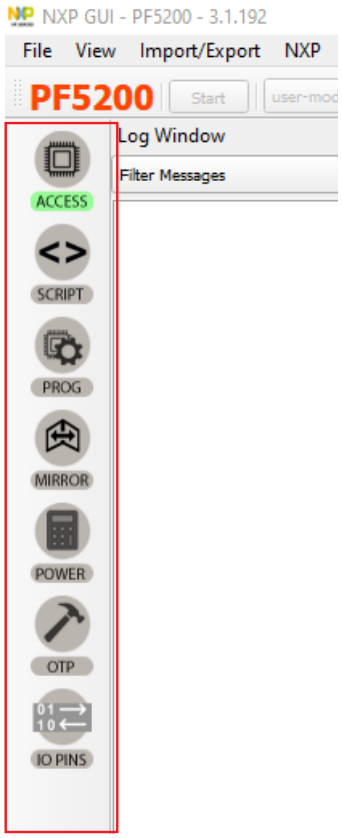
Secure Write sequence request actions from both PMIC and MCU. PMIC actions are enabled by **OTP_I2C_SECURE_EN**, and MCU action are enabled by **Secure Write** checkbox. This mechanism is fully operatives when both PMIC and MCU actions are enabled.



5.2.3.3 Tools access bar

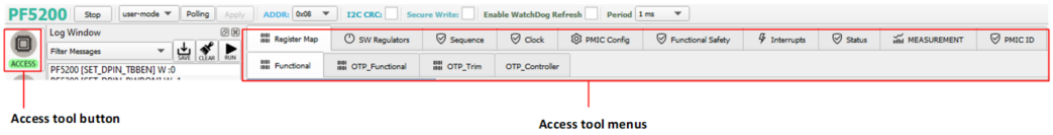
The Tools access bar appears in a vertical row along the left side of the framework window. It provides access to tools that implement various GUI functions. The tool access bar consists of seven items:

- **Access:** provides access to I^2C registers
- **Script:** creates, opens, saves, and runs scripts
- **Prog:** manages OTP fuse-burning process
- **Mirror:** provides access to mirror registers
- **Power:** not available this release
- **OTP:** creates, saves OTP configuration files
- **IO Pins:** reads and sets PF5200 IO pins



5.2.3.3.1 Access

The Access tool provides access all I^2C registers, either in a register map format or in a graphical and more readable view.

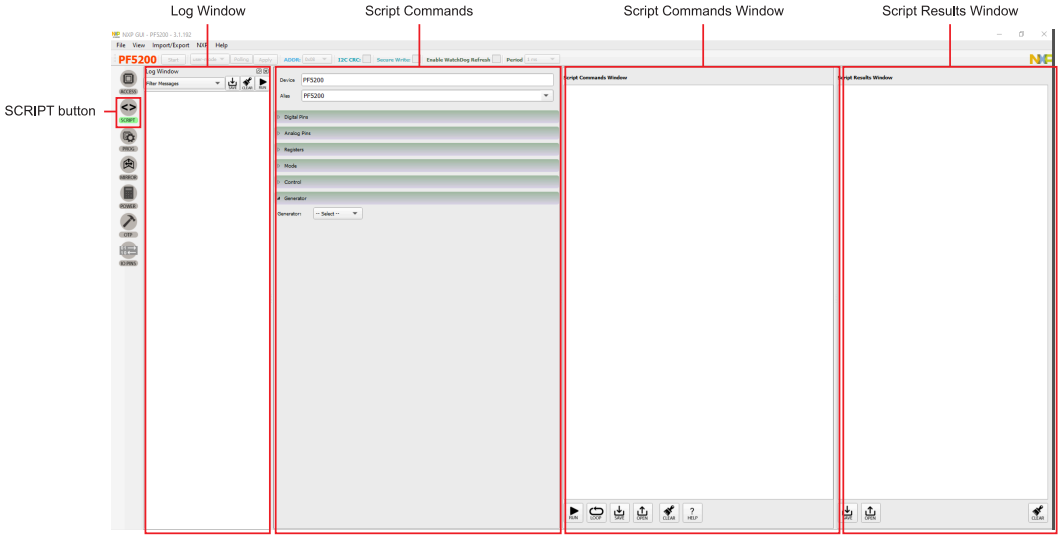


5.2.3.3.2 Script

The script editor allows you to create script sequences or to send existing sequences to the device. You can read/write individually to a register, to a digital pin, or to an analog pin. You can also emulate an OTP configuration with this tool. The Script tool is accessible from Tool access bar.

The Script editor window consist of four sections:

- Log window
- Script commands
- Script commands window
- Script results window



Log window

The Log window list events as they occur in real-time when the script is executing. The filter messages box allows you to limit log messages to certain events (Register Read, Register Write, Pin Read, Pin Write). The Log window menu bar also contains buttons for saving the log contents to a file, clearing the log, or running the script in the script command window.

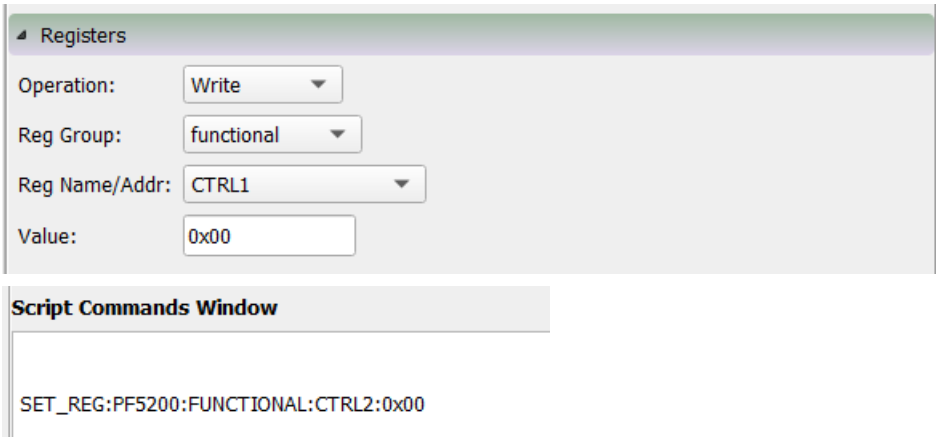
Commands

The Commands window allows you to enter commands into the script command window simply by clicking the appropriate command. This facilitates command entry and assures that there are no syntax errors in the command. The commands are organized into functional categories in the menu. Opening one of menu tabs and selecting the desired pin causes the associated command to appear in the Script Command Window.

- **Digital pins:** enters the script command to read the value of the selected digital pin.
- **Analog pins:** enters the script command to read the value of the selected analog pin.
- **Registers:** enters the script command to read or write to functional and OTP functional registers.
- **Mode:** enters the script command to set the mode to either tbb-mode or user-mode.
- **Control:** enters the script command to pause script execution or to delay script execution. By default, 300 ms is entered as the delay value, but this value can be edited in the Script command window and changed to any ms value. If a Pause command is entered in the Script command window, execution halts when the Pause command is encountered and a pop-up window appears prompting you to continue execution.
- **Generator:** clears the content of the script command window and enters an OTP script sequence.

All menu items function in a similar fashion. The example below shows a typical process using the **Registers** menu tab.

Clicking the Register tab brings up the panel shown in the top image. A Write operation to the CTRL1 register in the functional register group has been selected. The value 0x00 is selected as the value to be written to the register. Pressing Enter with the cursor in the value field enters the well-formed command in the Script Command Window (bottom image).



Script commands window

The Script command window is the area where existing script files can be loaded and where script commands are entered, edited, and executed. The menu bar at the bottom of the window contains the following six buttons:

- **Run:** initiates execution of the script sequence in the script command window.
- **Loop:** executes the script as a loop. Select **LOOP** and then click **RUN**.
- **Save:** saves the content of the Script Command Window as a .txt file that can be subsequently reloaded
- **Open:** clears the current content and loads a previously saved script into the script command window. The loaded file has to be a TBB file with .txt extension.
- **Clear:** clears the current content of the script command window.
- **Help:** shows a list of all script editor command and their command formats.

Script results window

This window displays the results of an executed script. The menu bar at the bottom of the window contains the following three buttons:

- **Save:** saves the content of the Script Results Window as .txt file that can be subsequently reloaded.
- **Open:** clears the current content and loads a previously saved results file into the script results window.
- **Clear:** clears the current content of the script results window.

5.2.3.3.3 Prog

The Prog tool provides an easy way for OTP fuses burning. This tool contains two sections:

- Device programming configuration: allows you to set configuration parameters.
- Fuse box status:
  - Programming status: shows the status program flags during the burn process.
  - Sector flags: shows the status of the sector flags during the burn process. A blue box next to a sector flag indicates that the sector is empty (has not been burned); an orange flag indicates that the sector has already been burned.

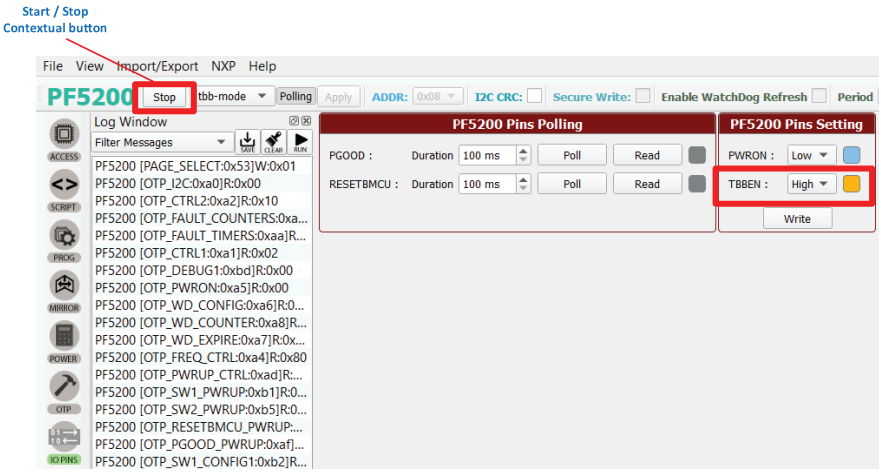
For information on using the Prog tool to burn PF5200 fuses, see Section 6.4 "Programming an OTP operation".

5.2.3.3.4 Mirror

The Mirror tool provides access to all mirror registers.

Note: *The Mirror tool tabs are similar to the corresponding OTP tool tabs.*

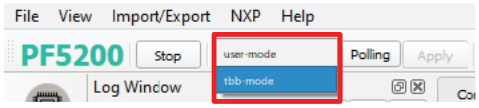
To avoid confusion, the tab header background colors are different. Mirror tool tab headers are brownish-red. OTP tool tab headers are blue.



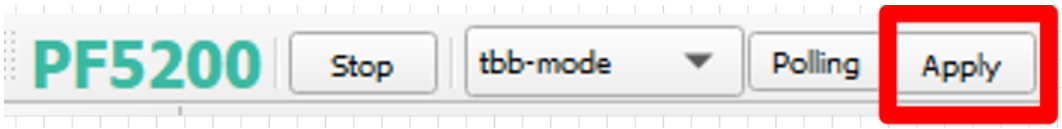
There are two different tbb-mode procedures, depending on whether or not the OTP fuses have already been burned.

Working with a part whose OTP fuses have not yet been burned:

1. Before performing a read or write, be sure you are in tbb-mode. To do so, select **tbb-mode** in the Device Manager menu and click **Apply**.
   This works even if you initially started running in user-mode.



aaa-fig51tmp



2. The usual way of working is to set the PWRON_SEL jumper on the PWRON_MCU side in order to allow the PWRON pin to be controlled by the MCU and the script.

Working with a part whose OTP fuses have already been burned:

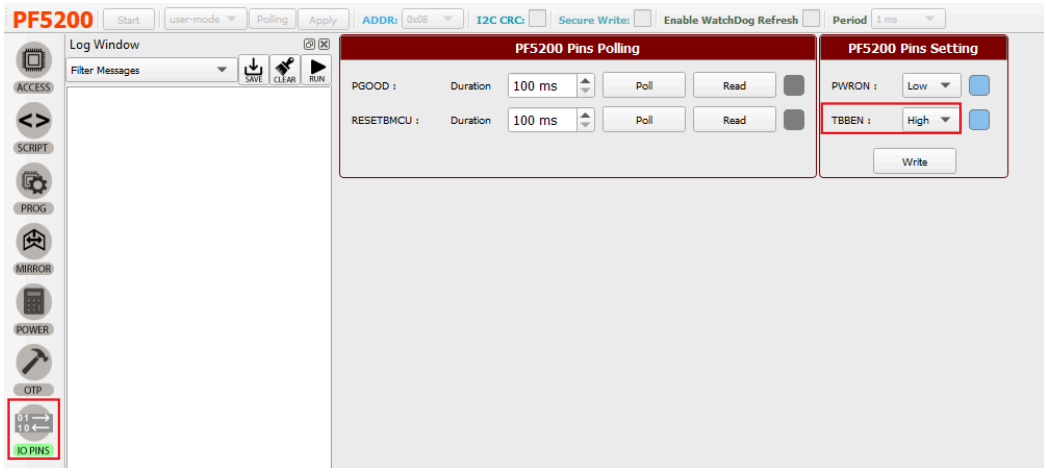
Under these circumstances, a write operation is possible only when the board has first been powered with PWRON set to low. Then the user can read, modify, and when ready, set PWRON to high.

The usual way of working is to set the PWRON_SEL jumper on the PWRON_SW side in order to allow PWRON to be controlled manually by the SW1 switch.

The procedure is as follows:

1. Set the PWRON_SEL jumper to the PWRON_SW position.
2. Move POWERON SW (SW1) to the OFF (0) position.
3. Power the board.

4. Click **IO PINS** button in the Tools access bar. When the IO PINS window appears, set TBBEN high. If TBBEN has already been set high by the MCU, do nothing.



5. Return to the Mirror tool and Read/Write the mirror registers as you require.
6. On the evaluation board, switch SW1 to the On (1) position. The part starts with the modified settings.

The following figure shows the Configuration tab of the Mirror tool.

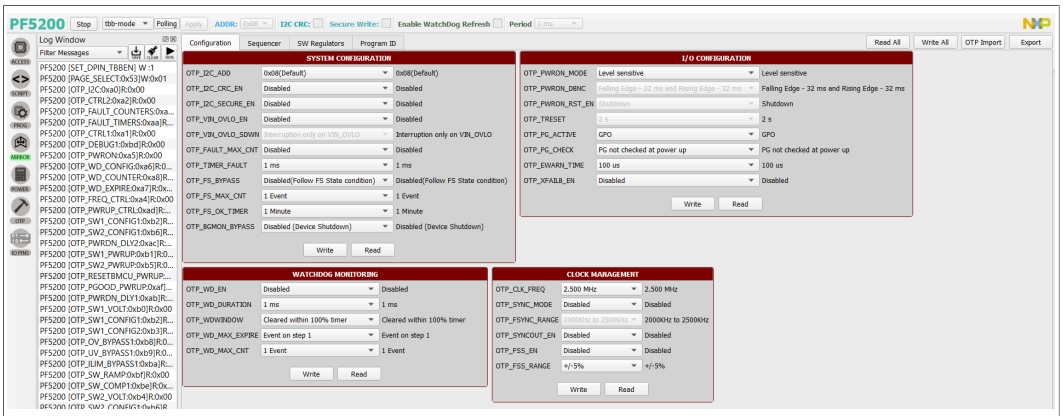


Figure 5. Mirror - Configuration tab

5.2.3.3.5 OTP

The OTP tool allows you to enter an OTP configuration and save it as a .cfg file. The .cfg file is used by the GUI to log all of the configuration information. A TBB file can be created with a .txt extension. The TBB file can be used either to load the mirror registers in TBB mode or to burn OTP fuses using the PROG tool.

The OTP configuration is not addressed here. For information on OTP configuration, see the PF5200 OTP configuration application note.

The main panel of the OTP tool main panel is divided into the four sections shown in Figure 6:

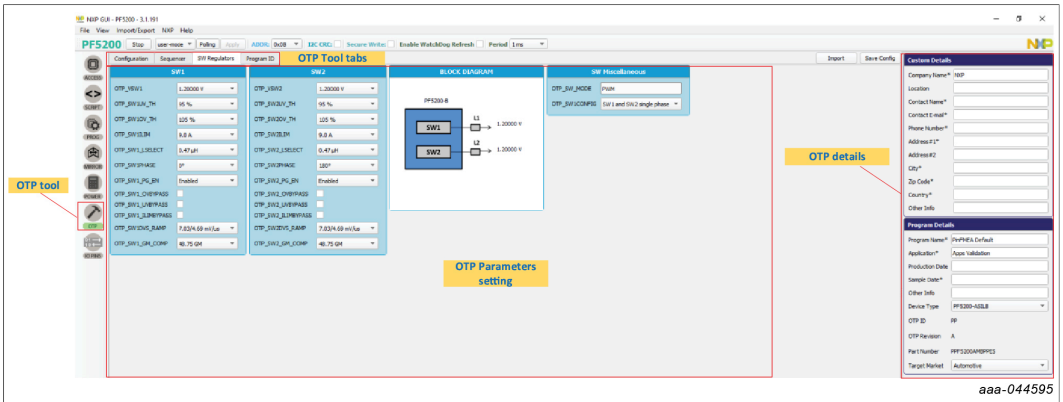
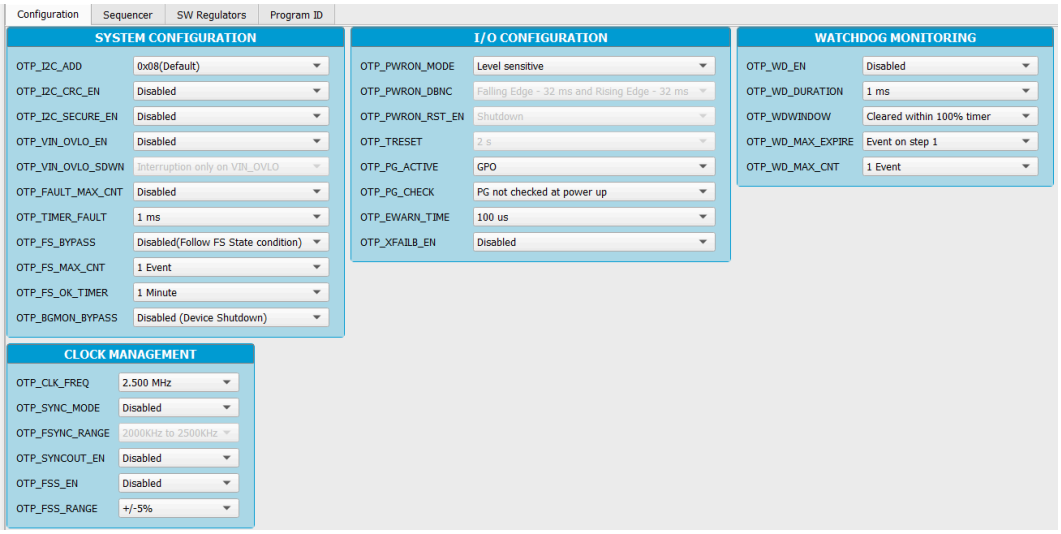
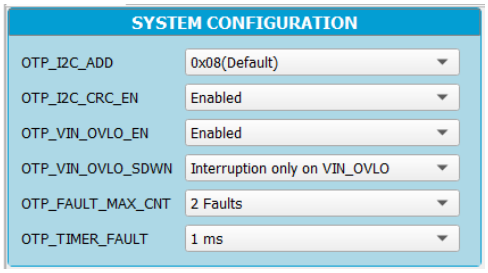


Figure 6. OTP tool main panel sections

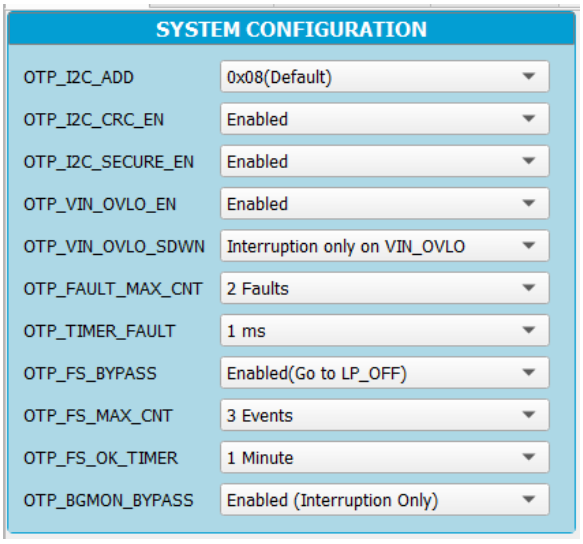
- **OTP parameter setting section:** this section is organized into four tabs.
  - **Configuration tab:** provides a means of setting miscellaneous PF5200 configuration parameters.



The system configuration tab displays a different window, depending on whether a QM device or an ASIL B device has been selected in the Program Details panel.



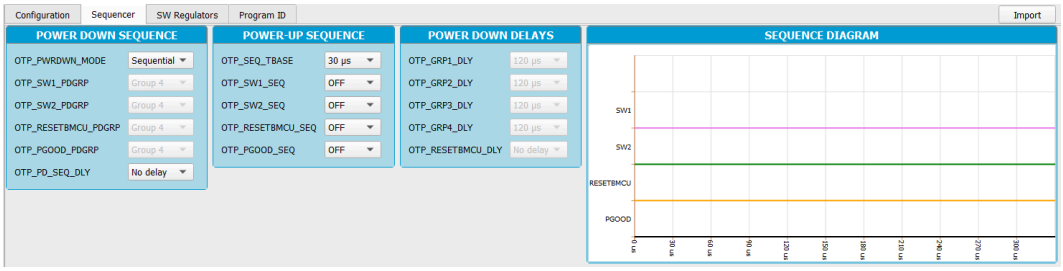
QM System Configuration



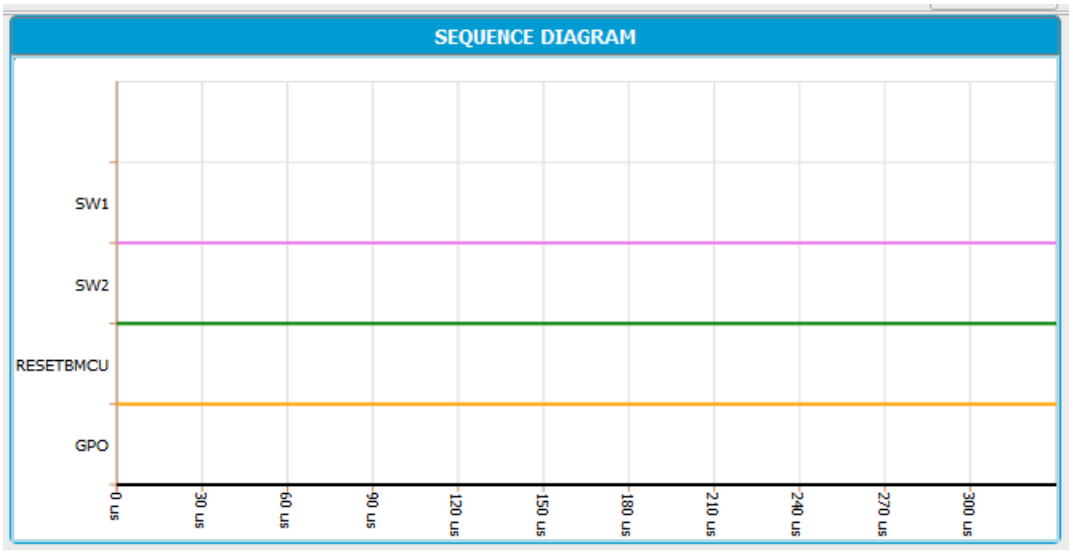
ASIL-B System configuration

  - **Sequencer tab:** configures the sequence and slot for the PGOOD and RESETBMCU switches. Also, allows the power-down mode (OTP_PWRDWN_MODE) to be set for group mode or sequential mode. As shown in

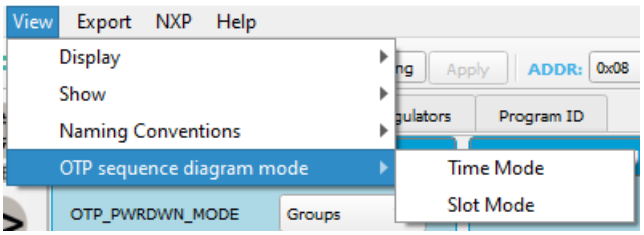
the following figure, some fields are unavailable when OTP_PWRDN_MODE is set to sequential instead group.



The Sequence diagram graph displays the power-up/power-down sequence.

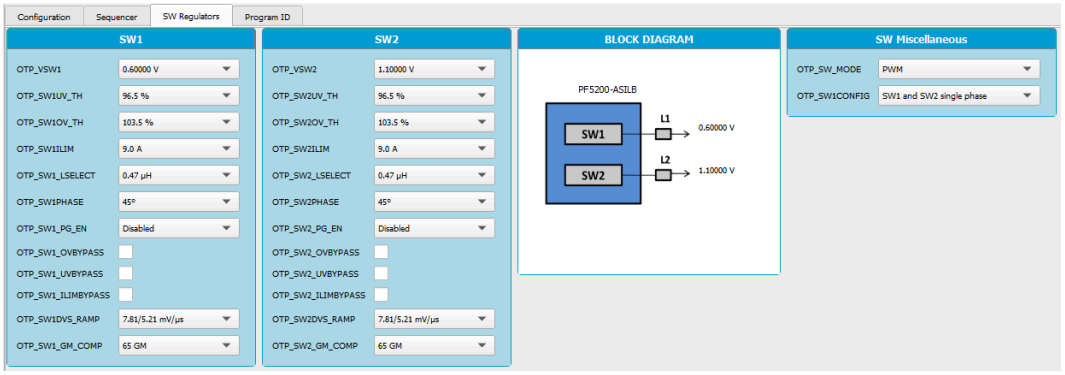


The x-axis of the Sequence diagram can be set to either time mode (displays the sequence in increments of time) or slot mode (displays the sequence in terms of the assigned sequence slots). To change this setting, go to **View / OTP sequence diagram mode** and select the mode.

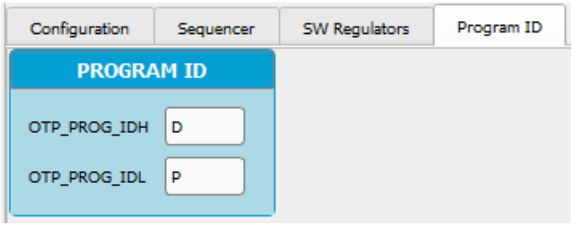


– **SW Regulators tab:** sets OTP Parameters for switcher 1 (SW1) and switcher 2 (SW2). The SW miscellaneous window on the right allows SW1 and SW2 to be configured as single phase or dual phase. The block diagram window displays a block diagram for the current device. Note that, because the PF5200 runs in PWM

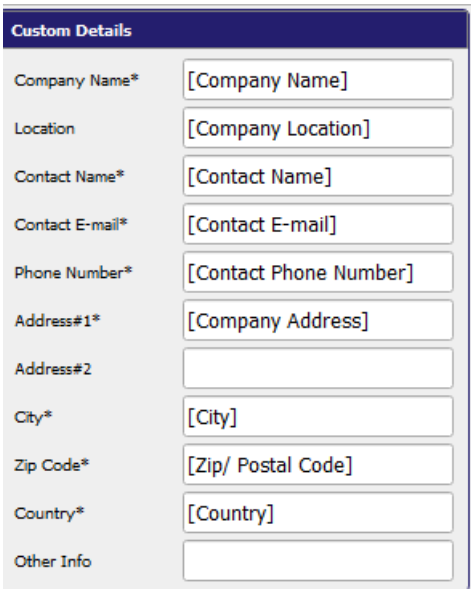
mode only, the OTP_SW_MODE setting in the SW miscellaneous window cannot be changed.



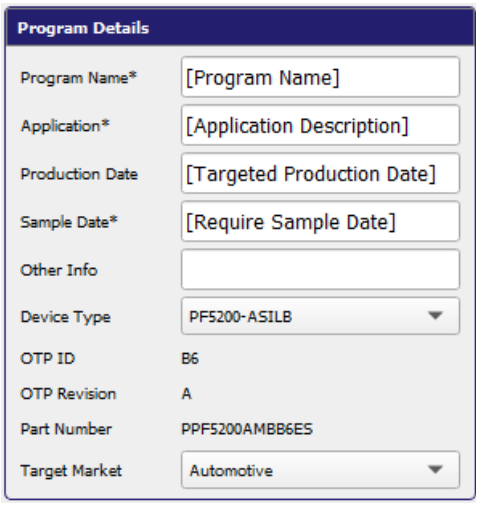
– **Program ID tab:** displays the OTP ID. Only NXP users can create a new OTP ID.



- **OTP Details section:** collects and stores information about the customer and OTP version. All the information entered in this section is retained as part of the .cfg and TBB file.
  - The Custom Details window collects information related to the customer.



  - The Program Details window, in addition to comments related to the application, allows you to do the following:
    - Select device type (see Configuration tab for details).
    - Display the OTP ID (set by NXP only).
    - Display the build part number (set by NXP only).
    - Select target market, either automotive or industrial.



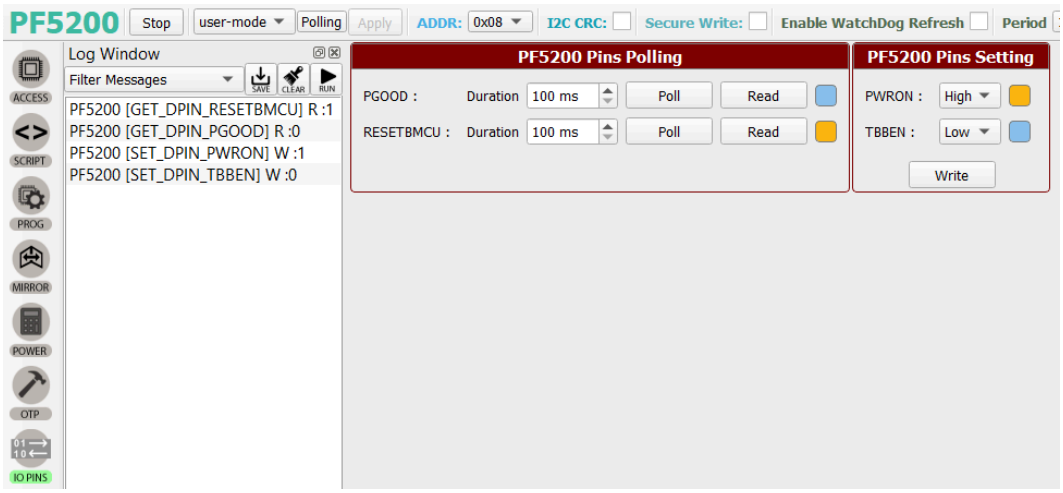
Note: *All other panels, tabs or windows are the same for both QM an ASIL B parts.*

5.2.3.3.6 IO pins

The IO pins tool provides a means of reading and setting the PF5200 IO pins (PGOOD, RESETBMCU, PWRON, TBBEN).

The IO PINS panel consists of three sections:

- **Log window:** maintains a running log of events initiated during the current session. A drop-down menu in the upper left allows the log to be filtered by register read, register write, pin read, and pin write. Buttons in the upper right allow the Log window contents to be saved, cleared, or run.
- **PF5200 pins polling:** allows the PGOOD and RESETBMCU pins to be read or polled during a selected time duration. In the indicator boxes, blue indicates low state, orange indicates high state. The displayed logical level is the last one sent to the device and not an actual sense of the pins.
- **PF5200 pins setting:** allows the PWRON and TBBEN pins to be set. The PGOOD pin must be set as a PGOOD or GPO function and not as a temperature sensor output. In the indicator boxes, blue indicates low state, and orange indicates high state.



You can enter into TBB mode while the part is live. To change to TBB mode, open the Script tool and go to the Mode tab.

5.2.3.4 Tab content

The Tab content window provides access to GUI functions that configure, monitor, and control the PF5200 device during the evaluation session. There are ten tabs:

- Register map
- SW regulators
- Sequence
- Clock
- PMIC config
- Functional safety
- Interrupts
- Status
- PMIC ID

5.2.3.4.1 Register map

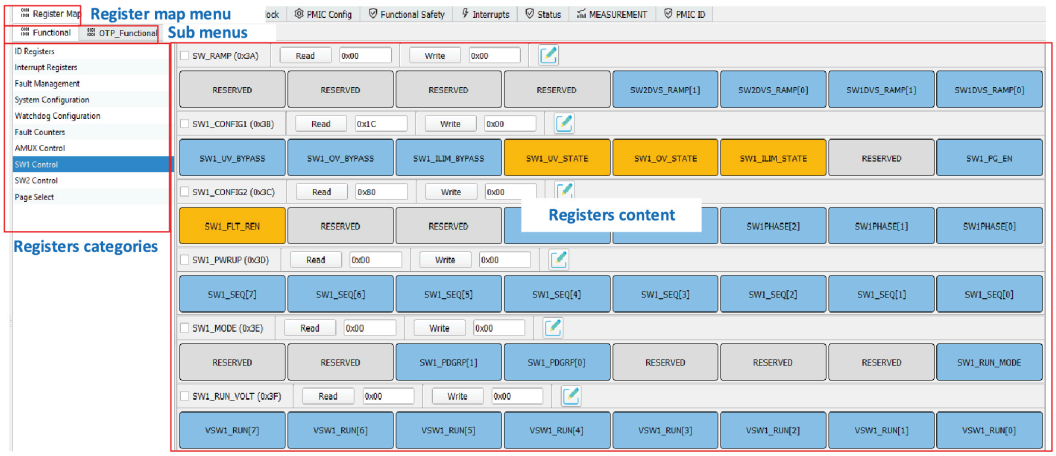
The Register map tab allows you to read or write to the PF5200 registers.

There are two sub-menus:

- **Functional:** functional registers access (I^2C register map)

- **OTP functional:** OTP functional registers access (OTP mirrors register map)

In each submenu, registers are organized by categories in the panel on the left.

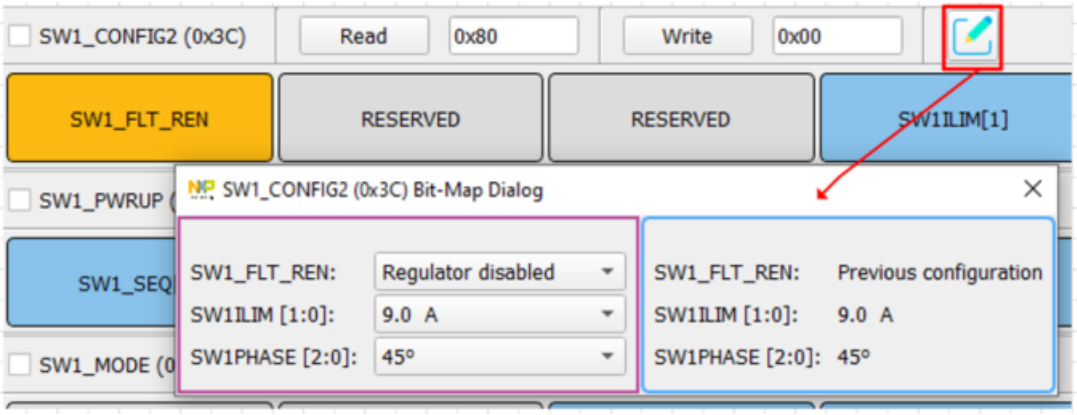


aaa-044596

The PF5200 has two types of registers. Read-only registers (for example, ID registers) appear with a Read button only. Read/Write registers (for example, Interrupt Registers, Fault Management, etc.) appear with both a Read and a Write button.

Clicking **Select All** checkbox in the bottom left side of the register panel allows you to simultaneously read or write to all of the registers in the window. Clicking **Reset** button switches all of the bits in the registers to 0.

To open a window that shows the name and description of all the bit fields in a register, click the green pen icon above the register.



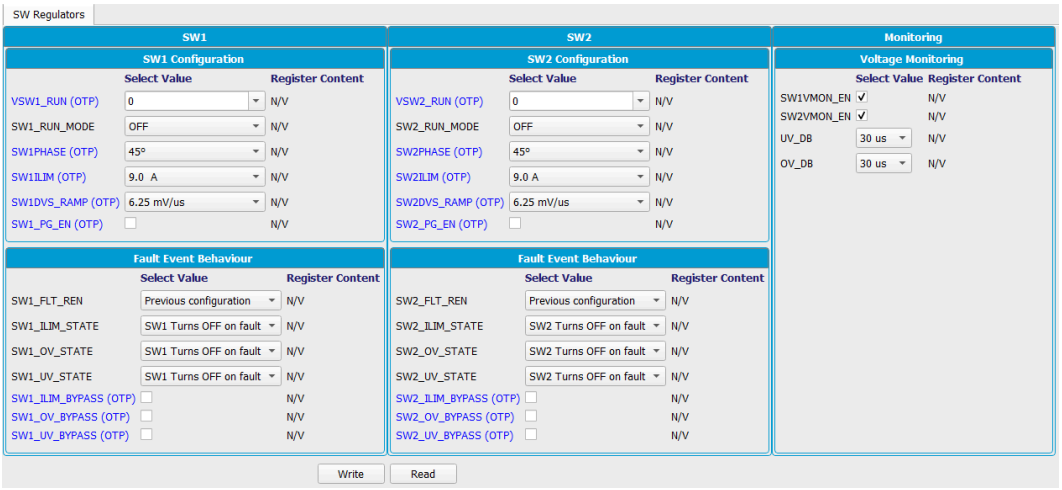
5.2.3.4.2 SW regulators

The SW regulators tab allows you to read and write the parameters related to the SW1 and SW2 regulators. For all graphical panels, register names that appear in blue with a (OTP) suffix are set by OTP and available later in the I^2C register mapping. For example, in the following figure:

VSW_RUN (OTP) is part of OTP and the I^2C functional mapping

SW_RUN_MODE: is available only in the I^2C functional mapping

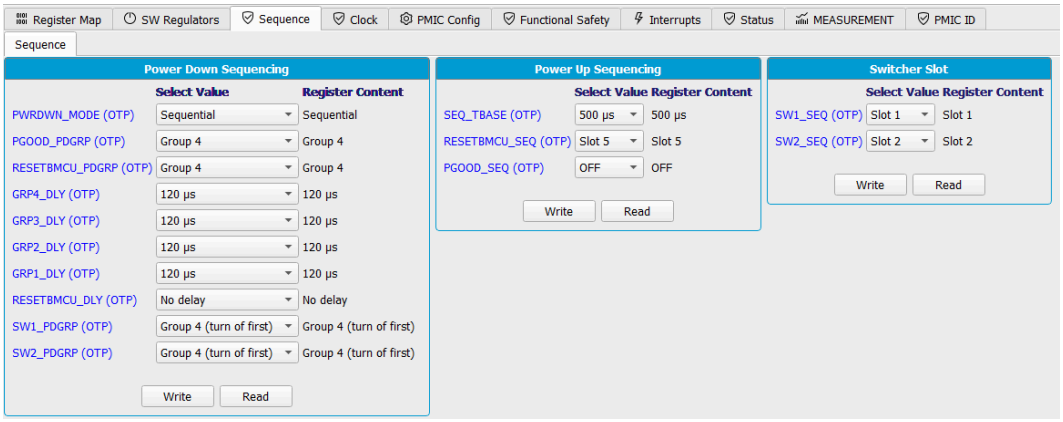
The SW regulators tab gives the main setting of each switch and monitoring configuration.



5.2.3.4.3 Sequence

The Sequence tab sets up the power up/power down sequence and the switcher slot assignments for the device. The tab has three sections:

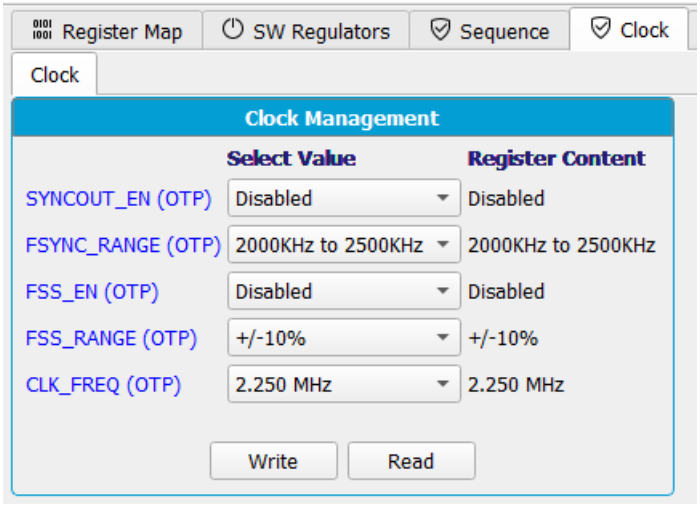
- Power down sequencing: allows you to read or write power down sequencing parameters.
- Power up sequencing: allows you to read or write power up sequencing parameters.
- Switcher slot: allows you to read or write the slots assigned to SW1 and SW2.



5.2.3.4.4 Clock

The Clock tab manages the SYNC pin, switcher clock frequency, and spread spectrum.

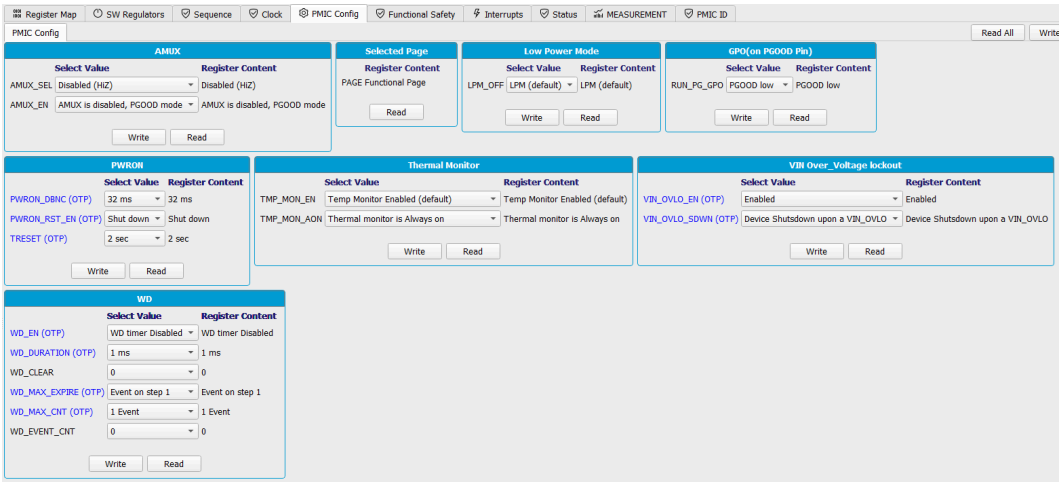
The SYNC pin can be used to either output the switcher frequency or to input the frequency synchronization signal. When SYNCOUT_EN is enabled (SYNC pin is output), FSYNC_RANGE (the SYNC pin used as the synchronization pin) is not usable and therefore is not available.



5.2.3.4.5 PMIC config

The PMIC config tab allows you to manage values related to various functions such as Watchdog, Thermal Monitoring, etc. The PMIC config tab contains the following windows:

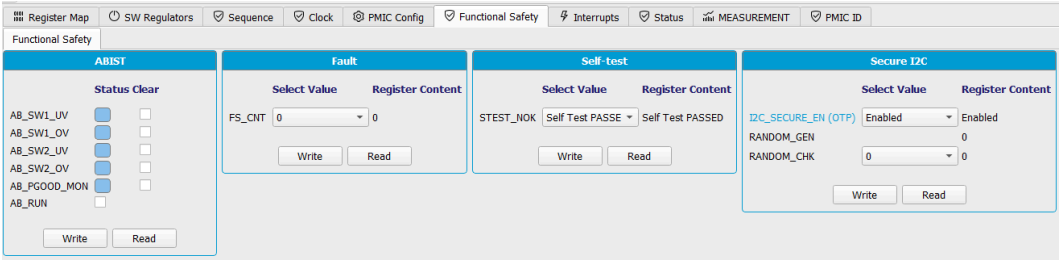
- **AMUX:** sets values for AMUX_SEL and AMUX_EN
- **Selected page:** reads the Page register
- **Low-power mode:** selects the Low-Power mode
- **GPO (on PGOOD pin):** sets PGOOD low or high
- **PWRON:** set PWRON values
- **Thermal monitor:** enables/disables the Thermal Monitor and selects whether the thermal monitor is always-on or whether it is turned on once every millisecond.
- **VIN Over_Voltage_lockout:** enables/disables VIN overvoltage lockout and selects whether an overvoltage triggers an interrupt or a shutdown.
- **WD:** sets up Watchdog parameters



5.2.3.4.6 Functional Safety

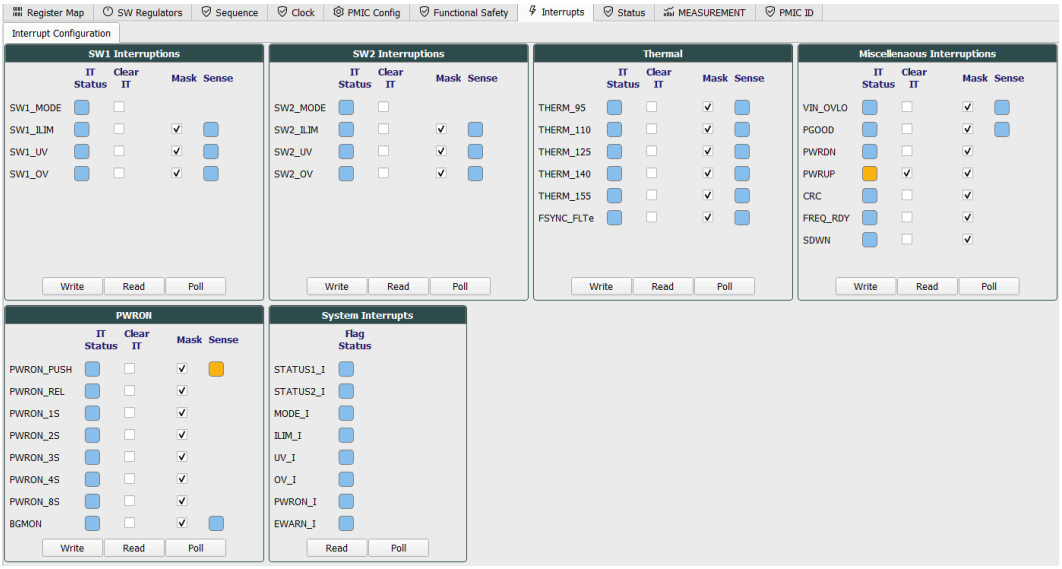
The Functional Safety tab manages ABIST, functional safety fault, self-test status, and secure I^2C.

In ASIL-B, an exhaustive list of bits is available only in the I^2C functional registers.



5.2.3.4.7 Interrupts

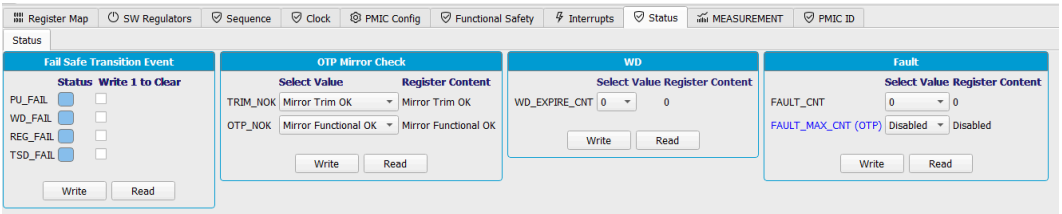
The Interrupts tag displays interrupts by category and allows you to clear or mask selected interrupts.



5.2.3.4.8 Status

The Status tab displays the status of selected functions and allows you to modify their associated values. The tab provides status on the following:

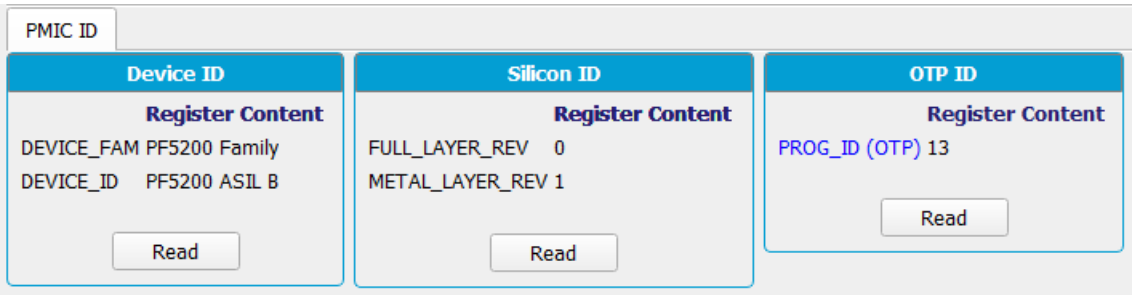
- **Fail-safe Transition Event:** allows you to read or clear Fail-safe hard-fault flags
- **OTP Mirror Check:** allows you to read and modify mirror register test flags
- **WD:** allows you to read and modify the Watchdog expiration counter
- **Fault:** allows you to read and modify the fault counter bit field and to enable/disable the max fault counter



5.2.3.4.9 PMIC ID

The PMIC tab provides basic information regarding the device. It contains three sections:

- **Device ID:** shows the device family and indicates whether the part is trimmed ASIL B or QM.
- **Silicon ID:** shows the revision level of the silicon layers.
- **OTP ID:** shows the OTP version burned in the part.



6 Setting up and running the KITPF5200FRDMEVM

6.1 Setting up the KITPF5200FRDMEVM

The procedure for setting up the KITPF5200FRDMEVM board is as follows:

1. Make sure that the board has the jumper's configured in their default positions as shown in Figure 7. The default configuration enables the board to be fully controlled by the FRDM-KL25Z and the GUI.

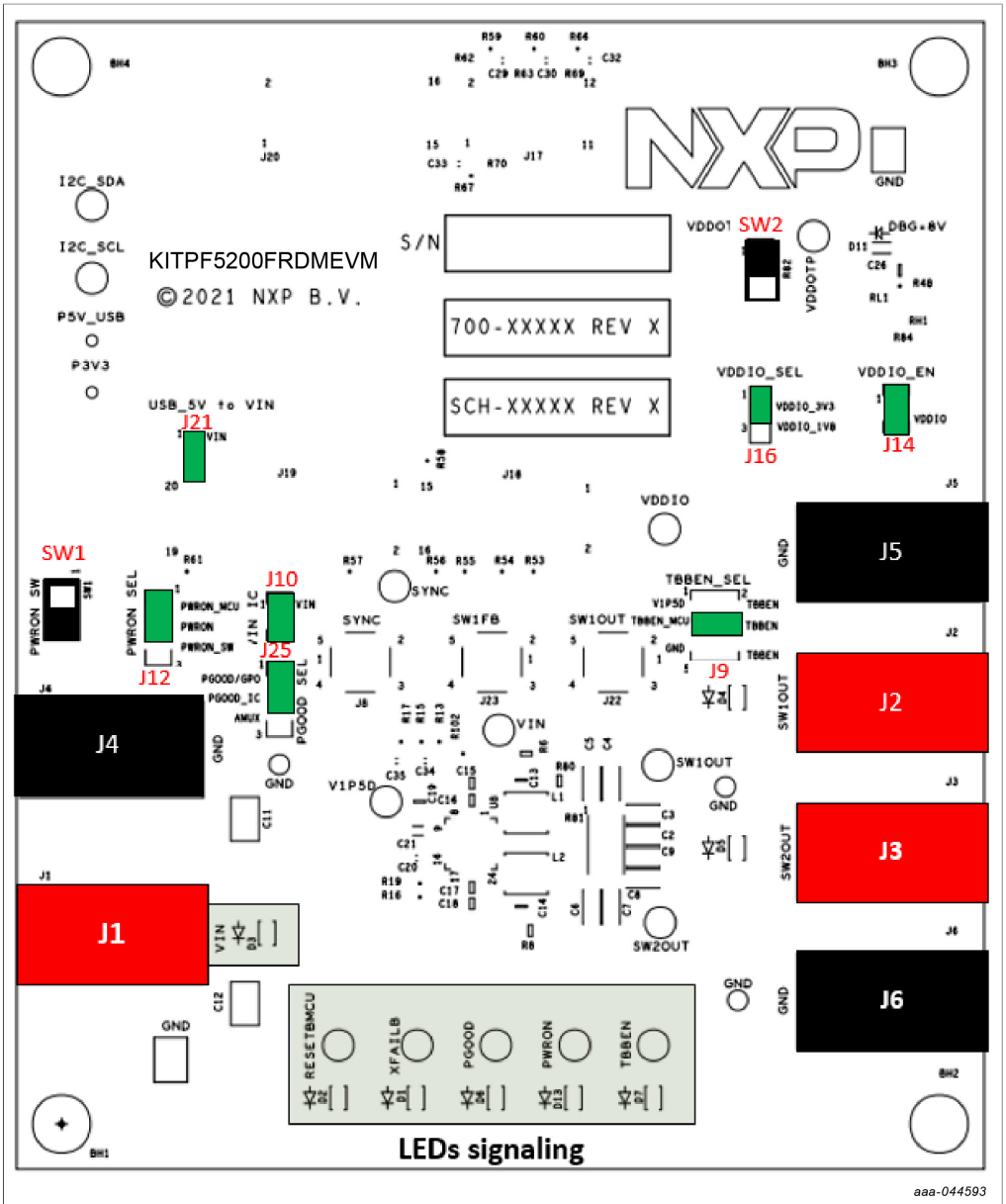


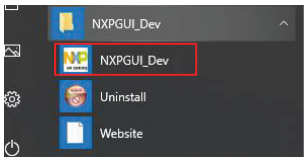
Figure 7. KITPF5200FRDMEVM default jumper configuration

2. Connect the power supply to J1 (VIN) and J4 (GND). The power supply should be set to an initial value of 5.0 V and current limited to 8.0 A.
3. Verify that the FRDM-KL25Z board is firmly mounted to the KITPF5200FRDMEVM board. Also, make sure that the USB cable between the FRDM-KL25Z and the PC is securely connected. This connection is critical because the USB port not only serves as a communication channel between the PC and the FRDM-KL25Z board, but also provides voltages and references to some onboard circuits and generates the VDDIO reference for the IC.

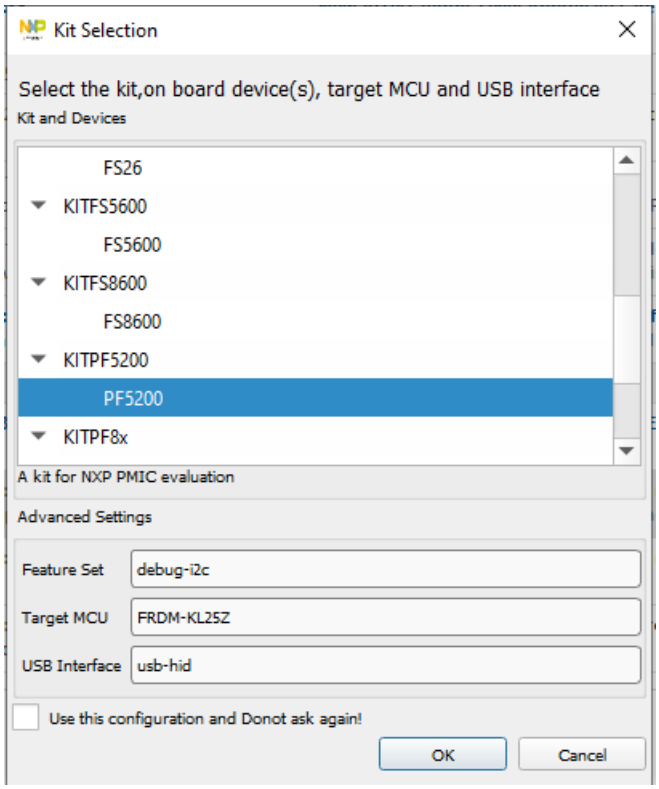
6.2 Connecting the PF5200 to the GUI

The procedure for connecting the PF5200 to the GUI is as follows:

1. Click the Windows icon at the bottom left of the screen and select NXPGUI icon to open the GUI.

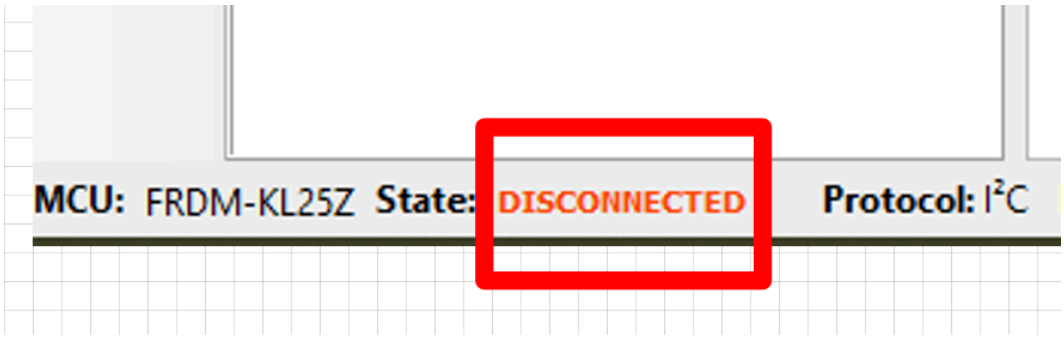


2. When the GUI opens, the Kit Selection window appears. Select PF5200 and click **OK**. Note: If the File menu shows a check mark next to the "Do not display GUI Kit selection at Start" item, the Kit Selection window does not appear at start-up.

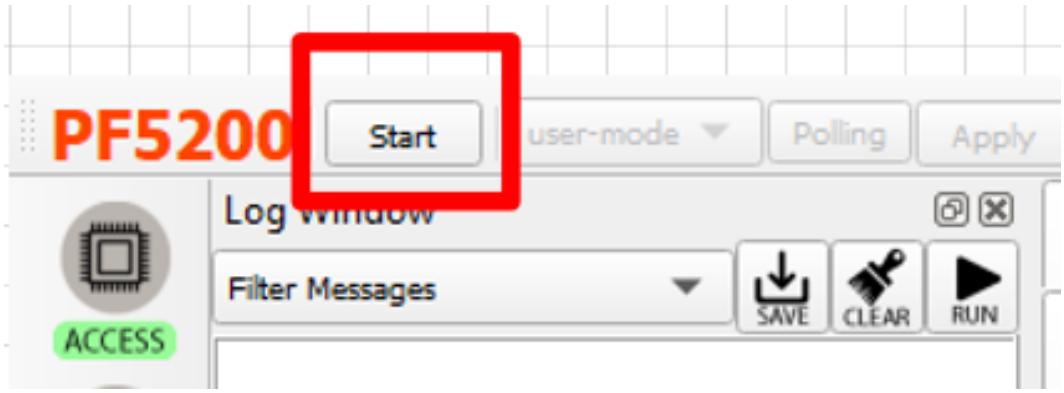


3. In the bar at the bottom of the window, the State message should display "DISCONNECTED". This indicates that the USB cable is plugged in but communication has not yet been established between the FRDM-KL25Z and the

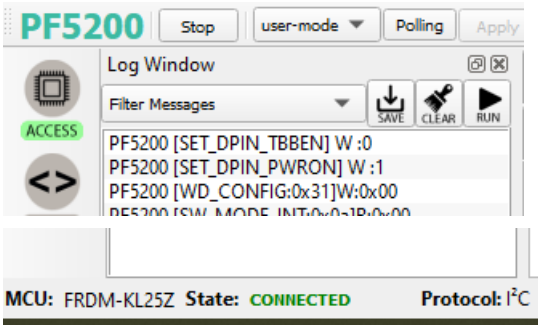
PF5200. If the USB cable is not plugged in, the State message displays "NOT DETECTED".



4. To establish communication between the FRDM- KL25Z and the PF5200 and allow the GUI to take control, click **Start** in the upper left corner.



5. When the GUI gains control, the PF5200 header text in the upper left corner changes from red to green. The State indicator in the bottom left displays CONNECTED and initial events appear in the Log Window.



6.3 Programing a TBB operation

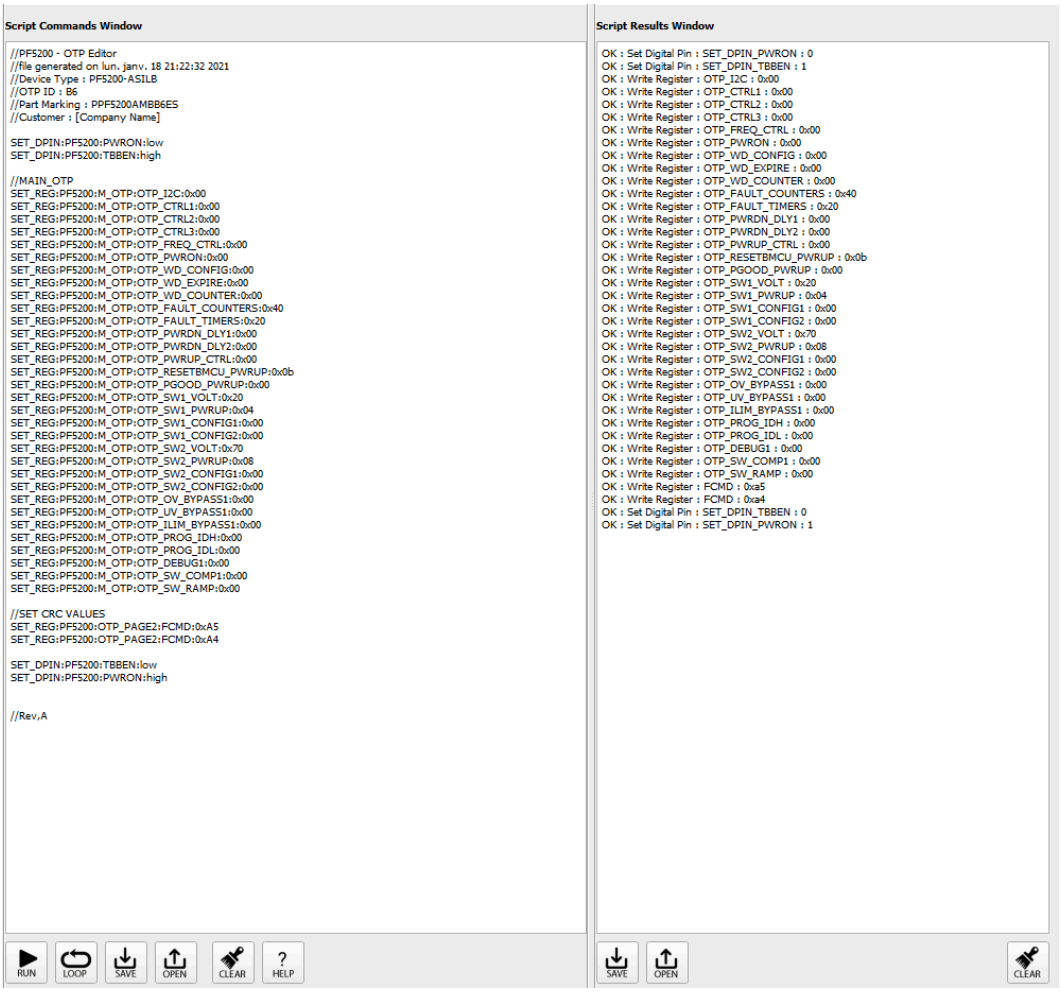
The Try Before Buy (TBB) operation allows you to create and test a preliminary version of a desired configuration in the mirror registers prior to submitting the configuration to the OTP fuse burning process. The TBB configuration is activated in the PF5200 as soon as PWRON goes active (assuming VIN is above VIN_UV).

1. To configure the mirror registers, use the Script tool (see Section 5.2.3.3.2 "Script") to load and execute the TBB script file. In the bar at the bottom of the Script Command

Window, click **OPEN** to load the TBB script file into the Script Command Window. Note that the script file must have a “PF5200” prefix. You can also copy and paste the script file in Section 6.5 "OTP script example" as a trial operation.

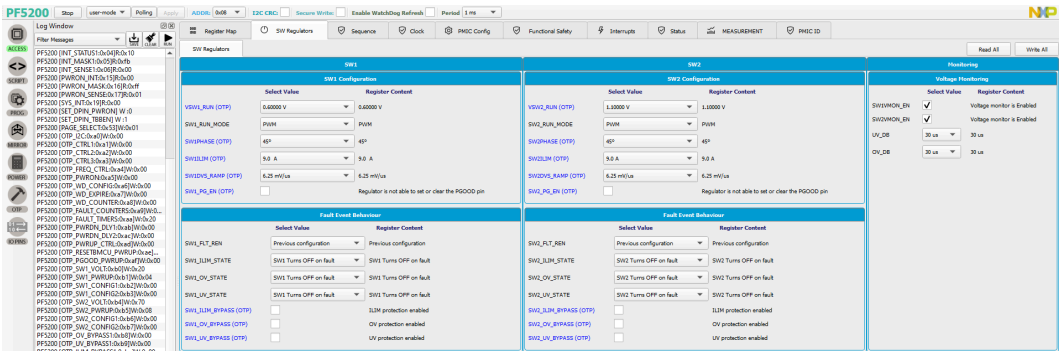
2. To execute the TBB script, click **RUN** in the bar at the bottom of the Script Command Window.

3. When the script execution completes, the Script panel appears as shown below. The Script Command Window displays the TBB script and Script Results Window shows the results after execution. The FRDM-KL25Z automatically controls the TBBEN and PWRON pins, so no further action is required on your part.



At this point, the PGOOD and RESETBMCU LEDs should be lit on the KITPF5200FRDMEVM board, indicating that the PGOOD and RESETBMCU pins have been released.

As a cross-check, open the Access tool and check the fields in the SW Regulators tab. If the operation completed without problems, all fields should appear as expected.

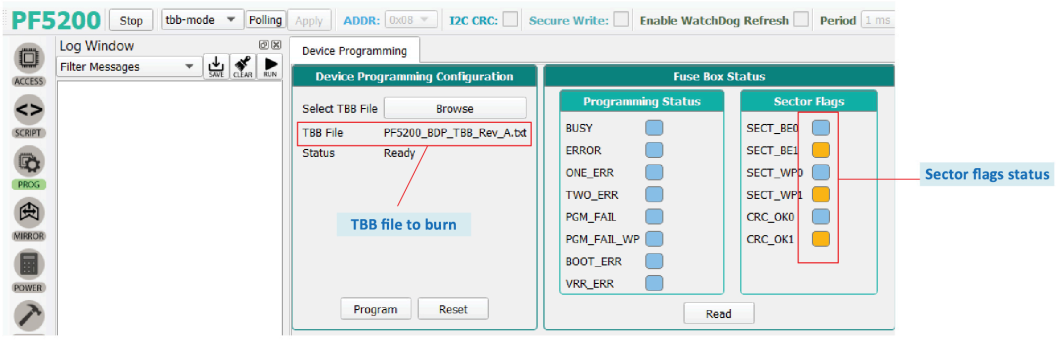


6.4 Programming an OTP operation

The PROG tool (Section 5.2.3.3.3 "Prog") is used to execute the OTP script and burn the PF5200 fuses. The OTP script can be the same one created and tested in Section 6.3 "Programing a TBB operation". There is no need to create another file specifically for OTP. Like the TBB file, the OTP file must have "PF5200" as the prefix.

Part Requirement:

A PF5200 device can be burned only once. Make sure that the socket contains a device that has not yet been burned before starting the burn process. To do so, open the PROG tool and check the flags in the Sector Flags section. If the SECT_BE0, SECT_WP0, and CRC_OK0 flags are set at 0 (blue), the device is empty and capable of being burned. Once the part is burned, all sectors flags are set to 1 (orange).



aaa-044597

PF5200 Programming interface (empty part shown here)

Programing procedure:

1. Insert the part into the socket.
2. Plug in the USB cable and connect the power supply.
3. Load the TBB file.
4. Click **Program**.

Two pop-up windows appear. Follow the instructions in the pop-ups:

- The first pop-up instructs you to apply 8.0 V on TP12. When done, the blue LED on the board lights up.
- When the burn process completes successfully, the second pop-up instructs you to remove the 8.0 V on TP12.

6.5 OTP script example

This section contains an example of a complete OTP script that can be load and executed.

```
//PF5200 - OTP Editor
//file generated on lun. janv. 18 21:22:32 2021
//Device Type : PF5200-ASILB
//OTP ID : B6
//Part Marking : PPF5200AMBB6ES
//Customer : [Company Name]
SET_DPIN:PF5200:PWRON:low
SET_DPIN:PF5200:TBBEN:high
//MAIN_OTP
SET_REG:PF5200:M_OTP:OTP_I2C:0x00
SET_REG:PF5200:M_OTP:OTP_CTRL1:0x00
SET_REG:PF5200:M_OTP:OTP_CTRL2:0x00
SET_REG:PF5200:M_OTP:OTP_CTRL3:0x00
SET_REG:PF5200:M_OTP:OTP_FREQ_CTRL:0x00
SET_REG:PF5200:M_OTP:OTP_PWRON:0x00
SET_REG:PF5200:M_OTP:OTP_WD_CONFIG:0x00
SET_REG:PF5200:M_OTP:OTP_WD_EXPIRE:0x00
SET_REG:PF5200:M_OTP:OTP_WD_COUNTER:0x00
SET_REG:PF5200:M_OTP:OTP_FAULT_COUNTERS:0x40
SET_REG:PF5200:M_OTP:OTP_FAULT_TIMERS:0x20
SET_REG:PF5200:M_OTP:OTP_PWRDN_DLY1:0x00
SET_REG:PF5200:M_OTP:OTP_PWRDN_DLY2:0x00
SET_REG:PF5200:M_OTP:OTP_PWRUP_CTRL:0x00
SET_REG:PF5200:M_OTP:OTP_RESETBMCU_PWRUP:0x0b
SET_REG:PF5200:M_OTP:OTP_PGOOD_PWRUP:0x00
SET_REG:PF5200:M_OTP:OTP_SW1_VOLT:0x20
SET_REG:PF5200:M_OTP:OTP_SW1_PWRUP:0x04
SET_REG:PF5200:M_OTP:OTP_SW1_CONFIG1:0x00
SET_REG:PF5200:M_OTP:OTP_SW1_CONFIG2:0x00
SET_REG:PF5200:M_OTP:OTP_SW2_VOLT:0x70
SET_REG:PF5200:M_OTP:OTP_SW2_PWRUP:0x08
SET_REG:PF5200:M_OTP:OTP_SW2_CONFIG1:0x00
SET_REG:PF5200:M_OTP:OTP_SW2_CONFIG2:0x00
```

SET_REG:PF5200:M_OTP:OTP_OV_BYPASS1:0x00

SET_REG:PF5200:M_OTP:OTP_UV_BYPASS1:0x00

SET_REG:PF5200:M_OTP:OTP_ILIM_BYPASS1:0x00

SET_REG:PF5200:M_OTP:OTP_PROG_IDH:0x00

SET_REG:PF5200:M_OTP:OTP_PROG_IDL:0x00

SET_REG:PF5200:M_OTP:OTP_DEBUG1:0x00

SET_REG:PF5200:M_OTP:OTP_SW_COMP1:0x00

SET_REG:PF5200:M_OTP:OTP_SW_RAMP:0x00

//SET CRC VALUES

SET_REG:PF5200:OTP_PAGE2:FCMD:0xA5

SET_REG:PF5200:OTP_PAGE2:FCMD:0xA4

SET_DPIN:PF5200:TBBEN:low

SET_DPIN:PF5200:PWRON:high

7 References

[1] **PF5200** — detailed information on PF5200, Dual-Channel PMIC for Automotive Applications – 2 High Efficient LVBUCK, Fit for ASIL B Safety Level
http://www.nxp.com/PF5200

[2] **KITPF5200FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITPF5200FRDMEVM

[3] **NXP GUI for Automotive PMIC Families** — Software GUI for NXP's Automotive PMIC products
https://www.nxp.com/PMIC-GUI-SW

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Date of release: 8 December 2021
Document identifier: UM11723

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