UM11603

RDGD31603PHSEVM three-phase inverter reference design

Rev. 1 — 18 August 2021 User manual

Document information

Information	Content
Keywords	GD3160, gate, driver, power, inverter, Automotive
Abstract	The RDGD31603PHSEVM three-phase inverter is a functional hardware power inverter reference design, which can be used as a foundation to develop a complete ASIL-D compliant high voltage, high-power traction motor inverter for electric vehicles.

Revision history

Revision history

Rev	Date	Description
v.1	20210818	Initial version

Important notice

NXP provides the enclosed product(s) under the following conditions:

This reference design is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This reference design may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The goods provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end product incorporating the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. In order to minimize risks associated with the customers applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

1 Introduction

This document is the user guide for the RDGD31603PHSEVM reference design. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of single-channel gate driver for IGBT/SiC, GD3160. The scope of this document is to provide the user with information to evaluate the single channel gate driver for IGBT/SiC, GD3160. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The RDGD31603PHSEVM is a fully functional three-phase inverter evaluation board populated with six GD3160 gate drivers with fault management and supporting circuitry. This board supports SPI daisy chain communication for programming and communication with three high-side gate drivers and three low-side gate drivers independently.

This board has low-voltage and high-voltage isolation in conjunction with gate drive integrated galvanic signal isolation. Other supporting features on the board include desaturation short-circuit detection, IGBT/SiC temperature sensing, DC Link bus voltage monitoring, phase current sensing, and motor resolver excitation and signal processing connection circuitry. See GD3160 data sheet for additional gate drive features.

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this reference design and its supported device(s) on http://www.nxp.com.

The information page for RDGD31603PHSEVM reference design is at http://www.nxp.com/RDGD31603PHSEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the RDGD31603PHSEVM reference design, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the RDGD31603PHSEVM requires kit contents and a Windows PC workstation with FlexGUI software installed.

3.1 Kit contents

- Assembled and tested RDGD31603PHSEVM (three-phase inverter populated with 5.0 V compatible gate driver devices) board in an anti-static bag
- 3.3 V to 5.0 V translator board connected to FRDM-KL25Z MCU (KITGD3160TREVB) with micro-USB cable for using FlexGUI software control
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this reference board.

- Microcontroller for SPI communication
- Compatible SiC MOSFET module
- DC link capacitor compatible with SiC (VE-Trac SiC from OnSemi NVXR17S90M2SP or ST SiC) MOSFET module
- HV power supply with protection shield and hearing protection
- Current sensors for monitoring each phase current
- 12 V, 1.0 A DC power supply
- 4-channel oscilloscope with appropriate isolated probes

3.3 Windows PC workstation

This reference design requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 8 or Windows 10

3.4 Software

Installing software is necessary to work with this reference design. All listed software is available on the information page at http://www.nxp.com/RDGD31603PHSEVM.

- Flex GUI software for using with KITGD3160TREVB MCU/translator board
- S32S Design Studio IDE for power architecture
- Automotive Math and Motor Control Library (AMMCL)
- FreeMaster 2.0 runtime debugging tool
- Motor Control Application Tuning (MCAT)
- Example code, GD3160 Device Driver notes and GD31xx Device Driver Reference

4 Getting to know the hardware

4.1 RDGD31603PHSEVM features

- Capability to perform double pulse and short-circuit tests on Phase U using KITGD3160TREVB and FlexGUI. See Phase U schematics and FlexGUI Pulse tab (Figure 32 and Figure 33).
- Evaluation board designed for and populated with GD3160 Gate Drivers and protection circuitry
- Capability to connect to Hybrid Drive type SiC specific modules for full three-phase evaluation and development (see Figure 8 for specific module pin placement)
- Daisy chain SPI communication (three high-side and three low-side gate drivers)
- Variable fly-back VCC power supply with GND reference and -3.9 V VEE supply
- Easy access power, ground, and signal test points
- 2×32 PCIe socket for interfacing MCU control (MPC5775B/E-EVB, MPC5777C-DEVB or MPC57744P). See Figure 34 and Figure 35.
- Optional connection for DC bus voltage monitoring
- Phase current feedback connections

- Resolver signal connector

4.2 Kit featured components

4.2.1 Voltage domains, GD3160 pinout, logic header, and IGBT pinout

Low-voltage domain is an externally supplied 12 V DC (VPWR) primary supply for non-isolated circuits, typically supplied by vehicle battery. The low-voltage domain includes the interface between the MCU and GD3160 control registers and logic control.

Low-side driver and high-side driver domains are isolated high-voltage driver control domains for SiC MOSFET or IGBT single phase connections and control circuits. Pins on bottom of board are designed to easily connect to a compatible three-phase SiC MOSFET or IGBT module.

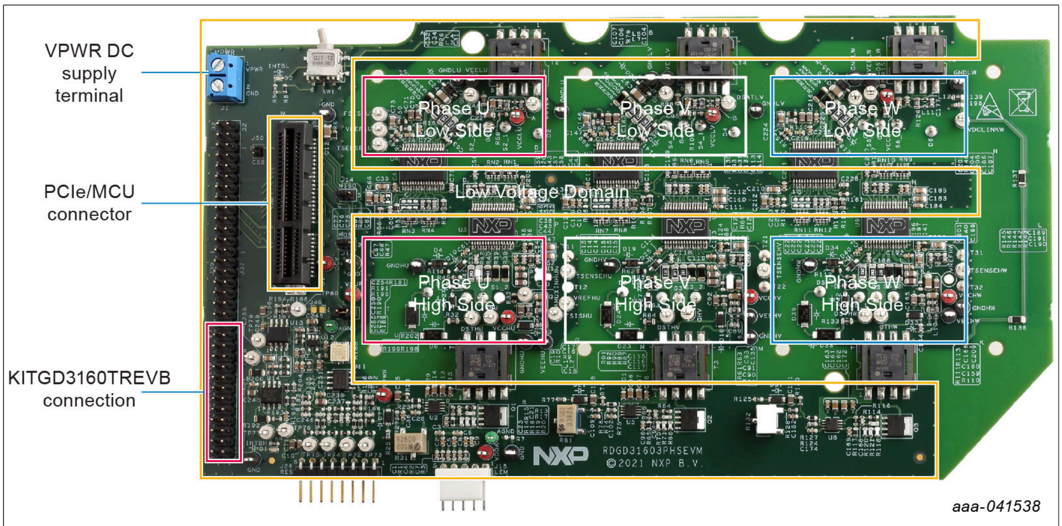


Figure 1. RDGD31603PHSEVM three-phase inverter board voltage domains and interfaces

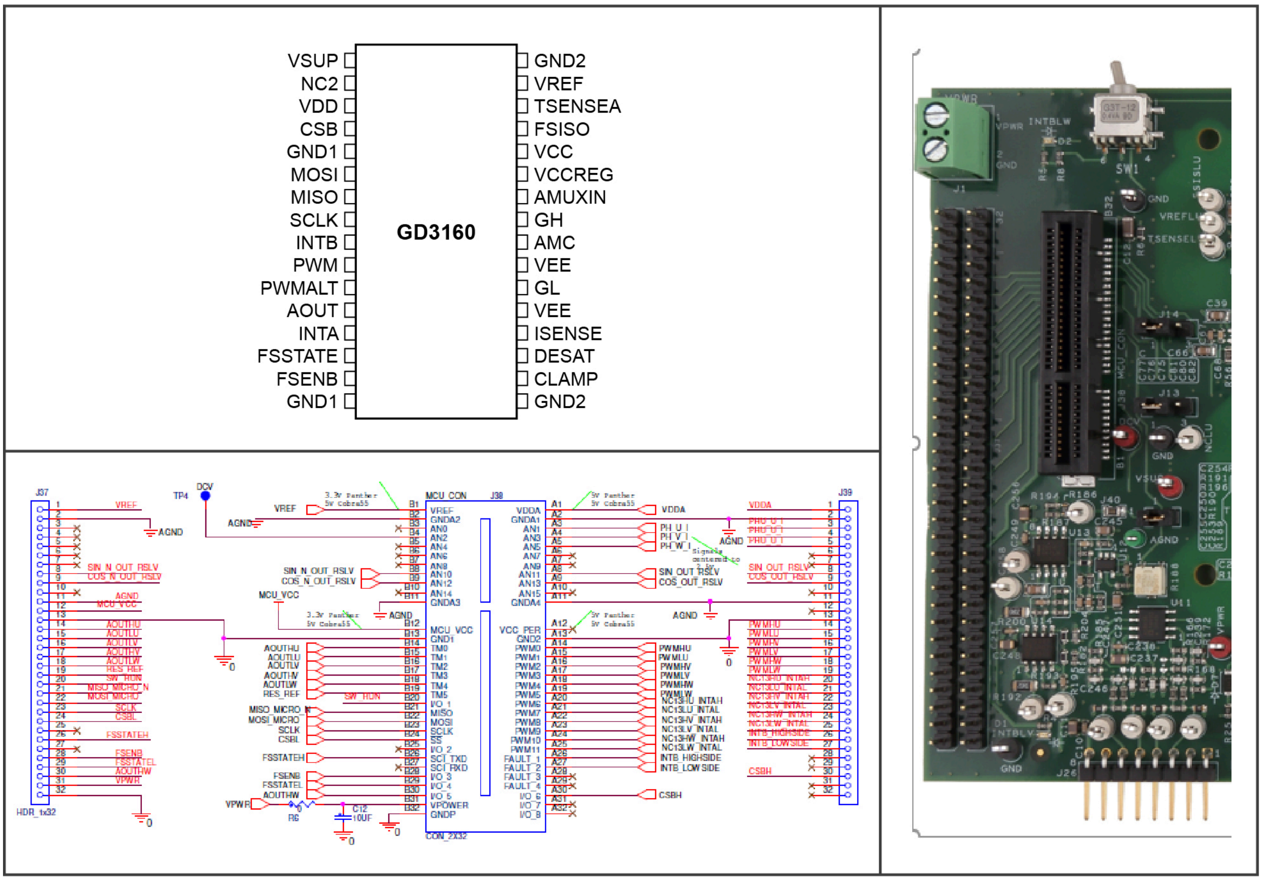
4.2.2 GD3160 pinout and MCU interface pinout

See GD3160 advanced IGBT/SiC gate driver data sheet for specific information about pinout, pin descriptions, specifications, and operating modes. VSUP/VPWR DC supply terminal is a low voltage input connection for supplying power to the low voltage non-isolated die and related circuitry. Typically supplied by vehicle battery +12 V DC.

MCU connector is a 2×32-pin PCIe interface connector for use with either MPC5775B/E-EVB or MPC5744P or MPC5777C 32-bit MCU board or any other MCU of preference. An MCU is needed for SPI communication and control of advanced IGBT/SiC gate drive devices (GD3160).

KITGD3160TREVB included with the kit can be attached to this board at bottom of dual row header pin interface. All gate drivers can be accessed via SPI control using FlexGUI software.

Note: *Double pulse and short-circuit tests can be conducted on Phase U only. See FlexGUI Pulse tab, see* [Figure 32](#) *and* [Figure 33](#)*.*



aaa-041541

Figure 2. Gate driver pinout and board interface connection PCIe 2×32

Table 1. PCIe connector pin definitions

Pin	Name	Function
A1	VDDA	Voltage reference resolver circuit
A2	GNDA1	Analog ground
A3	PH_U_I	Current feedback phase U
A4	PH_V_I	Current feedback phase V
A5	PH_W_I	Current feedback phase W
A6	n.c.	not connected
A7	n.c.	not connected
A8	SIN_OUT_RSLV	Sine resolver signal
A9	COS_OUT_RSLV	Cosine resolver signal
A10	n.c.	not connected
A11	GNDA4	Analog ground
A12	VCC_PER	5.0 V MCU not connected
A13	GND2	Ground
A14	PWMHU	Pulse width modulation high-side phase U
A15	PWMLU	Pulse width modulation low-side phase U
A16	PWMHV	Pulse width modulation high-side phase V

Table 1. PCIe connector pin definitions*...continued*

Pin	Name	Function
A17	PWMLV	Pulse width modulation low-side phase V
A18	PWMHW	Pulse width modulation high-side phase W
A19	PWMLW	Pulse width modulation low-side phase W
A20	HU_INTAH	GD3160 fault reporting/monitoring pin for high-side phase U
A21	LU_INTAL	GD3160 fault reporting/monitoring pin for low-side phase U
A22	HV_INTAH	Analog output signal high-side phase W
A23	LV_INTAL	GD3160 fault reporting/monitoring pin for high-side phase V
A24	HW_INTAH	GD3160 fault reporting/monitoring pin for high-side phase W
A25	LW_INTAL	GD3160 fault reporting/monitoring pin for low-side phase W
A26	INTB_HIGHSIDE	GD3160 fault reporting for high-side gate drive devices
A27	INTB_LOWSIDE	GD3160 fault reporting for low-side gate drive devices
A28	n.c.	not connected
A29	n.c.	not connected
A30	CSBH	Chip select bar to high gate drive devices
A31	n.c.	not connected
A32	n.c.	not connected
B1	VREF	Voltage reference from MCU
B2	GNDA2	Analog ground
B3	n.c.	not connected
B4	DCV	Optional DC bus voltage monitoring (not used by default)
B5	n.c.	not connected
B6	n.c.	not connected
B7	n.c.	not connected
B8	SIN_N_OUT_RSLV	Sine resolver signal
B9	COS_N_OUT_RSLV	Cosine resolver signal
B10	n.c.	not connected
B11	GNDA3	Analog ground
B12	MCU_VCC	MCU VCC regulator voltage
B13	GND1	Ground
B14	AOUTHU	GD3160 analog output signal high-side U phase
B15	AOUTLU	GD3160 analog output signal low-side U phase
B16	AOUTLV	GD3160 analog output signal low-side V phase
B17	AOUTHV	GD3160 analog output signal high-side V phase
B18	AOUTLW	GD3160 analog output signal low-side W phase
B19	RES_REF	Resolver reference voltage
B20	SW_RUN	Signal from onboard switch demo mode
B21	MISO_MICRO	SPI slave out signal
B22	MOSI_MICRO	SPI slave in signal
B23	SCLK	SPI clock
B24	CSBL	Chip select bar to low-side gate drivers

Table 1. PCIe connector pin definitions...*continued*

Pin	Name	Function
B25	n.c.	not connected
B26	FSSTATEH	not connected
B27	n.c.	not connected
B28	FSENB	Fail-safe state enable bar
B29	FSSTATEL	Fail-safe state low-side
B30	AOUTHW	GD3160 analog output signal high-side W phase
B31	VPWR	VPWR/VSUP 12 V voltage supply (low voltage domain)
B32	GNDP	Ground connection (low voltage domain)

4.2.3 Test points

All test points are clearly marked on the board. The following figure shows the location of various test points.

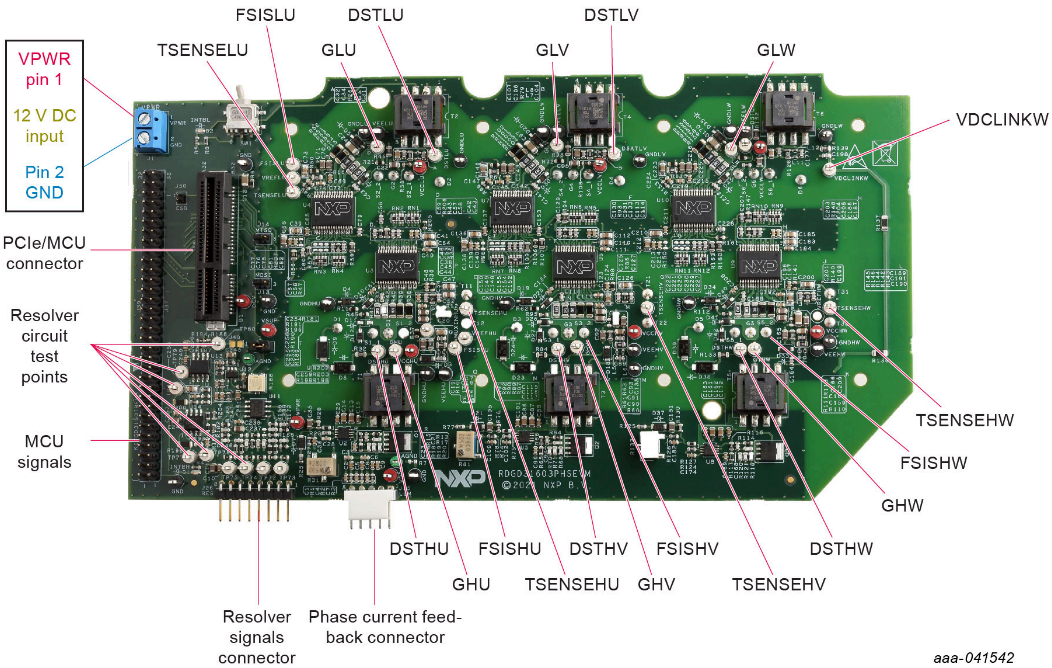


Figure 3. RDGD31603PHSEVM test points

Table 2. Test points

Test point name	Function
DCV	Micro DC voltage
DSTHU	DESAT high-side U phase V_{CE} desaturation connected to DESAT pin circuitry
DSTHV	DESAT high-side V phase V_{CE} desaturation connected to DESAT pin circuitry
DSTHW	DESAT high-side W phase V_{CE} desaturation connected to DESAT pin circuitry
DSTLU	DESAT low-side U phase V_{CE} desaturation connected to DESAT pin circuitry
DSTLV	DESAT low-side V phase V_{CE} desaturation connected to DESAT pin circuitry
DSTLW	DESAT low-side W phase V_{CE} desaturation connected to DESAT pin circuitry
FSISHU	FSISO connection

Table 2. Test points*...continued*

Test point name	Function
FSISHV	FSISO connection
FSISLU	FSISO connection
FSISLV	FSISO connection
FSISLW	FSISO connection
GHU	Gate high-side U phase which is the charging pin of IGBT gate
GHV	Gate high-side V phase which is the charging pin of IGBT gate
GHW	Gate high-side W phase which is the charging pin of IGBT gate
GLU	Gate low-side U phase which is the charging pin of IGBT gate
GLV	Gate low-side V phase which is the charging pin of IGBT gate
GLW	Gate low-side W phase which is the charging pin of IGBT gate
NCLU – NCHW	INTA Interrupt output signal test points from each gate driver
Resolver circuit	Test points for internal signals of resolver circuit (see schematic for more information)
MCU signals	Signal headers for analyzing all MCU signals (see schematic for signals)
TSENSEHU	TSENSE high-side U phase connected to NTC temperature sense
TSENSEHV	TSENSE high-side V phase connected to NTC temperature sense
TSENSEHW	TSENSE high-side W phase connected to NTC temperature sense
TSENSELU	TSENSE low-side U phase
TSENSELV	TSENSE low-side V phase
TSENSELW	TSENSE low-side W phase
VREFLU	5.0 V reference voltage test point low-side U phase
VREFHU	5.0 V reference voltage test point high-side U phase
VREFLV	5.0 V reference voltage test point low-side V phase
VREFHV	5.0 V reference voltage test point high-side V phase
VREFLW	5.0 V reference voltage test point low-side W phase
VREFHW	5.0 V reference voltage test point high-side W phase
VSUP	VSUP/VPWR test point low voltage domain

4.2.4 Indicators

The RDGD31603PHSEVM evaluation board contains LEDs as visual indicators on the board.

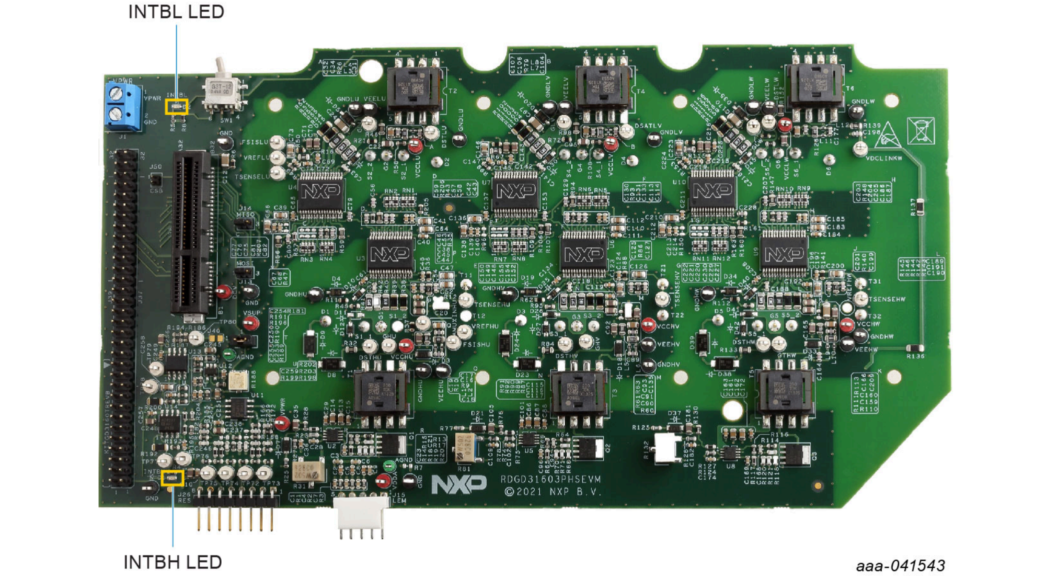


Figure 4. RDGD31603PHSEVM indicator locations

Table 3. RDGD31603PHSEVM indicator descriptions

Name	Description
INTBL LED	Indicates that a GD3160 INTB fault interrupt has occurred on the low-side
INTBH LED	Indicates that a GD3160 INTB fault interrupt has occurred on the high-side

4.2.5 Connectors and jumpers

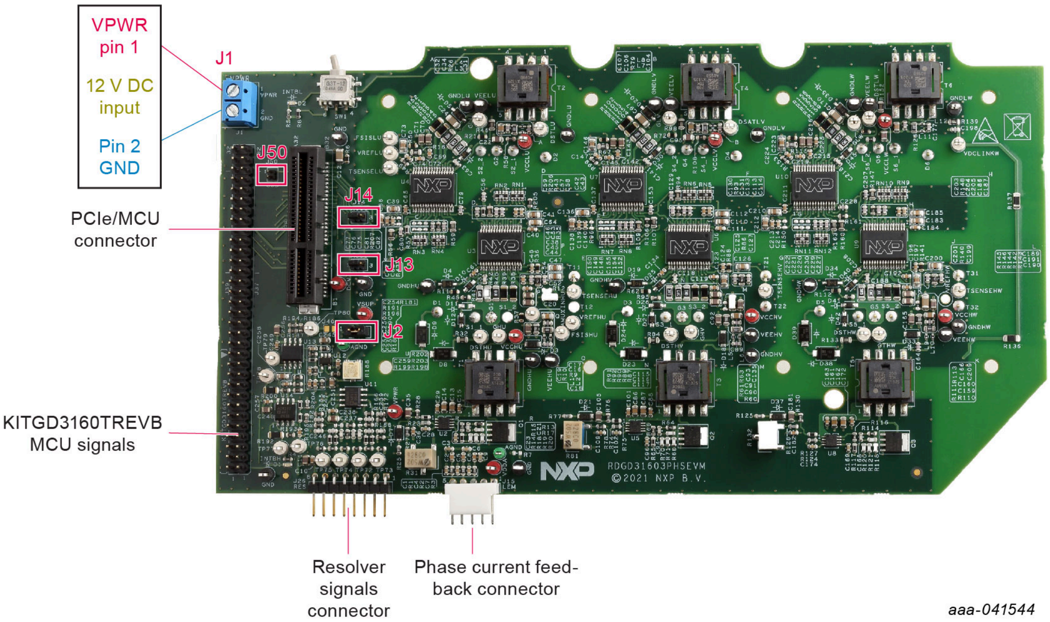


Figure 5. RDGD31603PHSEVM connector and jumper locations

Table 4. RDGD31603PHSEVM connector and jumper descriptions

Name	Description
J2	Jumper 1-2 default - DC supply for VSUP to gate drivers supplied through J1 terminal connection Jumper Open VSUP supply to gate drivers isolated
J13	Jumper 1-2 default MOSI – Normal mode three device daisy chain 3 device high-side, 3 device low-side (x3 – 2 channel) Jumper 2-3 MOSI - Six device daisy chain all six gate drivers daisy chained together (x6 – 1 channel)
J14	Jumper 1-2 default MISO-Normal mode three device daisy chain 3 device high-side, 3 device low-side (x3 – 2 channel) Jumper 2-3 MISO - Six device daisy chain all six gate drivers daisy chained together (x6 – 1 channel)
J50	Jumper open default CSB-Normal mode three device high-side, 3 device low-side (x3 - 2 channel) Jumper 1-2 CSB - Six device daisy chain all six gate drivers daisy chained together (x6 - 1 channel)
Phase current feedback connector	Current feedback connections from U, V, and W phases
Resolver signals connector	Resolver excitation signals (see schematic for more information)
MCU Signals	Two-row header of all MCU signals for debug and development. (See schematic for details)
PCIe/MCU connector	2x32 PCIe connector for easy connection to MPC5777CDEVB or MPC5744P via PCIe cable (S32SDEV-CON18)
J1 VPWR terminal connector	Used for external low voltage power supply connection typically 12 V Vbatt

4.2.6 Power supply test points

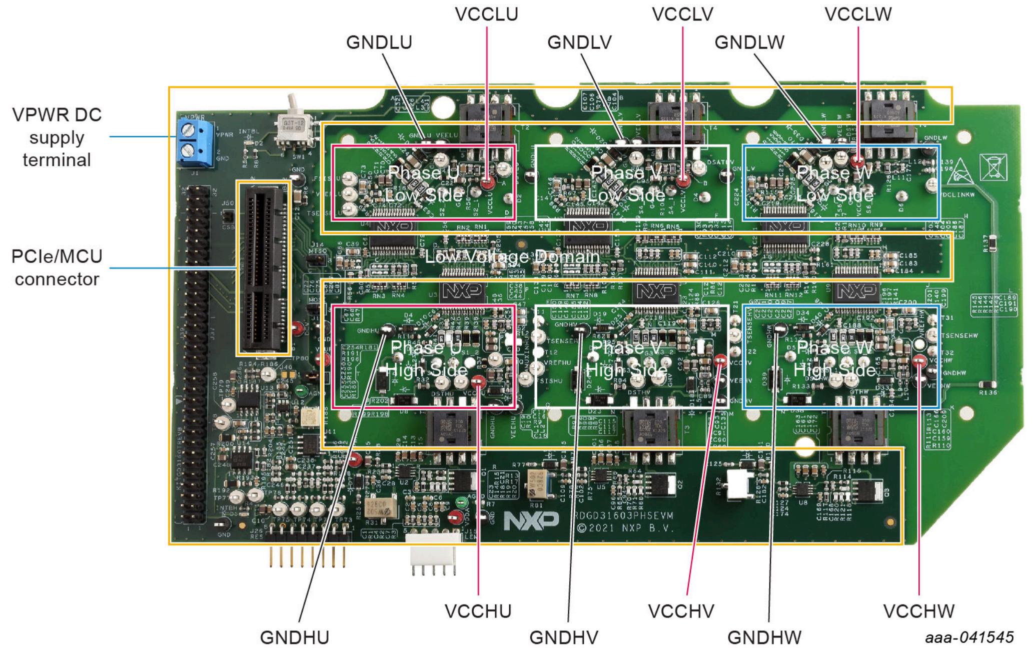


Figure 6. Power supply test point locations

Table 5. Power supply test point descriptions

Name	Function
VCCHU	High-side phase U VCC voltage test point Isolated positive voltage supply (15 V to 18 V)
VCCHV	High-side phase V VCC voltage test point Isolated positive voltage supply (15 V to 18 V)
VCCHW	High-side phase W VCC voltage test point Isolated positive voltage supply (15 V to 18 V)
VCCLU	Low-side phase U VCC voltage test point Isolated positive voltage supply (15 V to 18 V)
VCCLV	Low-side phase V VCC voltage test point Isolated positive voltage supply (15 V to 18 V)
VCCLW	Low-side phase W VCC voltage test point Isolated positive voltage supply (15 V to 18 V)
VPWR	+12 V DC VPWR low voltage positive supply connection (+12 V DC)
VPWR GND	VPWR low voltage supply ground connection (GND1)

4.2.7 Gate drive resistors

- RGH - RGH - gate high resistor in series with the GH pin at the output of the GD3100 high-side driver and IGBT gate that controls the turn on current for IGBT/SiC gate.
- RGL - gate low resistor in series with the GL pin at the output of the GD3100 low-side driver and IGBT gate that controls the turn off current for IGBT/SiC gate.
- RAMC - series resistor between IGBT/SiC gate and AMC input pin of the GD3100 high-side/low-side driver for gate sensing and Active Miller clamping.

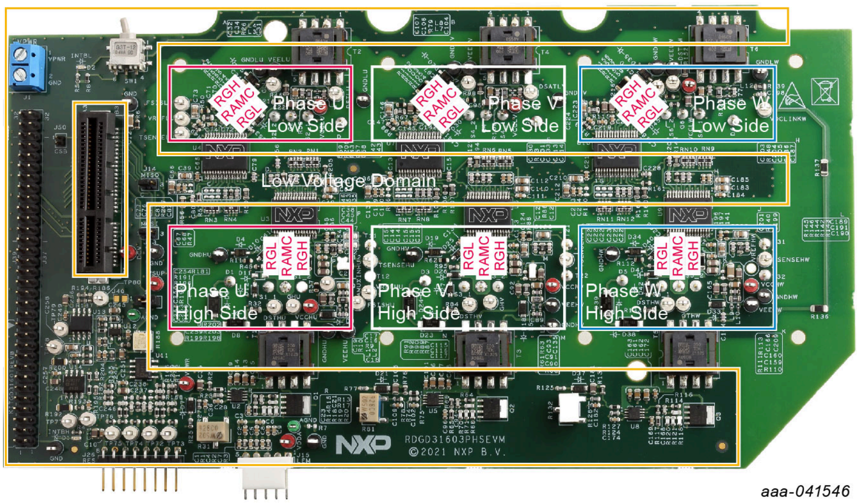


Figure 7. Gate drive resistors for each phase high-side and low-side

4.2.8 SiC module pin connections

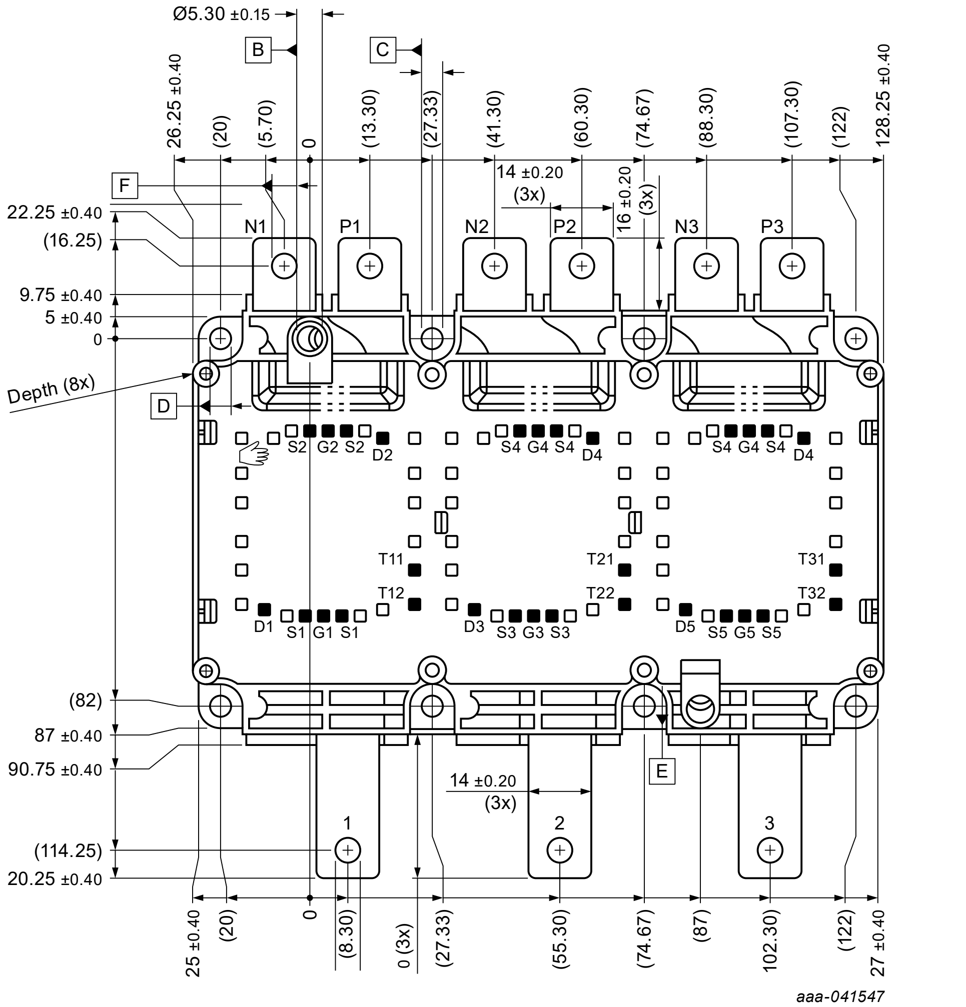


Figure 8. SiC module pin placement

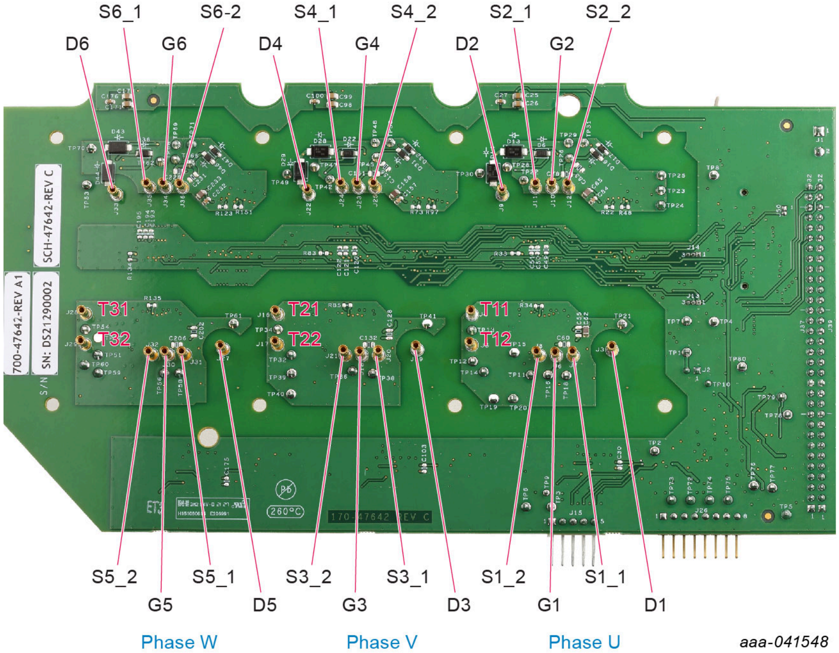


Figure 9. SiC module connection pins

Table 6. SiC module pin connections

Connection name	Pin description
G1	Gate high-side U phase
D1	Drain high-side U phase
S1_1	Source connection 1 high-side U phase
S1_2	Source connection 2 high-side U phase
T11	NTC temperature sensor connections U phase
T12	NTC temperature sensor connections U phase
G2	Gate low-side U phase
D2	Drain low-side U phase
S2_1	Source connection 1 low-side U phase
S2_2	Source connection 1 low-side U phase
T21	NTC temperature sensor connections V phase
T22	NTC temperature sensor connections V phase
G3	Gate high-side V phase
D3	Drain high-side V phase
S3_1	Source connection 1 high-side V phase
S3_2	Source connection 2 high-side V phase
T31	NTC temperature sensor connections W phase
T32	NTC temperature sensor connections W phase
G4	Gate low-side V phase
D4	Drain low-side V phase
S4_1	Source connection 1 low-side V phase
S4_2	Source connection 1 low-side V phase

Table 6. SiC module pin connections*...continued*

Connection name	Pin description
G5	Gate high-side W phase
D5	Drain high-side W phase
S5_1	Source connection 1 high-side W phase
S5_2	Source connection 2 high-side W phase
G6	Gate low-side W phase
D6	Drain low-side W phase
S6_1	Source connection 1 low-side W phase
S6_2	Source connection 1 low-side W phase

4.3 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.

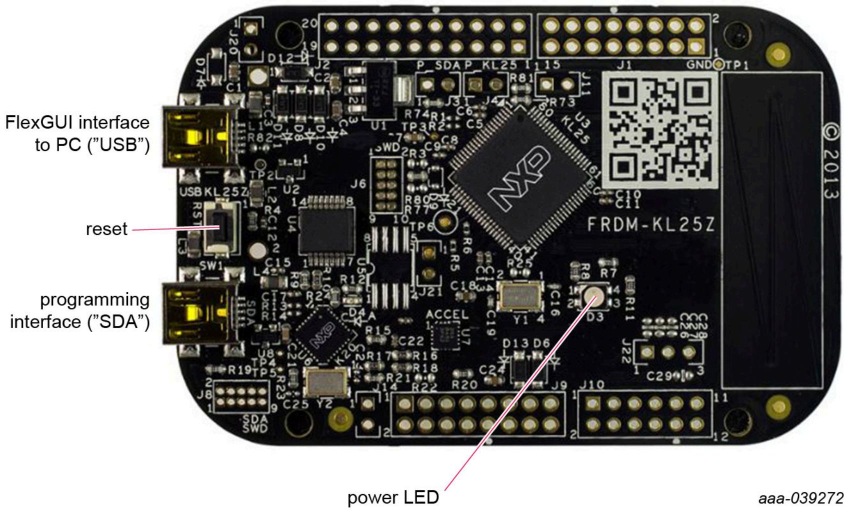


Figure 10. Freedom development platform

4.4 3.3 V to 5.0 V translator board

KITGD3160TREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

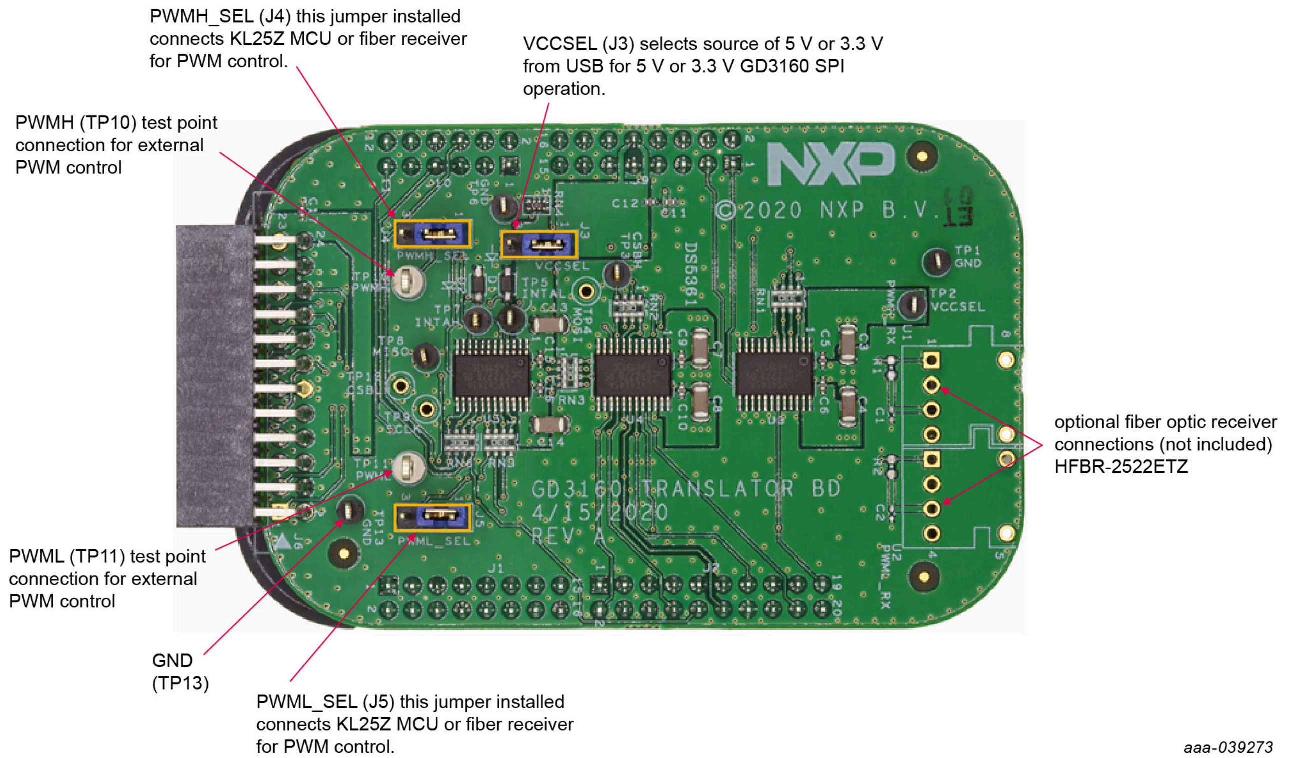


Figure 11. Translator board

Table 7. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J3)	1-2	selects 5.0 V for 5.0 V compatible gate drive
	2-3	selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	selects PWM high-side control from KL25Z MCU
	2-3	selects PWM high-side control from fiber optic receiver inputs
PWML_SEL (J5)	1-2	selects PWM low-side control from KL25Z MCU
	2-3	selects PWM low-side control from fiber optic receiver inputs

4.5 Schematic, board layout and bill of materials

The schematic, board layout and bill of materials for the RDGD31603PHSEVM reference design are available at http://www.nxp.com/RDGD31603PHSEVM.

5 Installing and configuring software and tools

Software for RDGD31603PHSEVM is distributed with the FlexGUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

Even if the user intends to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.

5.1 Installing FlexGUI on your computer

The latest version of FlexGUI supports the GD3100 and GD3160. It is designed to run on any Windows 10 or Windows 8 based operating system. To install the software, do the following:

1. Go to www.nxp.com/FlexGUI and click **Download**.
2. When the FlexGUI software page appears, click **Download** and select the version associated with your PC operating system.
3. FlexGUI wizard creates a shortcut, an NXP FlexGUI icon appears on the desktop. By default, the FlexGUI executable file is installed at **C:\flexgui-app-des-gd31xx.exe**. Installing the device drivers overwrites any previous FlexGUI installation and replaces it with a current version containing the GD31xx drivers. However, configuration files (.spi) from the previous version remain intact.

5.2 Configuring the FRDM-KL25Z microcode

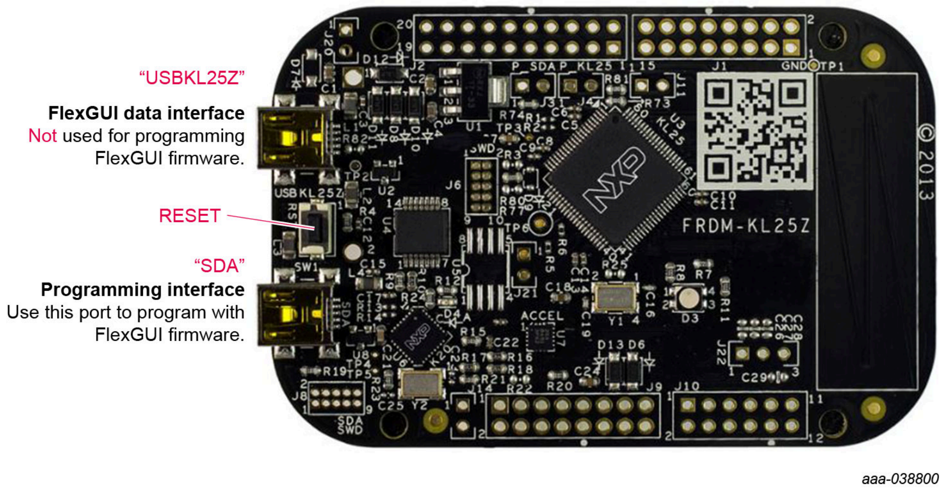


Figure 12. FRDM-KL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open FlexGUI, and verify that the software version at the bottom is 6.4 or later (see Figure 13).

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in bootloader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.

2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, you may go to step 6.
3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI package.
   a. From the FlexGUI install directory, which is located in the **flexgui-app-des-gd31xx\bin** folder and is named in the form “flexgui-fw-KL25Z_usb_hid_gd31xxC_vx.x.x.bin”.
   b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of RDGD31603PHSEVM.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .bin file into the KL25Z device memory. Once done, disconnect the USB and plug into the other USB port, labeled **KL25Z**.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.
8. The FRDM-KL25Z board is now fully set up to work with RDGD31603PHSEVM and the FlexGUI.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

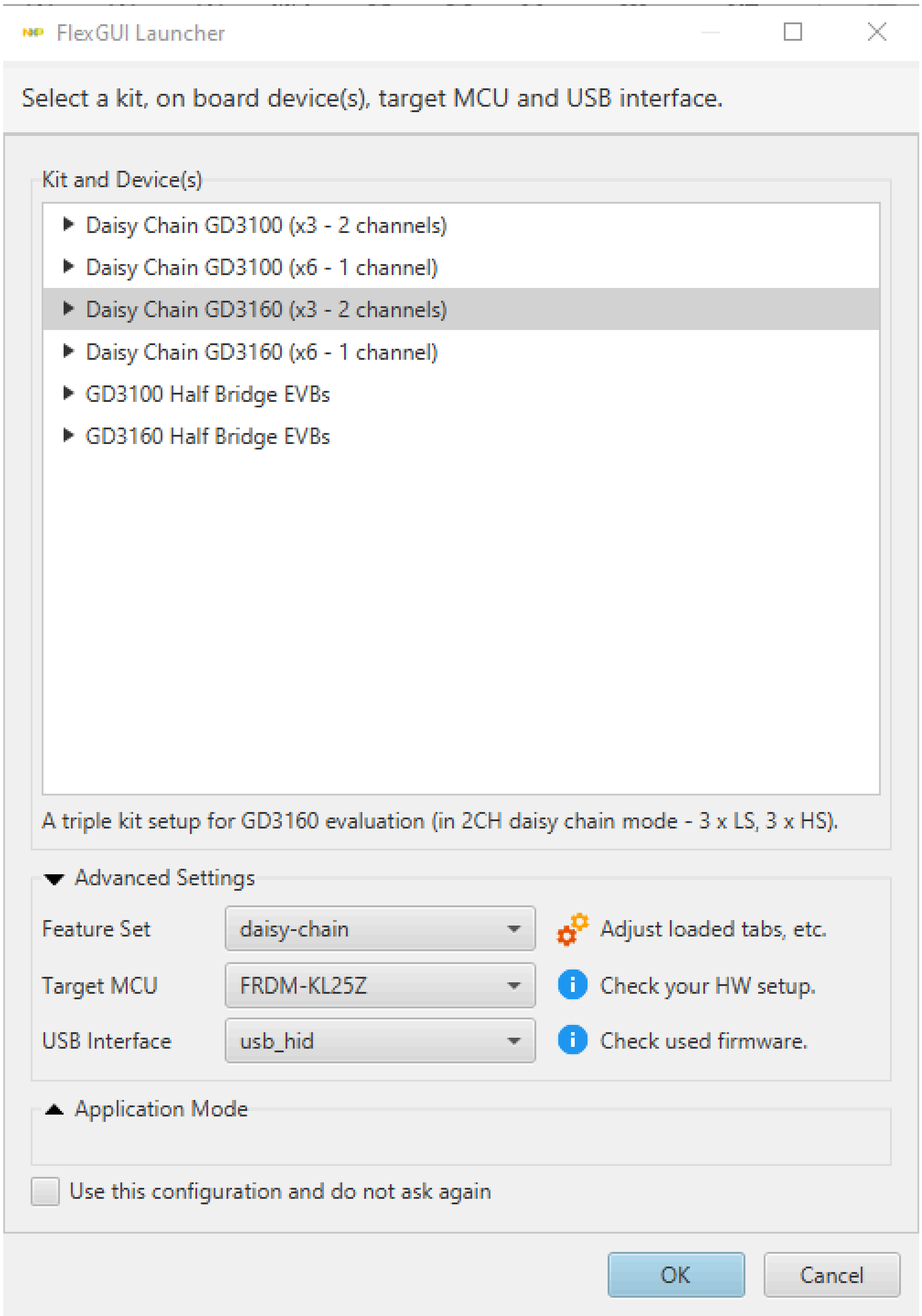
5.3 Using the FlexGUI

The FlexGUI is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD31xx-specific functionality, configuration, and fault reporting. FlexGUI also includes basic capacity for the RDGD31603PHSEVM to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both GD31xx on the board via daisy chain. See Figure 13 to Figure 32 for FlexGUI for GD31xx internal register read and write access.

Starting FlexGUI for GD31xx

- FlexGUI install program (flexgui-app-des-gd31xx-0.x.x.exe)
- Download FlexGUI and run the install program on your PC.
- When you start the application, Figure 13 allows you to select the target application board, feature set (standard or daisy chain), target MCU, and USB interface. Leave all settings as shown.



Note: *See Table 4 for required jumper configuration to enable (x3 - 2 channel) or (x6 -1 channel) SPI daisy chain operation.*

Figure 13. Kit selection

FlexGUI settings

- Access settings by selecting Settings from the File menu

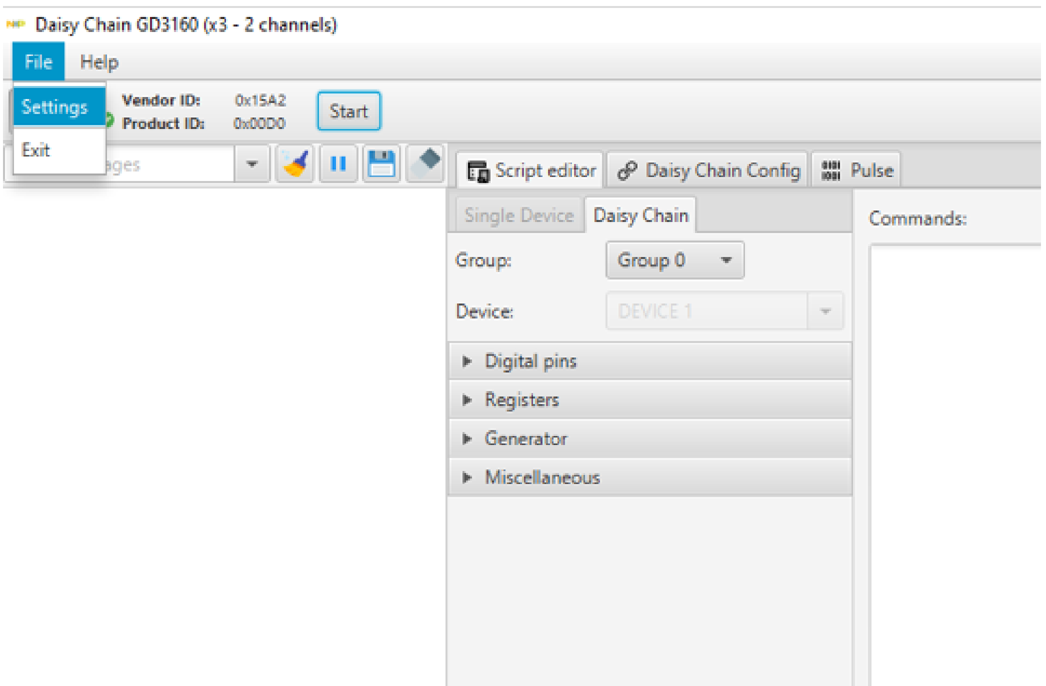
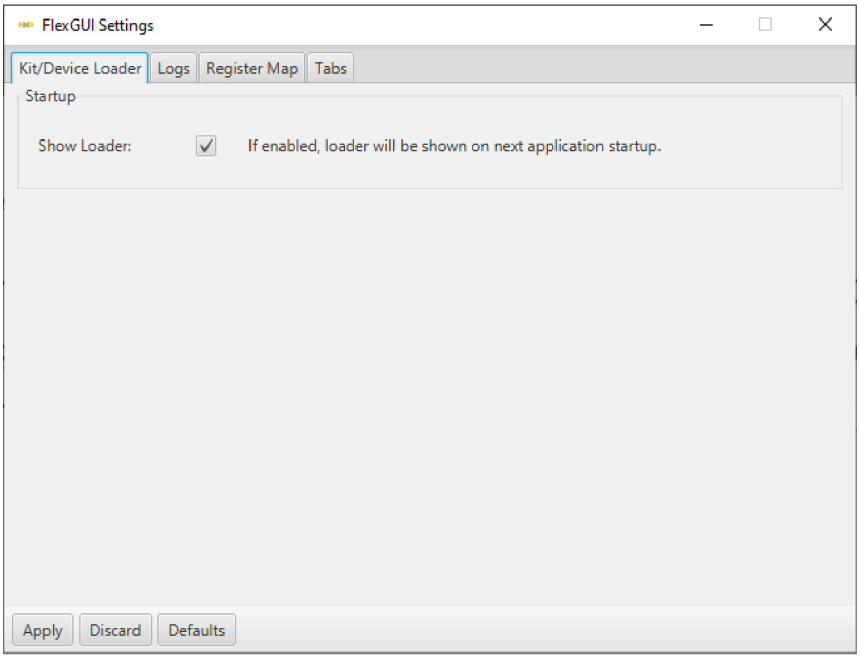


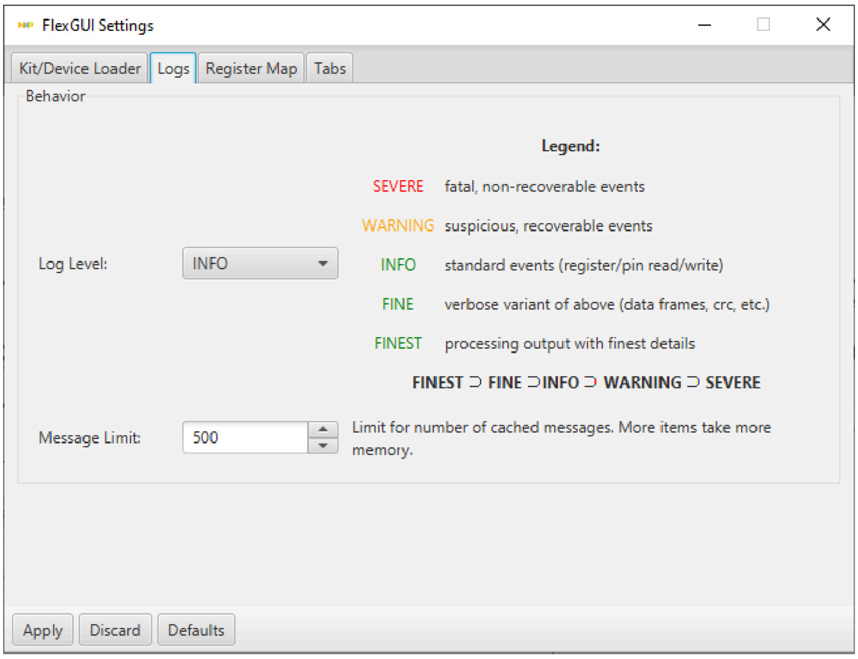
Figure 14. GUI settings menu

- The Loader and Logs settings are shown below:



aaa-038532

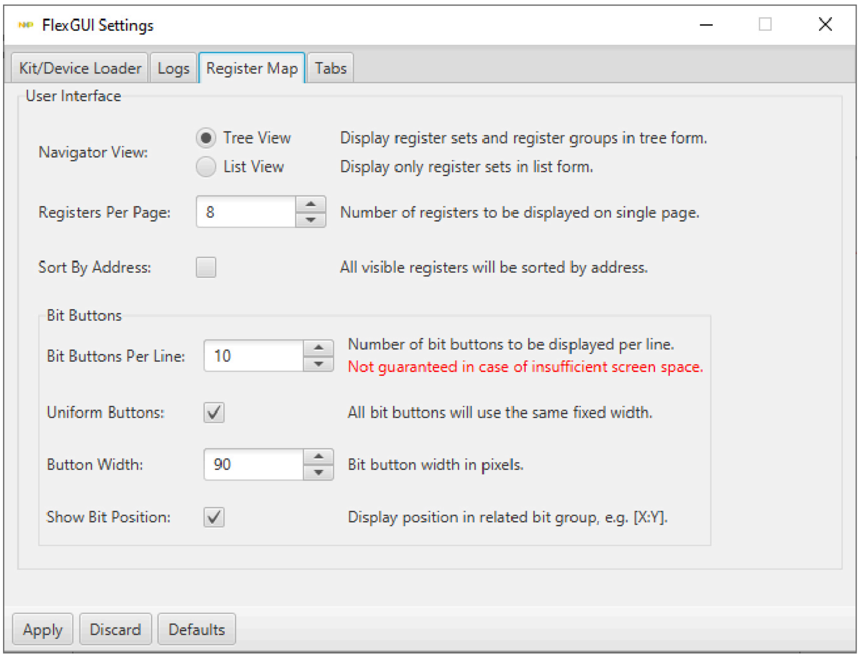
Figure 15. Loader settings



aaa-038533

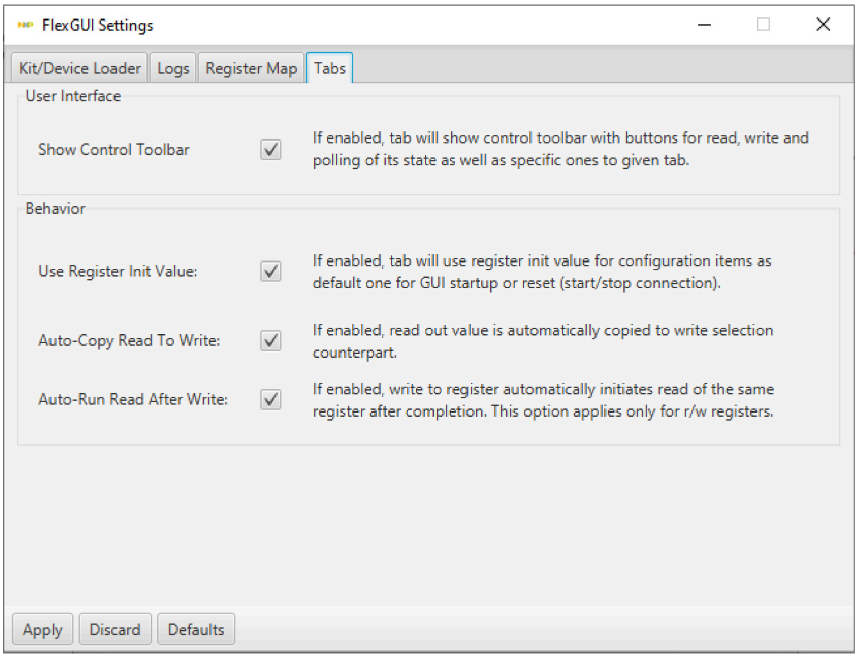
Figure 16. Logs settings

- Access settings by selecting Settings from the File menu.
- The Register Map and Tabs settings are shown below:



aaa-038534

Figure 17. Register map settings



aaa-038535

Figure 18. Tabs settings

Command Log window

- The Command Log area informs the user about application events.

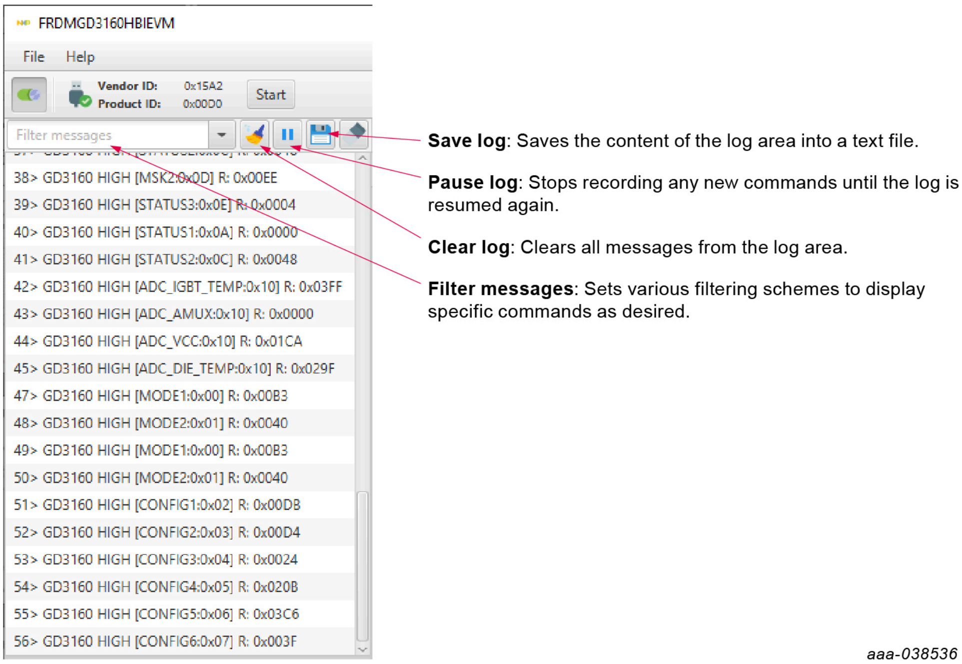


Figure 19. Command Log area

Global workspace controls

- Always visible in the lower left corner of the main application window.
  - GD3160 tab functionality
    - Switch modes between run and configuration mode
    - Set SPI frequency

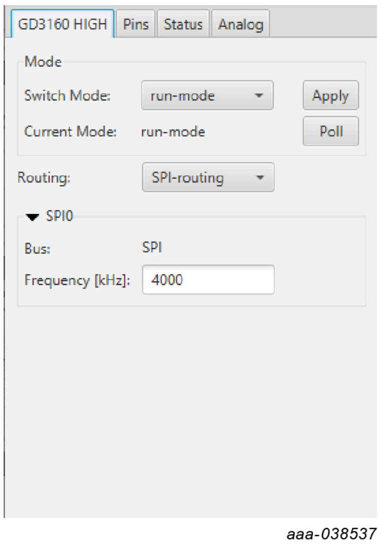


Figure 20. Device pins settings and status menus

- Pins tab functionality
  - Set control levels. Default values are shown.
  - Read and automatically poll INTB pins (INTA pins are added for GD3160).
  - Control pins set values to a default to a functional state.
    - FSENB - enable/disable fail-safe enable
    - EN_PS - enables flyback supply on EVB at 17 V V_{CC} on high-side and low-side
    - FSSTATEL and FSSTATEH set the fail-safe state when FSENB is enabled
    - PWML and PWMH set the default state PWM inputs for high-side and low-side

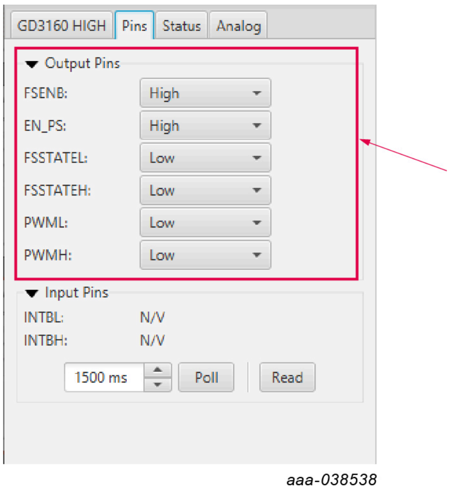


Figure 21. Pins tab functionality

- Status tab functionality
  - Monitors Status 1 and Status 2 fault bits. Bits that are set are shown in red.
  - Ability to clear all faults and automatically poll status registers.

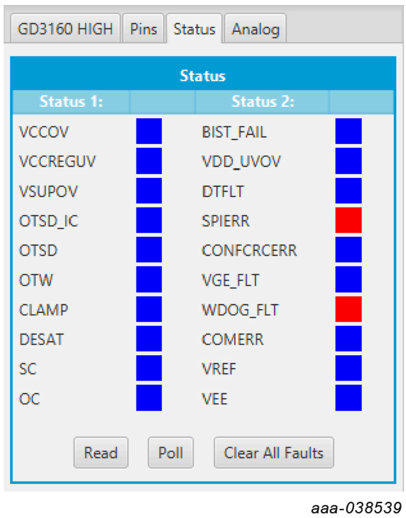


Figure 22. Status tab functionality

- Analog tab functionality
  - Read and poll ADC values from the high-voltage domain
  - Displays raw ADC and converted values

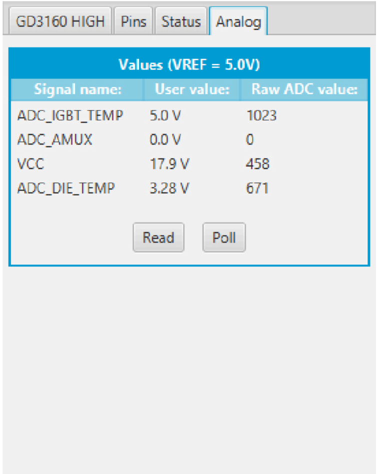


Figure 23. Analog tab functionality

Register map

- Registers are grouped according to function; independent lines to read and write the registers
- Registers can be read and write by selecting Set to Read and SEND for read and Set to Write and SEND for write.
- Copy button to copy the read values to the write line; can be set to copy automatically
- Reset button to undo the changes on the write line and reset to the previous value
- Global register controls perform the selected command on all registers with the checkbox selected.

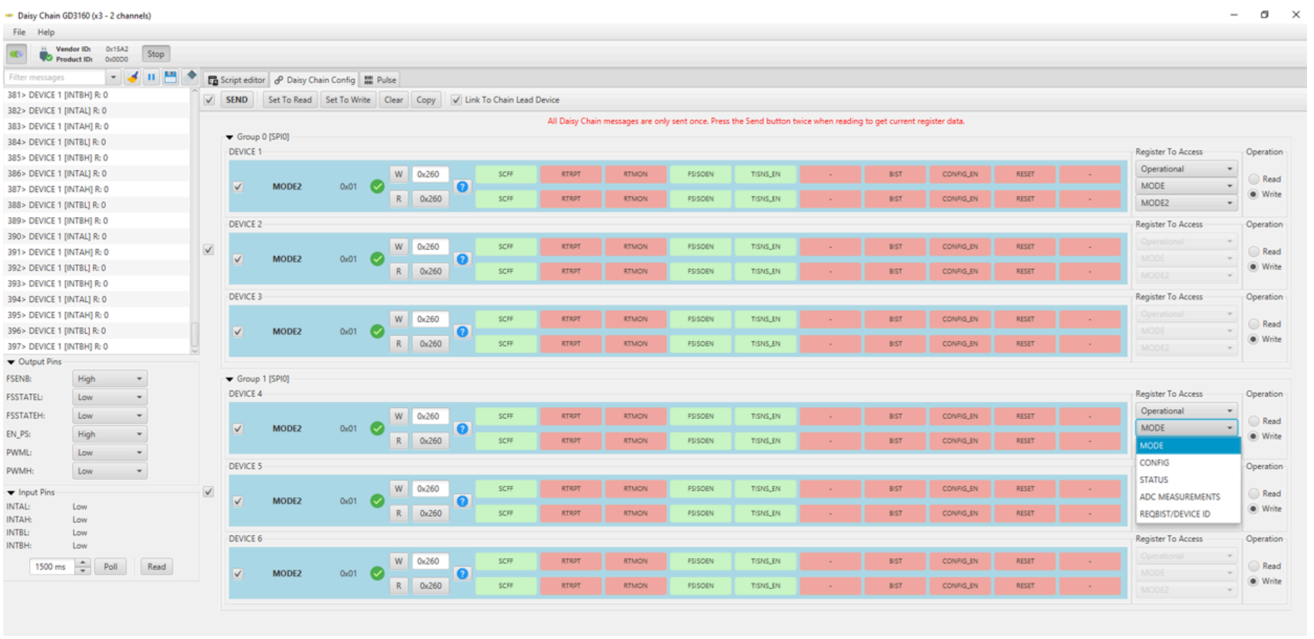


Figure 24. Register map

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

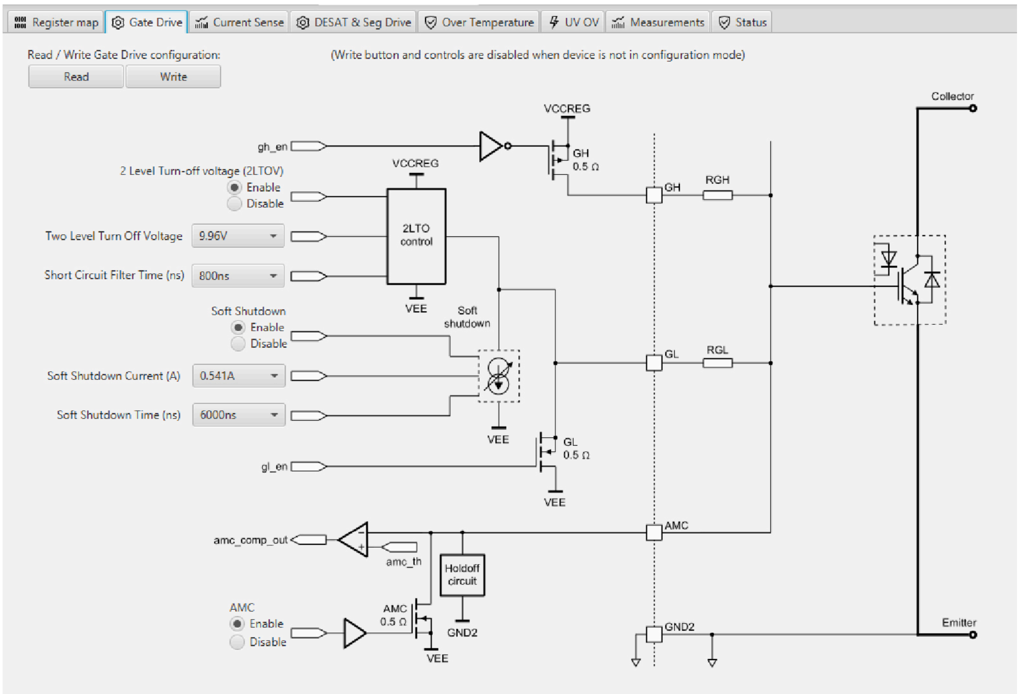


Figure 25. Gate drive tab

Current Sense tab

- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

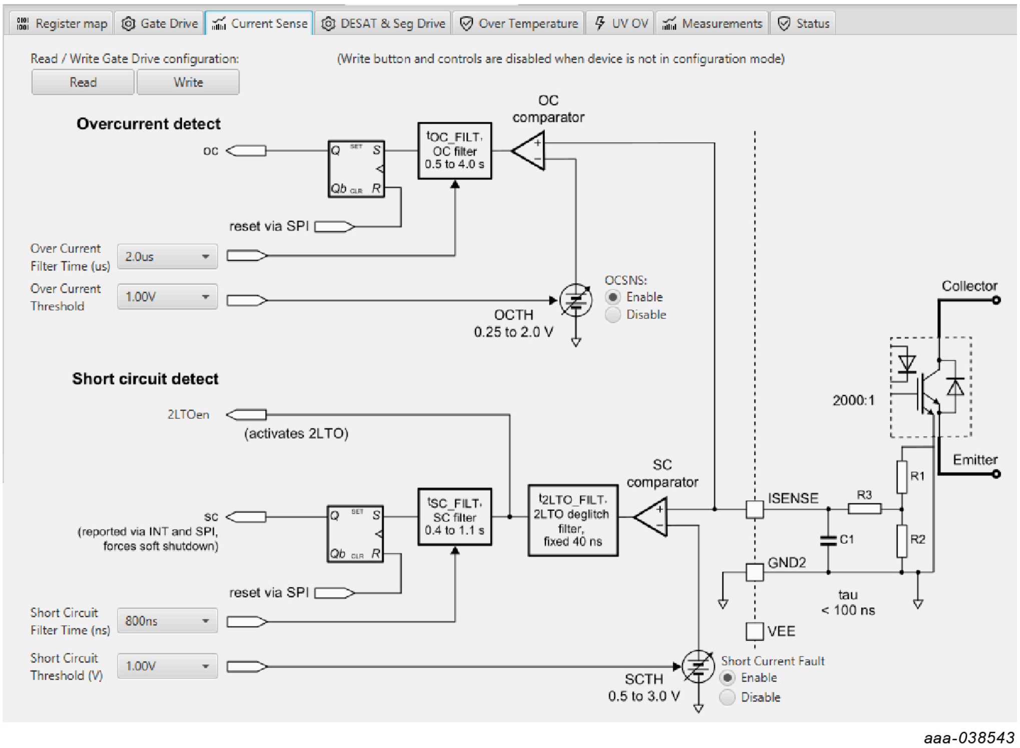


Figure 26. Current sense tab

DESAT and Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

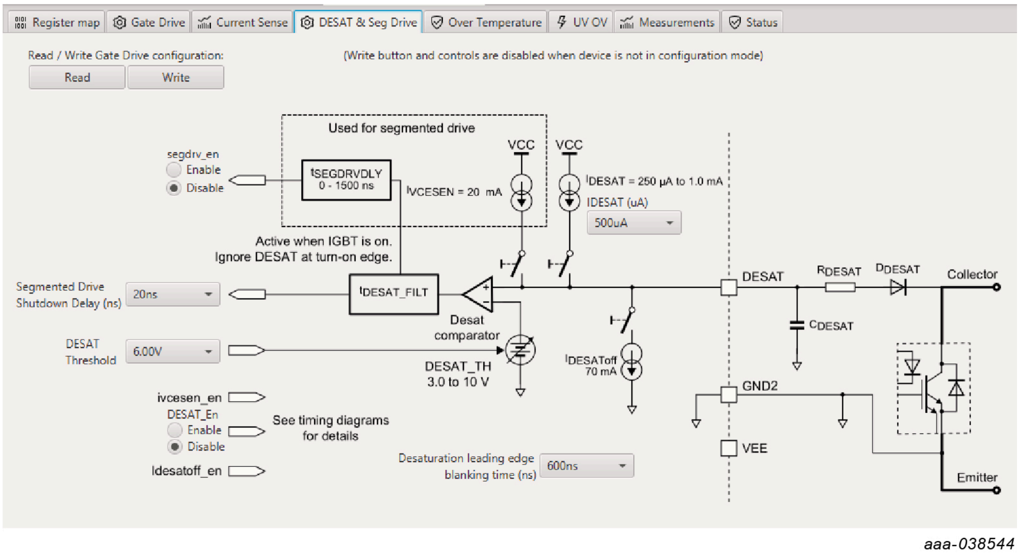
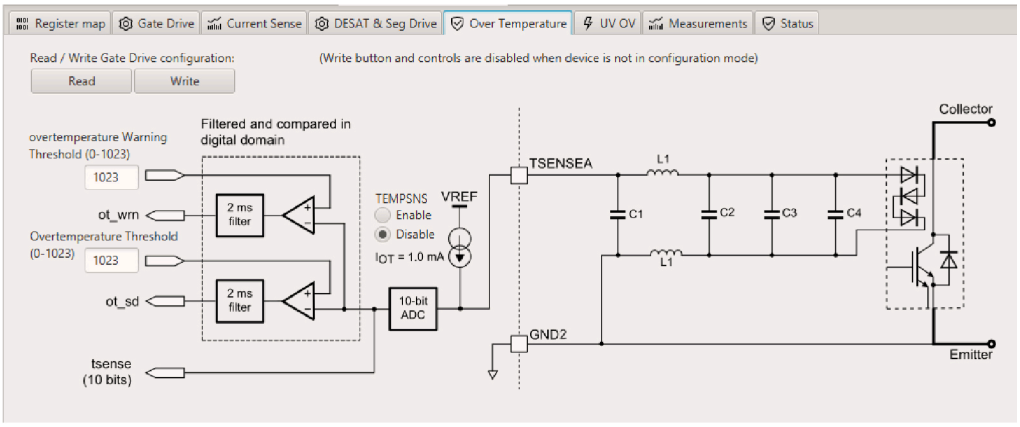


Figure 27. Desat and segmented drive tab

Overtemperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

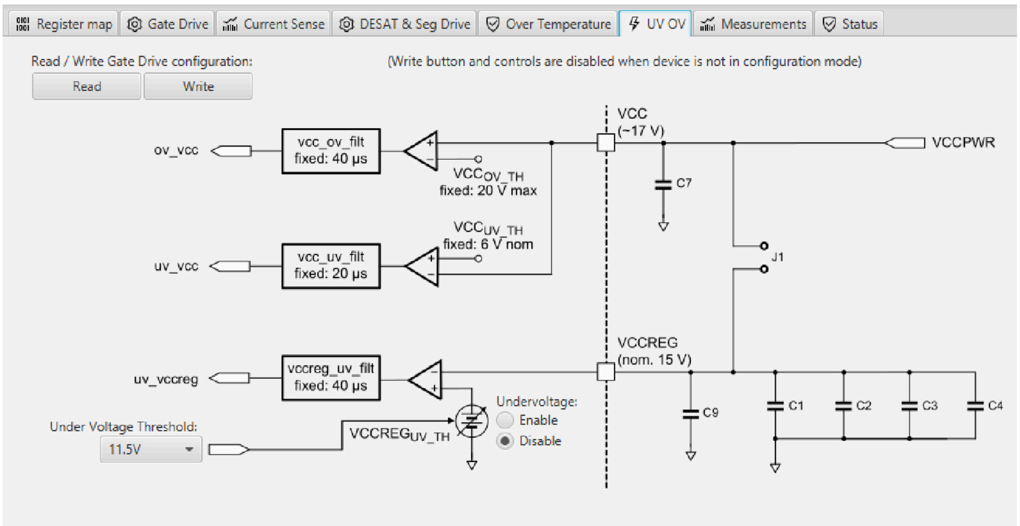


aaa-038545

Figure 28. Overtemperature tab

Undervoltage threshold tab

- Allows setting of parameters related to undervoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.



aaa-038546

Figure 29. Undervoltage and overvoltage tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values

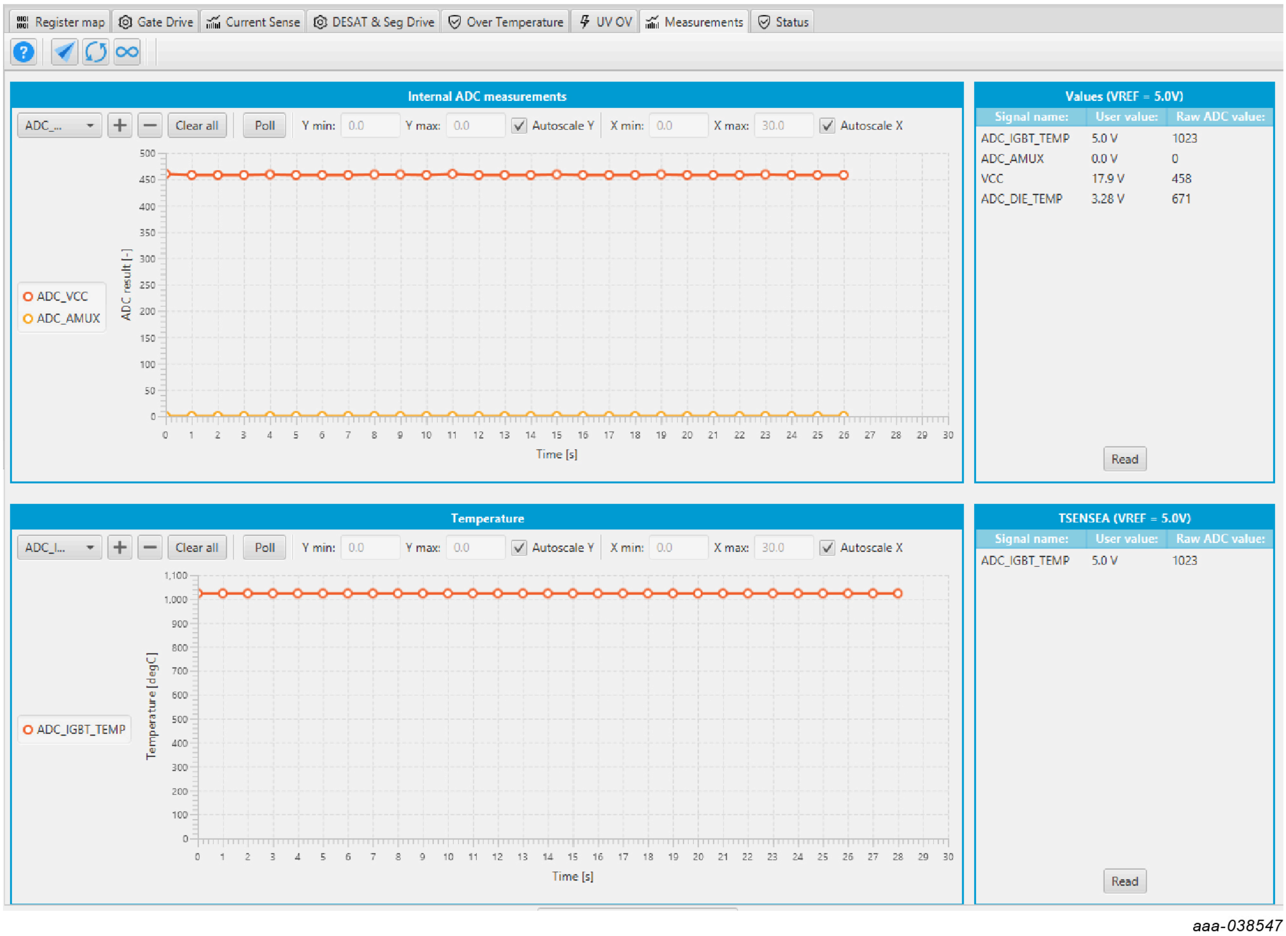


Figure 30. Measurements tab

Status tab

- Allows monitoring of Status 1, Status 2, and Status 3 register values
- Status 1 and Status 2 faults can be cleared
- Status mask registers can be modified when in configuration mode

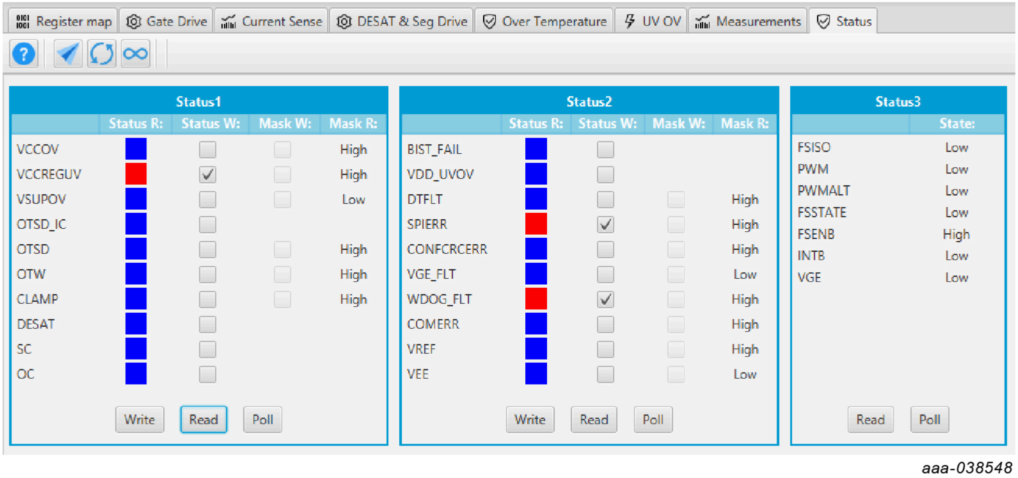


Figure 31. Status tab

Pulse tab

- Used for double pulse, short-circuit, and PWM testing
- Select desired T1, T2, and T3 timings for each test type; select enable then generate pulses

Note: *Phase U can be configured for performing Double pulse and short-circuit testing. To enable short-circuit testing, two resistors (R46, R53) must be pulled from PWMALT phase U signals to disable Deadtime control on Phase U Gate drivers.*

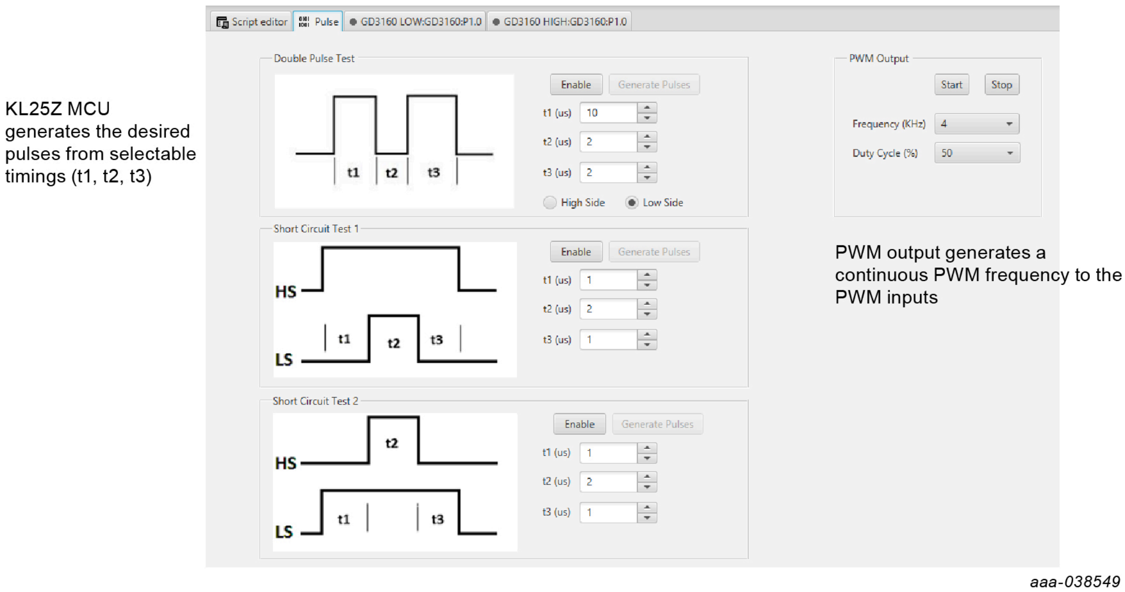


Figure 32. Pulse tab

5.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 4.4
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3160	Monitor EXT_PWML (TP14) and EXT_PWMH (TP15) for commanded PWM state
	Check FSENB status (see GD3160 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3160: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check Phase U PWMALT weak pull-downs R206 and R57 are in place to bypass dead time faults. Consider adjusting dead time settings on GD3160: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3160: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3160 VDD voltage	Low translator output voltage (compared with correct VDD at GD3160) causes the high threshold at the GD3160 pin to be crossed later than commanded	Check translator output voltage selection (J233) is configured to the same level as the GD3160 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3160 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3160 after translator is powered (over USB).

Problem	Evaluation	Explanation	Corrective action(s)
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (5 kΩ potentiometer).
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using 5 kΩ potentiometer feedback
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (5 kΩ potentiometer). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	For short-circuit test, set PWMLSEL (J9) and PWMHSEL (J10) to bypass dead time.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check PS_EN is set to HIGH in FlexGUI; see Figure 21	VCC/VEE can be enabled/disabled in software.	Enable VCC/VEE from FlexGUI
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using 5 kΩ potentiometer feedback

6 Configuring the hardware

RDGD31603PHSEVM with KITGD3160TREVB attached as shown in Figure 33 utilizing Windows based PC and FlexGUI software.

Note: *Double pulse and short-circuit testing can be conducted on Phase U only. See FlexGUI Pulse Tab, Figure 32.*

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor compatible with HybridPACK Drive module
- IGBT or SiC MOSFET HybridPACK Drive module
- Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP
  - +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- Load coil for double pulse and short-circuit testing, Phase U only

Note: *To enable short-circuit testing, two resistors (R46, R53) must be pulled from PWMALT phase U signals to disable Deadtime control on Phase U gate drivers.*

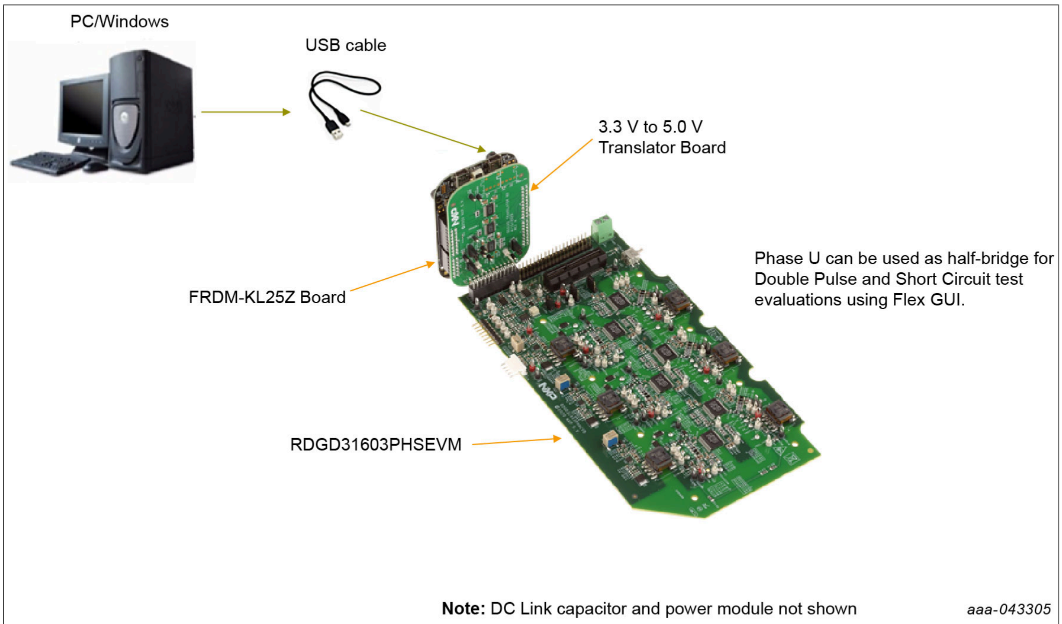


Figure 33. Evaluation setup using KITGD3160TREVB and FlexGUI

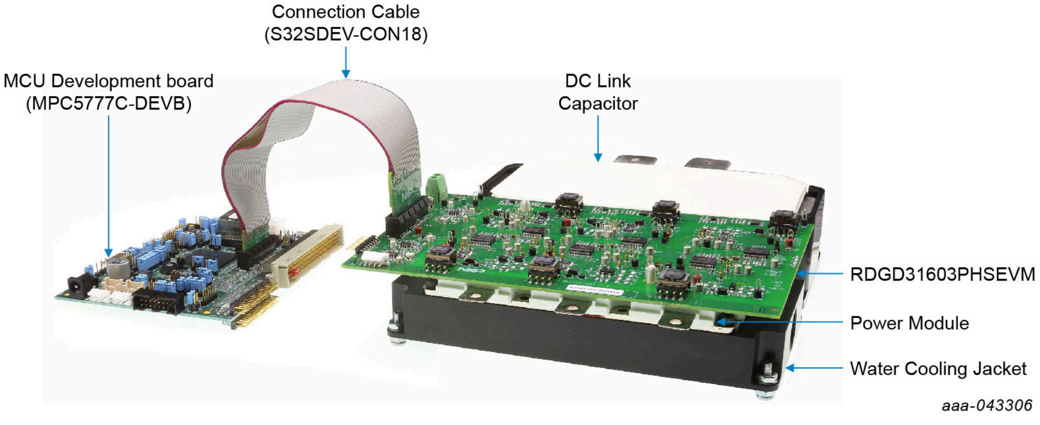


Figure 34. Evaluation setup using MPC5777C-DEVB MCU dev kit

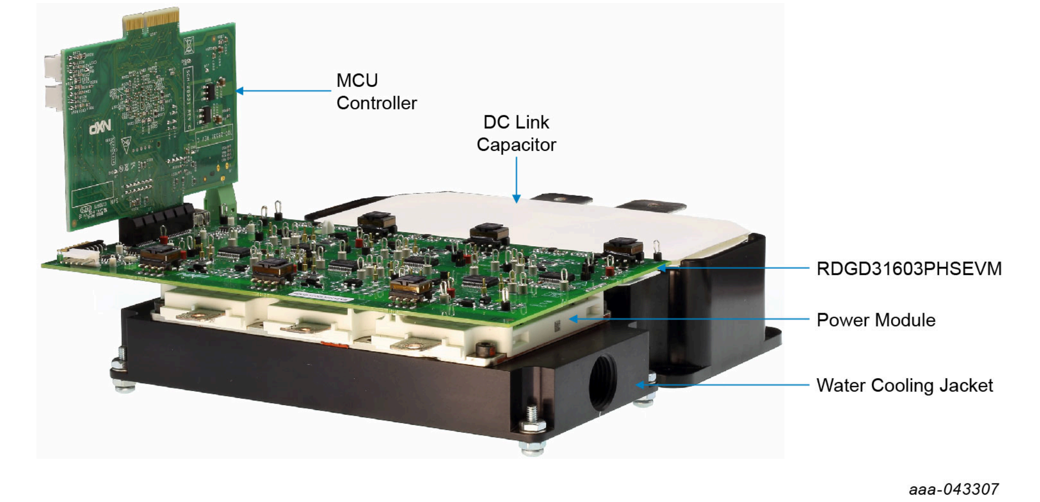


Figure 35. Evaluation setup using MPC5744P MCU dev kit

7 References

[1] **RDGD31603PHSEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/RDGD31603PHSEVM

[2] **GD3160** — product information on Advanced single-channel gate driver for IGBT/SiC
http://www.nxp.com/GD3160

[3] **MPC5777C** — ultra-reliable MCU for automotive and industrial engine management
http://www.nxp.com/MPC5777C

[4] **MPC5744P** — ultra-reliable MCU for automotive and industrial safety applications
https://www.nxp.com/MPC574xP

[5] **MPC5775B/E-EVB** — low-cost development board for Battery Management and Inverter
https://www.nxp.com/MPC5775B-E-EVB

8 Legal information

8.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

8.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

8.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

Date of release: 18 August 2021
Document identifier: UM11063