UM11493

TEA2209DB1584 active bridge rectifier controller demo board

Rev. 1.1 — 6 April 2021 User manual

Document information

Information	Content
Keywords	TEA2209T, TEA2209DB1584, active bridge rectifier controller, X-capacitor discharge, self-supplying, high efficiency, traditional diode bridge, power supply, demo board
Abstract	The TEA2209T is an active bridge rectifier controller replacing the traditional diode bridge. Using the TEA2209T with low-ohmic high-voltage external MOSFETs significantly improves the efficiency of the power converter as the typical rectifier diode-forward conduction losses are eliminated. In addition, the TEA2209T includes an X-capacitor discharge function. To reduce power consumption at a standby condition, an external signal via the COMP pin can disable the TEA2209T. This user manual describes how the TEA2209DB1584 demo board can be used to replace the traditional diode bridge. This demo board contains a TEA2209T and four low-ohmic high-voltage MOSFETs.

Revision history

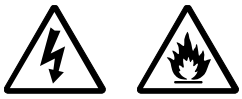
Rev	Date	Description
v.1.1	20210406	Updated version
Modifications:		• Figure 6 in Section 5 has been updated. • Figure 9 in Section 6.3 has been updated.
v.1	20210129	Initial version

1 Introduction

Note: *This product has not undergone formal EU EMC assessment. As a component used in a research environment, it is the responsibility of the user to ensure that the finished assembly does not cause undue interference when used. It cannot be CE marked unless assessed.*

WARNING

Lethal voltage and fire ignition hazard



The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This user manual describes the TEA2209DB1584 demo board. It provides a functional description, supported with instructions on how to connect the board to obtain the best results and performance.

The TEA2209T is a product of a new generation of active bridge rectifier controllers replacing the traditional diode bridge.

Using the TEA2209T with low-ohmic high-voltage external MOSFETs significantly improves the efficiency of the power converter as the typical rectifier diode-forward conduction losses are eliminated. Efficiency can improve up to about 1.4 % at 90 V (AC) mains voltage.

The TEA2209T is intended for power supplies with a boost-type power-factor controller as a first stage. The second stage can be a resonant controller, a flyback controller, or any other controller topology. It can be used in all power supplies requiring high efficiency such as adapters, server and telecom power supplies, desktop PCs, all-in-all PC power supplies, and television power supplies.

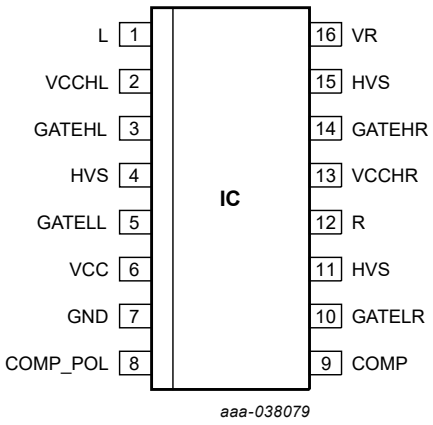


Figure 1. Pin configuration diagram (SO16)

1.1 Features

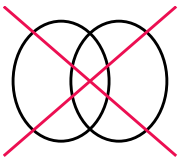
- Elimination of forward conduction losses of the diode rectifier bridge
- Very low IC power consumption (2 mW)
- Integrated high-voltage level shifters
- Directly drives four rectifier MOSFETs
- Very low external part count
- Integrated X-capacitor discharge (2 mA)
- Self-supplying
- Full-wave drive improving total harmonic distortion (THD)
- Undervoltage lockout (UVLO) for high-side and low-side drivers
- Drain-source overvoltage protection for all external power MOSFETs
- Gate pull-down currents at start-up for all external power MOSFETs
- Disable function for all external power FETs

2 Safety warning

This demo board is connected to the mains voltage. Avoid touching the board while it is connected to the mains voltage and when it is in operation. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. Galvanic isolation from the mains phase using a fixed or variable transformer is always recommended.

019aab173

a. Isolated



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b. Not isolated

Figure 2. Isolation symbols

3 Board photographs

The TEA2209DB1584 demo board consists of the TEA2209T in an SO16 package with four MOSFETs (600 V; 28 mΩ). Figure 3 shows the front side of demo board.

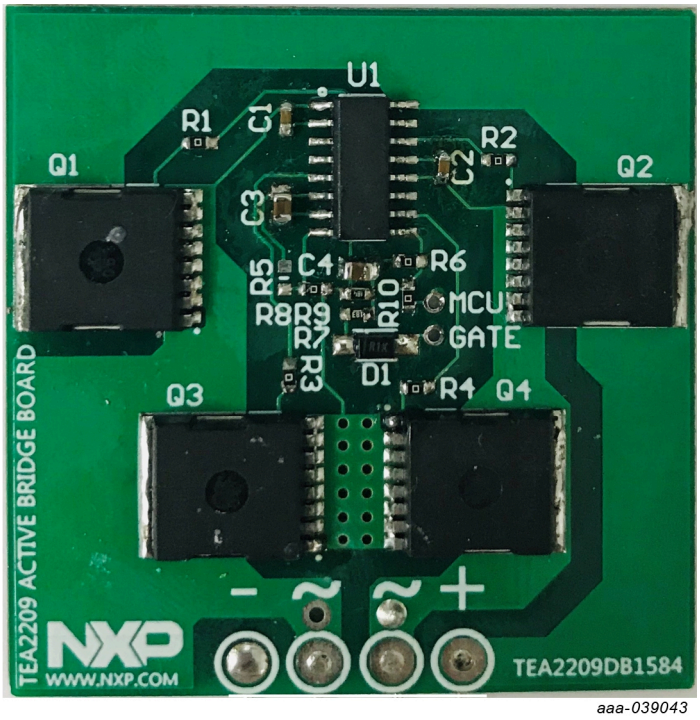
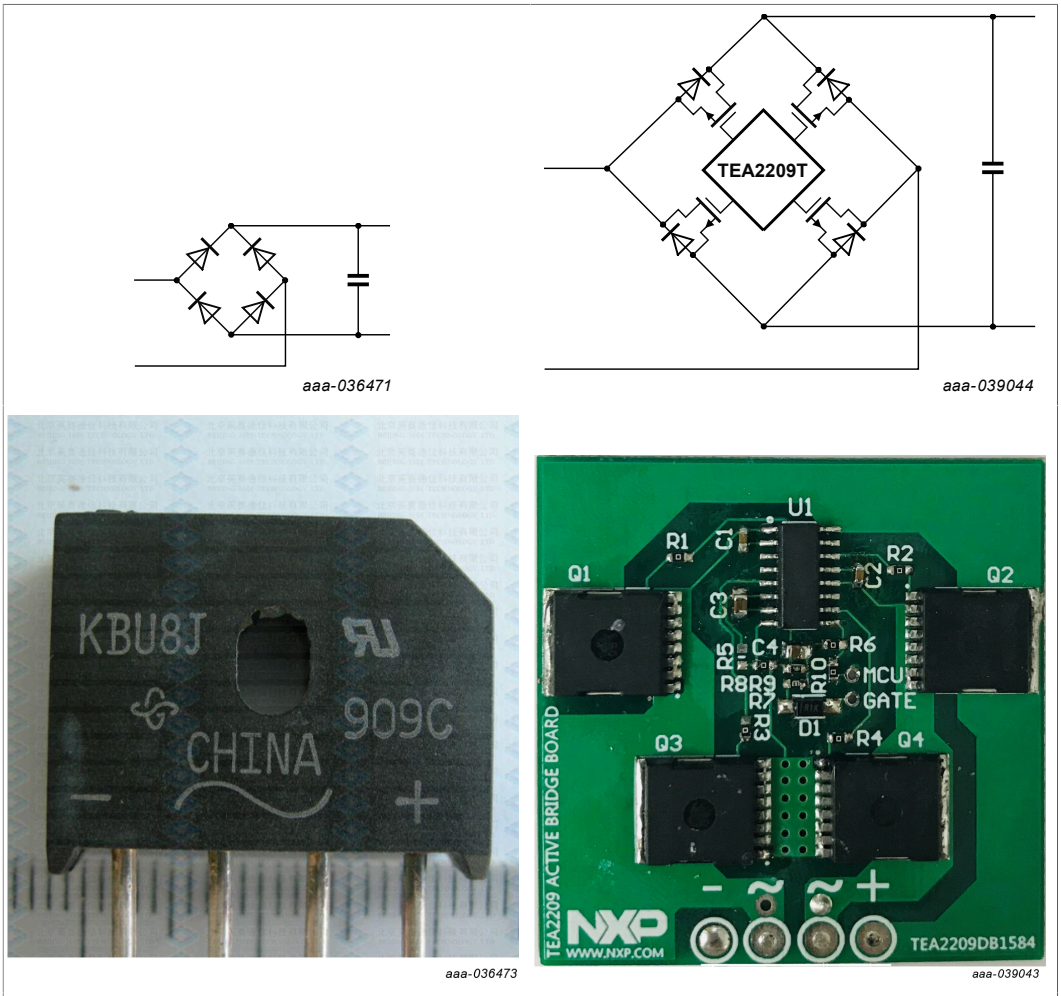


Figure 3. TEA2209DB1584 demo board photograph

4 TEA2209DB1584 demo board setup

The TEA2209DB1584 demo board contains four 600 V/28 mΩ MOSFETs. It makes the board suitable for universal AC input and output power applications of several hundreds of Watts. The TEA2209DB1584 demo board contains four leads that can easily replace a traditional diode bridge. The outer two leads are connected to positive and negative rectified voltages. The inner two leads are connected to AC mains lines. These four leads are pin-to-pin with typical bridge rectifier diodes pins. Figure 4 describes the difference between bridge diodes and active bridge configurations.



a. Diode bridge b. Active bridge

Figure 4. Diode bridge configuration versus TEA2209DB1584 demo board typical configuration

Figure 5 shows an example of the TEA2209DB1584 demo board mounted on an NXP Semiconductors TEA2016DB1519 demo board.

Figure 5. TEA2209DB1584 demo board added to 240 W resonant adapter board

5 Operation

The TEA2209T is a controller IC for an active bridge rectifier. It can directly drive the four MOSFETs in an active bridge. Figure 6 shows a typical configuration. As the output is a rectified sine wave, a boost-type power-factor circuit must follow the application.

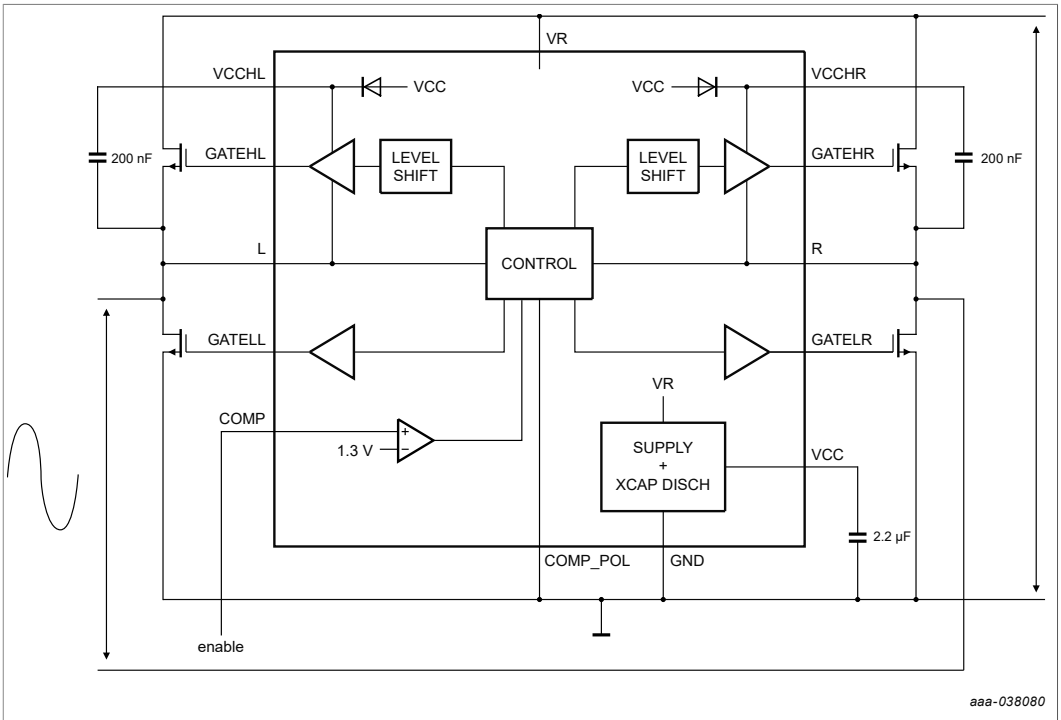


Figure 6. Typical configuration

The control circuit of the TEA2209T senses the polarity of the mains voltage between pins L and R. Depending on the polarity, either GATELL or GATELR is switched on. The comparator in the control circuit, which compares the L and R voltages, has thresholds of 250 mV and −250 mV depending on the slope polarity. If the difference voltage between L and R is less than 250 mV both GATELL and GATELR are low.

The gate drivers are high-current rail-to-rail MOS output drivers. An on-chip supply circuit which draws current from either L or R generates the gate driver voltage. After a zero-crossing of the mains voltage, the supply capacitor C_{VCC} is charged to the regulation level V_{reg}. Then the discharge state is entered. The resulting power dissipation from the mains voltage is about 1 mW excluding gate charge losses of the external power MOSFETs. These gate charge losses typically add 1 mW of dissipation.

At start-up, the supply capacitor is first charged to the V_{start} voltage and enters the start-up state. After a next zero-crossing of the mains voltage, the supply capacitor is charged to V_{reg} in the charging state. When the voltage at the supply capacitor exceeds V_{dis}, the gate driver outputs are enabled. When all drivers are active, the MOSFETs take over the role of the diodes which, compared to a passive diode rectifier bridge, results in lower power loss.

When the mains voltage is disconnected, the internal bias current in the discharge state discharges the supply capacitor. When the voltage at pin VCC drops to below V_{dis}, the X-capacitor discharge state is entered, which draws 2 mA of current from VR to discharge the X-capacitor. The waiting time t_d until X-capacitor discharge starts is:

$$t_d = C_{VCC} * \left(V_{reg} - V_{dis}\right) / 23\ \mu A = 0.11E6 * C_{VCC} \quad (1)$$

Using a typical value of 2.2 µF for C_{VCC} yields about 0.24 s. While VR discharges the X-capacitor, the mains can be reconnected. In that case, the charge mode is entered again. Figure 7 describes the start-up, the normal operation, and the power-off of the TEA2209T.

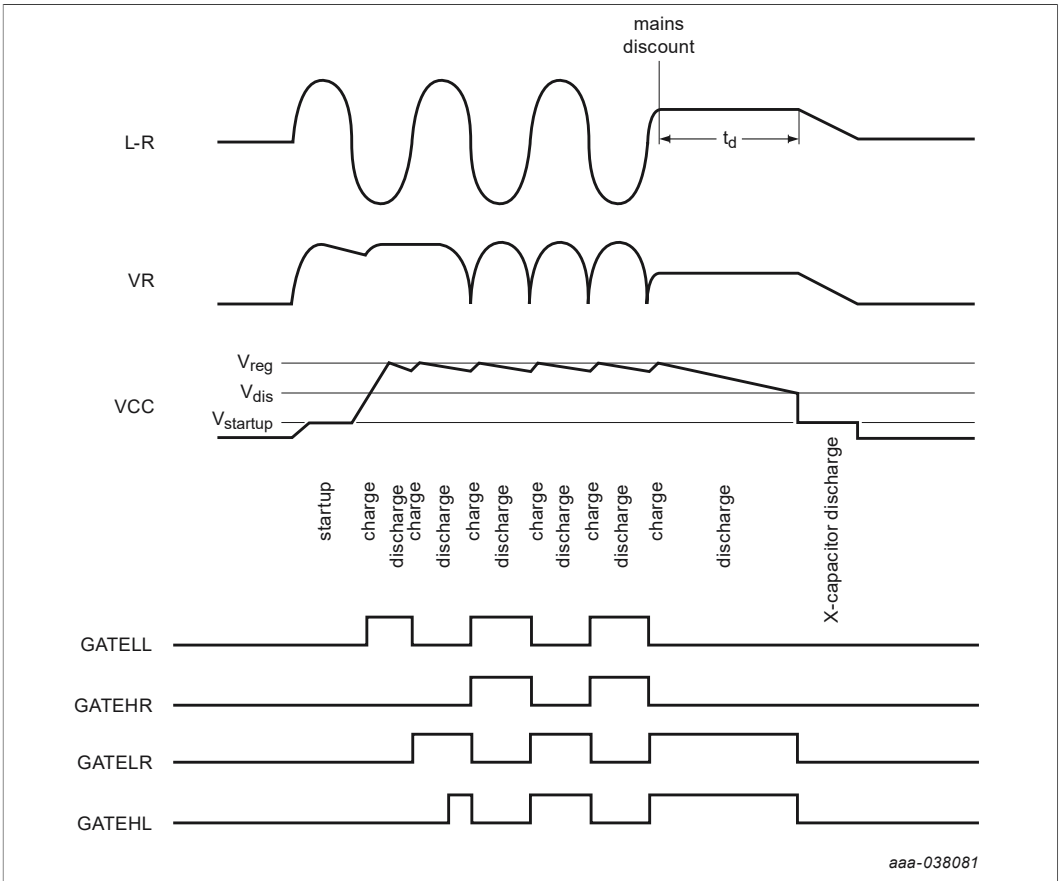


Figure 7. TEA2209T signals (start-up, normal operation and power-off)

6 Performance

6.1 Test facilities

- Oscilloscope: Agilent Technologies DSOX3034T
- AC power source: Chroma 61504
- Electronic load: Chroma 63600-2
- Digital power meter: WT210
- Power board: TEA2016DB1519

6.2 Test setup

To measure the system performance the TEA2209DB1584 is mounted on the TEA2016DB1519. The diode bridge rectifier, BD101, is removed from the TEA2016DB1519 and replaced by the TEA2209DB1584. Figure 8 shows details of the test setup.

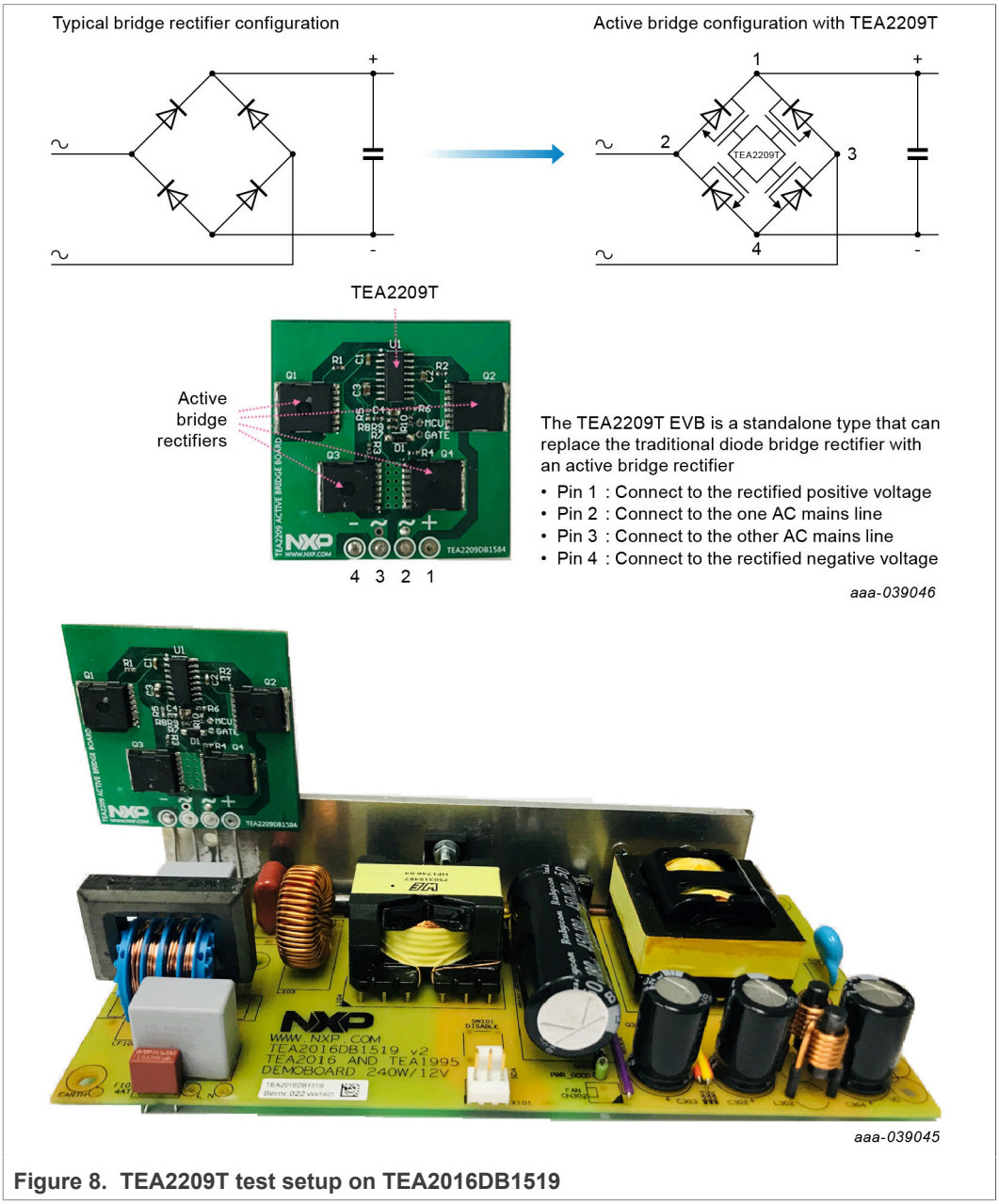


Figure 8. TEA2209T test setup on TEA2016DB1519

When the MOSFET pin open test for active bridge is required, add a diode in parallel to each active bridge MOSFET.

To enable or disable active bridge operation via the COMP pin, the TEA2209T supports an external signal. This COMP pin is connected to digital high/low signal output from the MCU or the PFC gate signal throughout RC filter. When the PFC gate signal is used, the PFC gate pin can be connected to the TEA2209DB1584 directly, because the RC filter is already implemented. When a digital high/low signal is input, remove the C4 capacitor on the TEA2209DB1584 to avoid additional delay time.

6.3 Design guideline for COMP and COMP_POL

The TEA2209T can disable gate drivers using an external signal. The external signal is connected to the COMP pin. Depending on the COMP_POL selection, either a high level or a low level on the COMP pin disables gate operation. Table 1 shows the functionality of COMP and COMP_POL. When COMP pin voltage exceeds 1.3 V, the COMP level is HIGH. When the COMP pin voltage is lower than 0.95 V, the COMP level is LOW.

Table 1. COMP and COMP_POL functionality

	COMP_POL = VCC	COMP_POL = GND
COMP HIGH	All gate drivers are disabled	All gate drivers are enabled
COMP LOW	All gate drivers are enabled	All gate drivers are disabled

Disabling all gate drivers is helpful to reduce power loss and increase efficiency at a low-load condition. A signal from a microprocessor can disable gate drivers. When there is no microprocessor on the system, the PFC gate signal can be used to disable the gate drivers at light load throughout the external circuit. Figure 9 shows an application example with PFC gate signal. The PFC gate duty-ratio, the PFC gate level, and the external resistor divider determine the COMP level. When PFC operates in burst mode, COMP level has ripple according to burst mode frequency. Whenever the ripple exceeds 1.3 V threshold, gate drivers are enabled. Section 6.5 shows the test waveform.

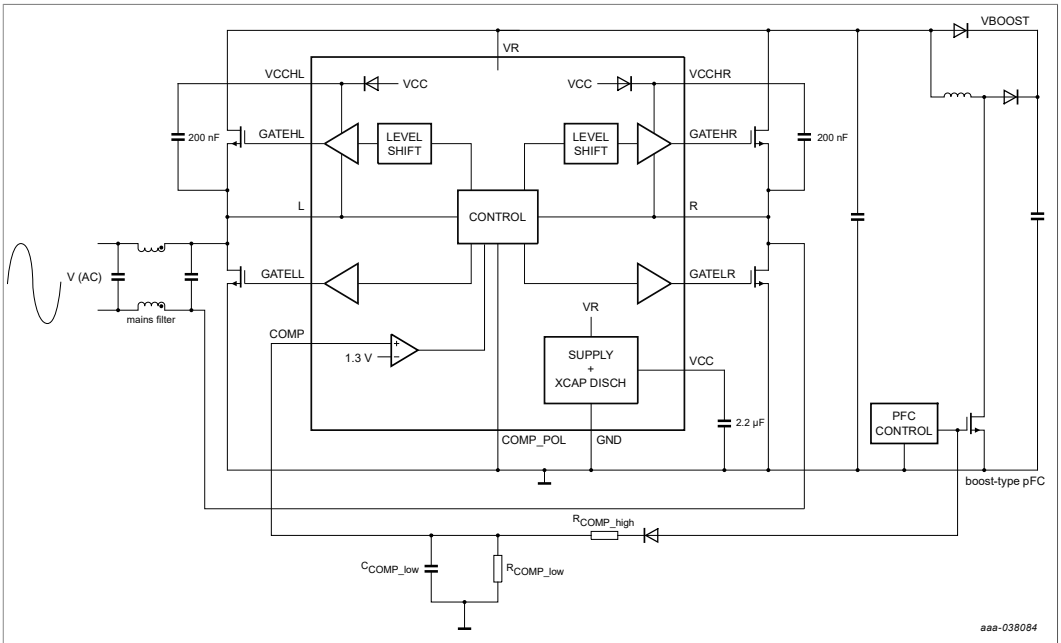


Figure 9. Application diagram example with PFC gate signal

The TEA2209DB1584 implements an external RC filter with R_{COMP_high} = 18 kΩ, R_{COMP_low} = 180 kΩ, C_{COMP_high} = 2.2 µF and 1N4148. To adjust the output power level which disables gate drivers, change R_{COMP_high}. As reducing R_{COMP_high} value, gate drivers can be disabled at lower power levels. Section 6.8.2 gives the test result with the TEA2016DB1519.

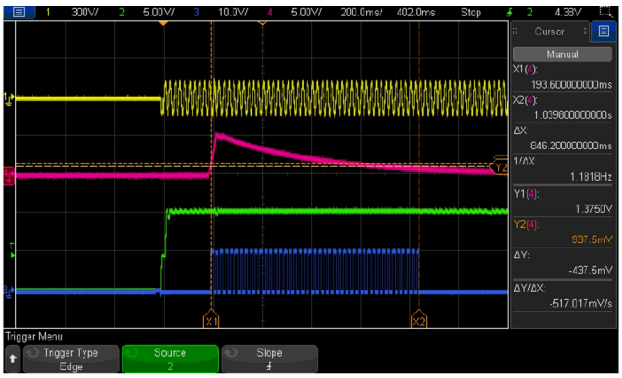
6.4 Start-up sequence

After AC mains voltage is applied, the body diodes of the MOSFET rectifiers are connected until the TEA2209T is enabled. The internal self-bias circuit from the rectified mains voltage, VR, supplies the VCC.

Depending on the output load condition, the COMP pin voltage may vary. At 264 V (AC) and a no-load condition, the TEA2209T is disabled. At 90 V (AC) and a no-load condition, however, the COMP pin level is high enough to enable the TEA2209T when PFC gate signals are available.

When the 3.3 V (DC) external source level to enable the TEA2209T is connected to the COMP pin, TEA2209T is enabled when VCC has reached the V_{start} level. As mentioned in Section 6.2, the C4 capacitor is removed from the TEA2209DB1584 demo board.

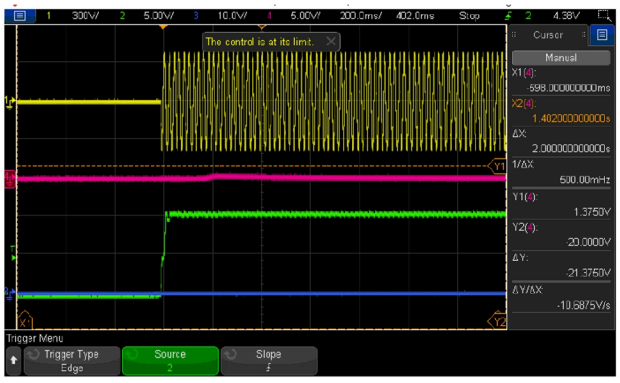
Figure 12 and Figure 13 show the start-up sequences when an external 3.3 V (DC) source is connected to COMP pin.



aaa-039049

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 200 ms/div

a. 90 V (AC)

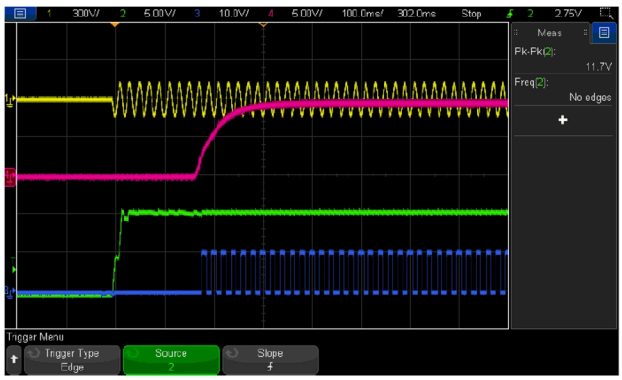


aaa-039050

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 200 ms/div

b. 264 V (AC)

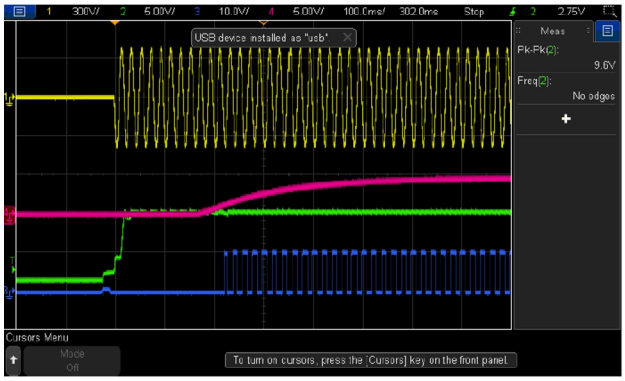
Figure 10. Start-up sequence at no load; PFC gate signal connected to COMP pin



aaa-039051

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 100 ms/div

a. 90 V (AC)



aaa-039052

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 100 ms/div

b. 264 V (AC)

Figure 11. Start-up sequence at 240 W load; PFC gate signal connected to COMP pin

aaa-039053

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

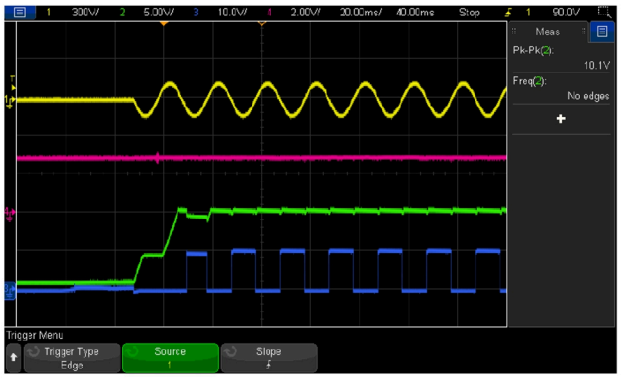
a. 90 V (AC)

aaa-039054

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

b. 264 V (AC)

Figure 12. Start-up sequence at no load; 3.3 V (DC) connected to COMP pin



aaa-039055

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

a. 90 V (AC)

aaa-039056

CH1: AC mains (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

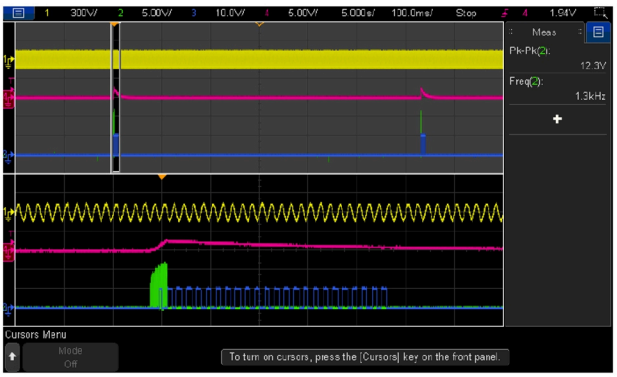
b. 264 V (AC)

Figure 13. Start-up sequence at 240 W load; 3.3 V (DC) connected to COMP pin

6.5 Normal operation

6.5.1 Connecting the PFC gate signal to the COMP pin

When the voltage between L and R is higher than 250 mV, the GATEHL and GATELR are enabled. When the voltage between L and R is below −250 mV, the GATEHR and GATELL are enabled. Depending the +250 mV and −250 mV detection thresholds, dead time occurs between the gates. At no load, the PFC of the TEA2016 operates in burst mode. Because the on-time of the PFC gate and the switching period in burst mode are long at 90 V (AC) and no load, the TEA2209T is enabled in every PFC burst period.



aaa-039059

CH1: AC mains (300 V/div)
CH2: PFC gate from TEA2016 (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 5 s/div and 100 ms/div

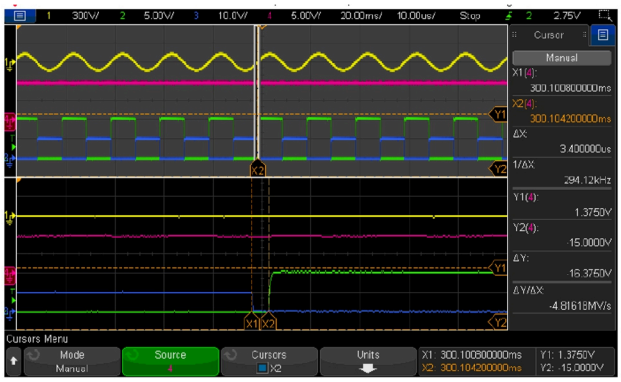
a. 90 V (AC)

aaa-039060

CH1: AC mains (300 V/div)
CH2: PFC gate from TEA2016 (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 100 ms/div

b. 264 V (AC)

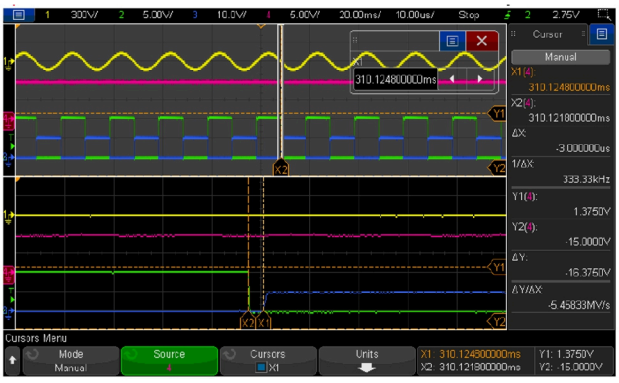
Figure 14. Normal operation at no load; the PFC gate signal is connected to the COMP pin



aaa-039062

CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 20 ms/div and 10 µs/div

a. Dead time while GATELR is enabled

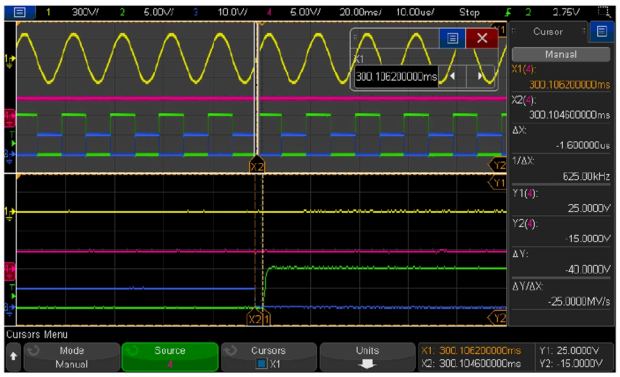


aaa-039063

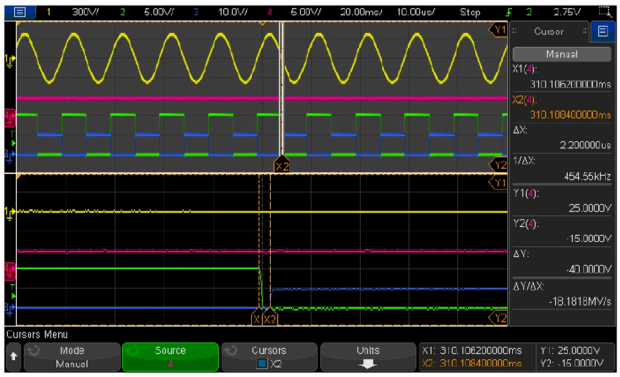
CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 20 ms/div and 10 µs/div

b. Dead time while GATELL is enabled

Figure 15. Normal operation at 90 V (AC)/240 W load; the PFC gate signal is connected to the COMP pin



aaa-039064



aaa-039065

CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 20 ms/div and 10 µs/div

a. Dead time while GATELR is enabled

CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 20 ms/div and 10 µs/div

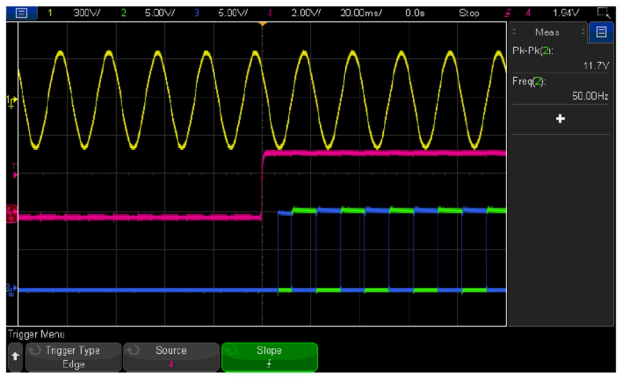
b. Dead time while GATELL is enabled

Figure 16. Normal operation at 264 V (AC)/240 W load; the PFC gate signal is connected to the COMP pin

6.5.2 Connecting the external DC signal to the COMP pin

When the COMP level exceeds 1.3 V, the TEA2209T is enabled. Before enabling the first gate signal after TEA2209 is enabled, it can have a maximum of around a half mains cycle delay time because of the MOSFET drain-source overvoltage protection. As soon as COMP level is below 0.95 V, the TEA2209T is disabled.

aaa-039066



aaa-039067

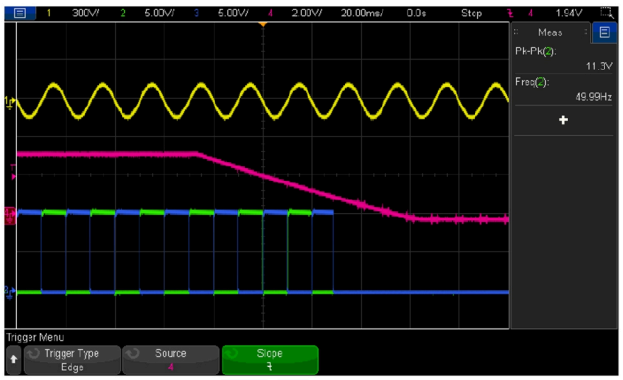
CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (5 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

a. 90 V (AC)

CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (5 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

b. 264 V (AC)

Figure 17. COMP level increase at no load condition



aaa-039068

CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (5 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

a. 90 V (AC)

aaa-039069

CH1: AC mains (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (5 V/div)
CH4: COMP (2 V/div)
Time: 20 ms/div

b. 264 V (AC)

Figure 18. COMP level decrease at no load condition

6.6 Output dynamic load condition operation

Output dynamic load is applied between 240 W and a no-load condition. The dynamic load period is 14 ms. Regardless of the output load condition, the gates operate well in alignment with the mains polarity without shoot-through. Because the output dynamic load frequency is lower than the RC filter design on the COMP pin, the COMP level is still the DC level. The COMP level is in accordance with the average output load.

aaa-039070

CH1: AC mains (300 V/div)
CH2: Output load (20 A/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 20 ms/div

a. 90 V (AC)

aaa-039071

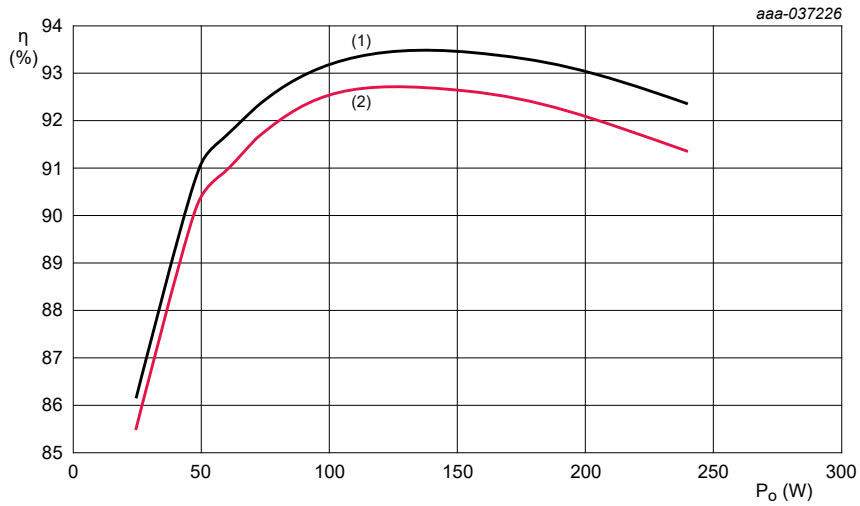
CH1: AC mains (300 V/div)
CH2: Output load (20 A/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 20 ms/div

b. 264 V (AC)

Figure 19. Dynamic load operation; the PFC gate is connected to the COMP pin

6.7 Efficiency test result and R_{DSon} selection

The efficiency test result includes power losses of bridge rectifiers and other power stages, such as PFC and LLC. However, throughout the active bridge incorporated in the TEA2209T an efficiency improvement compared a diode bridge can be seen. Depending on the different R_{DSon} values of the active bridge MOSFET, the efficiency improvement varies.

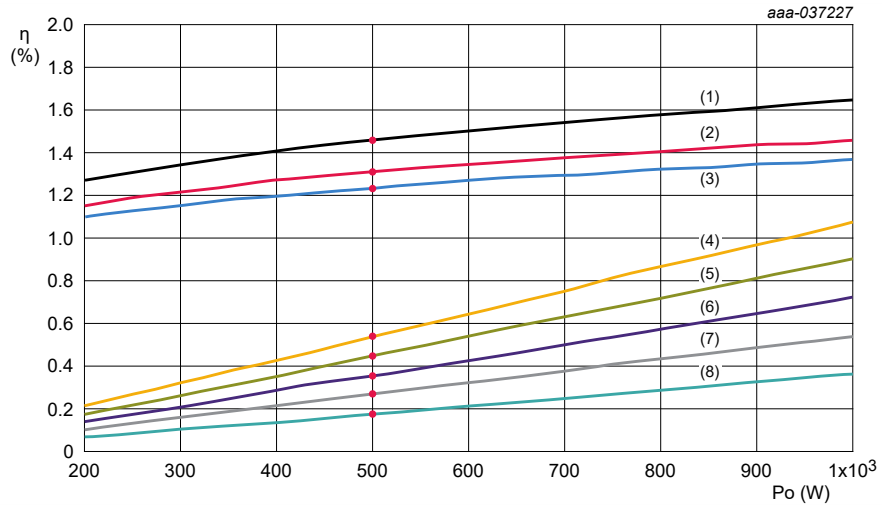


(1) Active bridge with the TEA2209T

(2) Diode bridge

Figure 20. Efficiency comparison between diode and active bridge at 115 V (AC)

Figure 21 shows the comparison between different MOSFET R_{DSon} values and the number of diodes in parallel at 115 V (AC). To see the improvement achieved with the active bridge with a MOSFET at its worst condition, the efficiency is calculated at a junction temperature of 125 °C. The efficiency improvement can reduce the temperature on the bridge rectifier. It helps to increase power density.



Efficiency drop comparison calculation based on 115 V (AC) input and a die temperature of 125 °C (bridge diode bridge: GSIB15A60;15 A; 600 V; 20 A 600 V).

(1) One diode bridge (eff_drop_Diode_125deg_onePoVin_rms)
(2) Two diode bridges parallel (eff_drop_Diode_125deg_twoPoVin_rms)
(3) Three diode bridges parallel (eff_drop_Diode_125deg_threePoVin_rms)
(4) Active bridge with MOSFET R_{DSon} = 30 mΩ (eff_drop_Active_125degPo0.030, 2, Vin_rms)
(5) Active bridge with MOSFET R_{DSon} = 25 mΩ (eff_drop_Active_125degPo0.025, 2, Vin_rms)
(6) Active bridge with MOSFET R_{DSon} = 20 mΩ (eff_drop_Active_125degPo0.02, 2, Vin_rms)
(7) Active bridge with MOSFET R_{DSon} = 15 mΩ (eff_drop_Active_125degPo0.015, 2, Vin_rms)
(8) Active bridge with MOSFET R_{DSon} = 10 mΩ (eff_drop_Active_125degPo0.01, 2, Vin_rms)

Figure 21. Efficiency improvement based on different R_{DSon} values at 115 V (AC)

Example:

When an R_{DSon} of 0.015 Ω is used on a MOSFET for a 500 W design, the efficiency improvement that can be achieved, when compared to a single diode for a diode bridge, is 1.2 %.

6.8 Standby power consumption test result and design guidelines

6.8.1 Recommended setting for low standby power consumption

When active bridge is enabled, the rectified AC mains voltage is a full-wave rectified waveform even at no-load condition. Although a full wave rectified waveform achieves a better THD performance, it can make an additional current path on capacitors (which are placed on the rectified mains voltage). The result is extra power losses on these capacitors because of ESR. To minimize standby power consumption, disable the TEA2209T via COMP pin. To disable the TEA2209T at a no-load condition, either the external DC level or the PFC gate signal can be selected. When the PFC gate signal is used, an external RC filter can adjust a power level which disables the TEA2209T.

Table 2. Standby power consumption

	115 V (AC) and no load (mW)	230 V (AC) and no load (mW)
Standby power consumption of TEA2209DB1584 standalone (COMP = low)	3.8	7.4
Standby power consumption with TEA2016DB1519	33	52

6.8.2 Enable and disable power levels; PFC gate connected to COMP pin

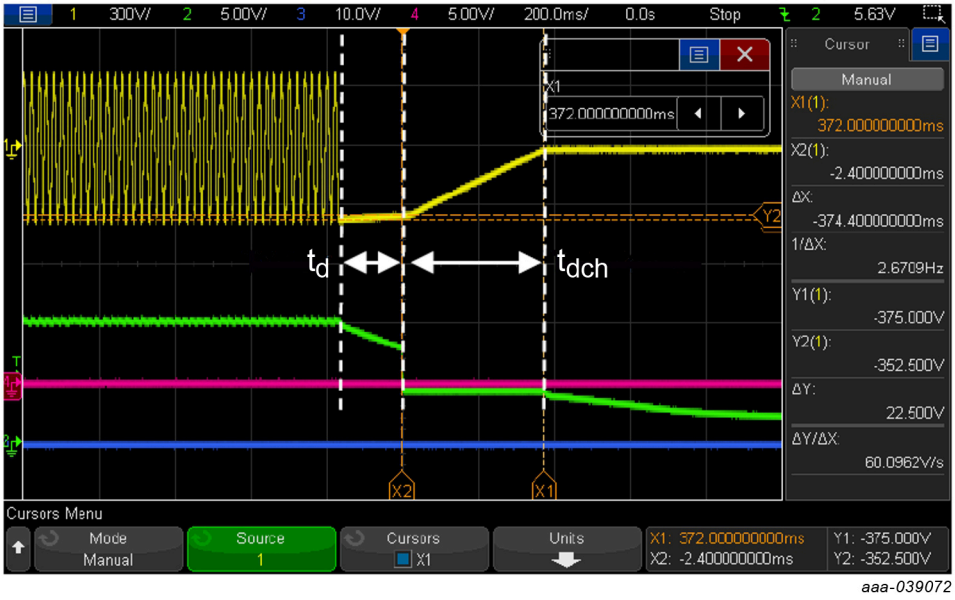
When the COMP pin is connected to PFC gate throughout external RC filter, the COMP level is increased as increasing output power level. Table 3 shows enable and disable power levels with PFC gate connection.

Table 3. Enable and disable power levels; the PFC gate is connected to the COMP pin

	90 V (AC)	115 V (AC)	230 V (AC)	264 V (AC)
TEA2209T enable power level	2.0 W	2.5 W	7.4 W	21.6 W
TEA2209T disable power level	1.8 W	2.4 W	7.2 W	13.2 W

6.9 AC power-off sequence and X-capacitor discharge test

If the X-capacitor discharge function is activated, the discharge current flows from VR to Ground via the internal path of the IC. After AC mains is disconnected, the VCC capacitor is discharged. While VCC is discharged to V_{dis}, the X-capacitor discharge current is not enabled. This delay time (t_d) can be adjusted with different VCC capacitors. After VCC is decreased to V_{dis}, the X-capacitor discharge current is enabled. It takes 370 ms to discharge the 940 nF the X-capacitor and the 1470 nF capacitor on the rectified AC mains voltage.



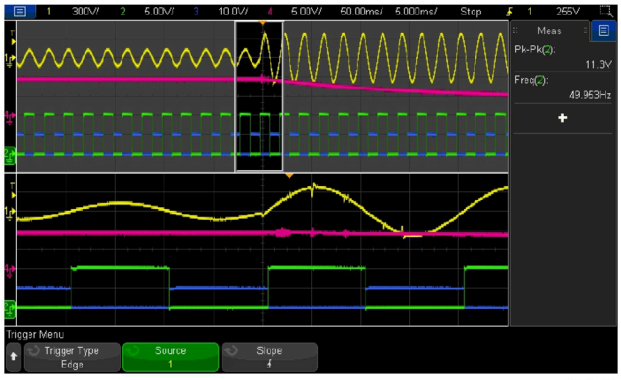
aaa-039072

CH1: AC mains voltage (300 V/div)
CH2: VCC (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 200 ms/div

Figure 22. X-capacitor discharge test at 264 V (AC) and a no-load condition; the PFC gate is connected to the COMP pin

6.10 AC mains transition test

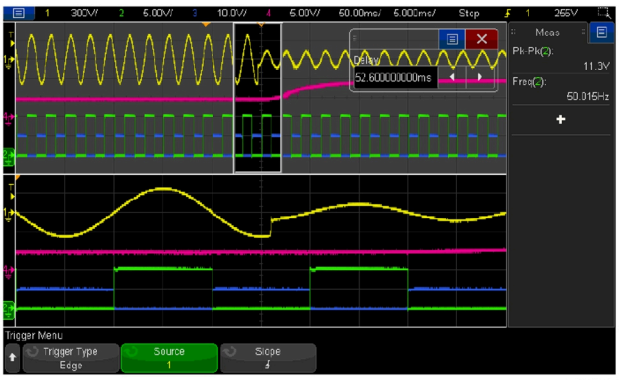
When the AC mains voltage is changed from high mains to low mains, or vice versa, no shoot-through occurs. The active bridge operates normally.



aaa-039073

CH1: AC mains voltage (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 50 ms/div and 5 ms/div

a. Mains change from 90 V (AC) to 264 V (AC)



aaa-039074

CH1: AC mains voltage (300 V/div)
CH2: GATELR (5 V/div)
CH3: GATELL (10 V/div)
CH4: COMP (5 V/div)
Time: 50 ms/div and 5 ms/div

b. Mains change from 264 V (AC) to 90 V (AC)

Figure 23. AC mains voltage transition test at a 240 W load; the PFC gate is connected to the COMP pin

6.11 Surge test result

To test the system surge, the TEA2209DB1584 is mounted on the TEA2016DB1519. In addition, one MOV, 14D511, is added between two AC mains lines. Figure 24 shows the MOV position. Surge test can pass up to 5 kV without damage, which is same test result as with the diode bridge.

Additionally, to increase power capability, the R107 and R108 resistors on the TEA2016DB1519 are changed to a metal-alloy type. The power rating of the R106 is also increased.

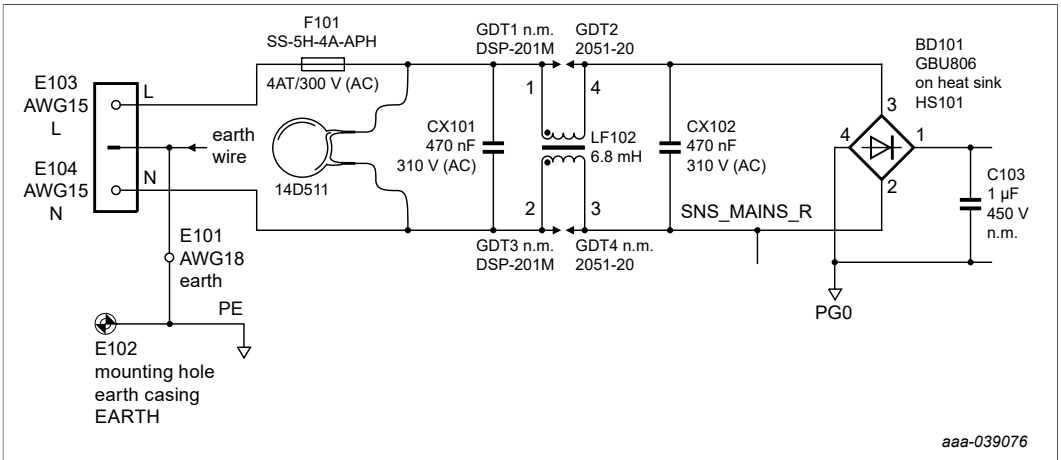


Figure 24. Circuit diagram which adding MOV 14D511 on the AC mains lines

Table 4. Surge test result, EN61000-4-5

Surge voltage (V)	Surge degree	Test result
1000	0 deg, 90 deg, 180 deg, 270 deg	pass without damage
2000	0 deg, 90 deg, 180 deg, 270 deg	pass without damage
3000	0 deg, 90 deg, 180 deg, 270 deg	pass without damage
4000	0 deg, 90 deg, 180 deg, 270 deg	pass without damage
5000	0 deg, 90 deg, 180 deg, 270 deg	pass without damage

7 Schematic

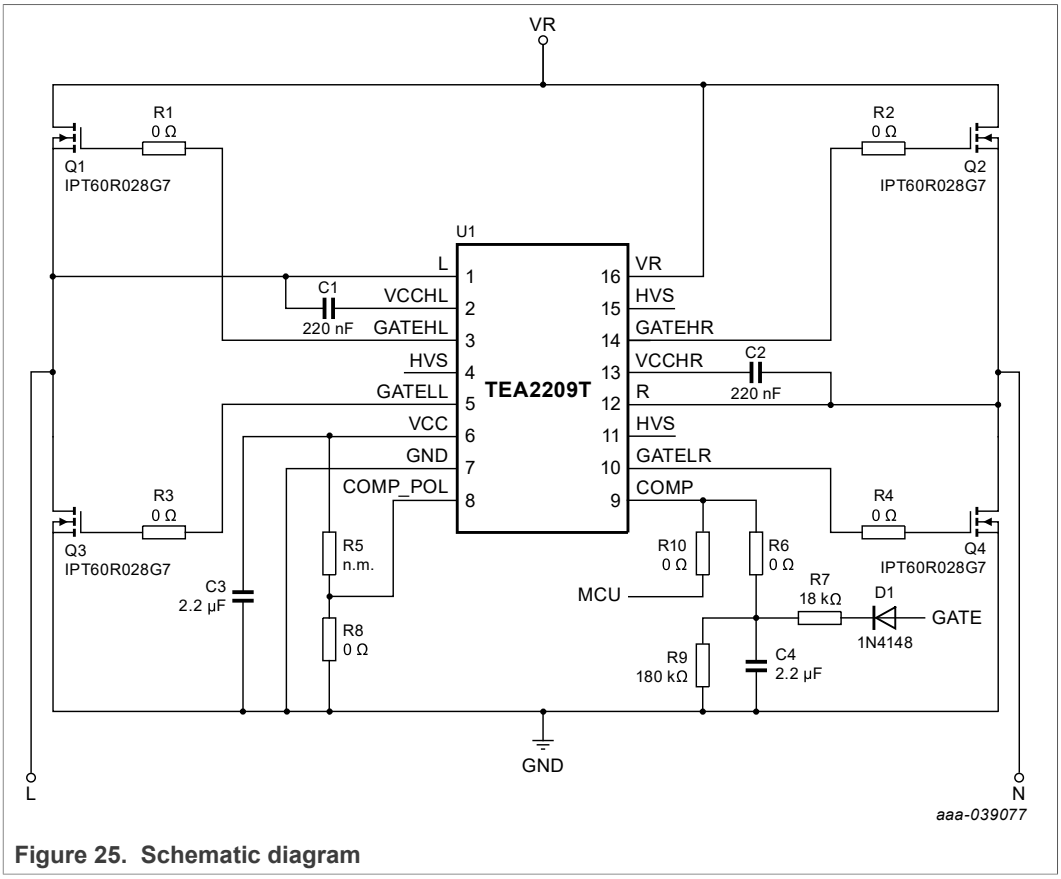


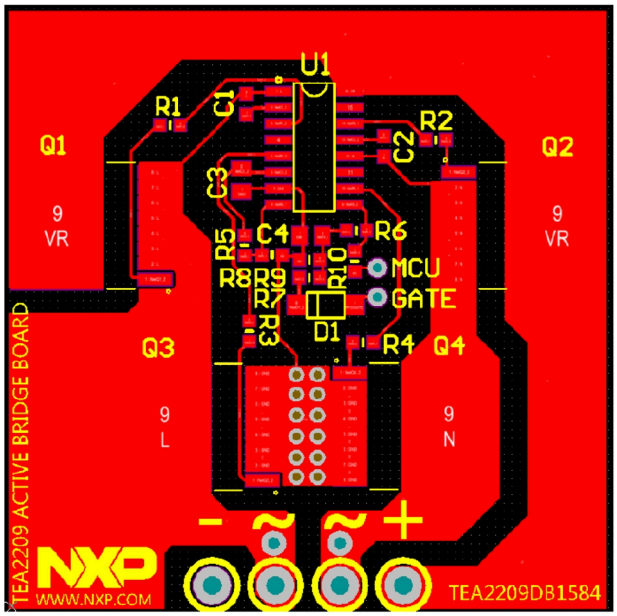
Figure 25. Schematic diagram

8 Bill of materials (BOM)

Table 5. Bill of materials (BOM)

Part reference	Values and description	Part number	Manufacturer
C1; C2	capacitor; 220 nF; 10 %; 50 V; X7R; 0603	-	-
C3; C4	capacitor; 2.2 µF; 10 %; 25 V; X7R; 0805		
Q1; Q2; Q3; Q4	MOSFET-N; 600 V; 75 A	IPT60R028G7	Infineon
R1; R2; R3; R4; R6; R8; R10	resistor; jumper; 0 Ω;100 mW; 0603	-	-
R5	resistor; not mounted; jumper; 0 Ω;100 mW; 0603	-	-
R7	resistor; jumper; 18 kΩ; 100 mW; 0603	-	-
R9	resistor; jumper; 180 kΩ; 100 mW; 0603	-	-
D1	diode; fast switching; SOD123	1N4148W	Diodes
U1	active bridge rectifier controller	TEA2209T	NXP Semiconductors

9 Layout



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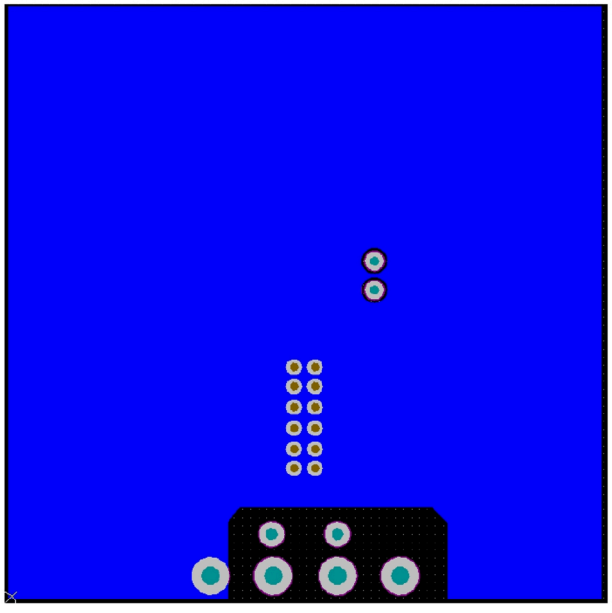
a. Front view layout and assembly



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b. Back view layout and assembly

Figure 26. TEA2209DB1584 demo board layout

10 Abbreviations

Table 6. Abbreviations

Acronym	Description
MOSFET	metal-oxide semiconductor field-effect transistor
UVLO	undervoltage lockout
THD	total harmonic distortion
PCB	printed-circuit board

11 References

[1] **TEA2209T data sheet** — Active bridge rectifier controller; 2020, NXP Semiconductors

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