UM11214

KITPF8121FRDMEVM evaluation board

Rev. 1.0 — 22 April 2019 User guide

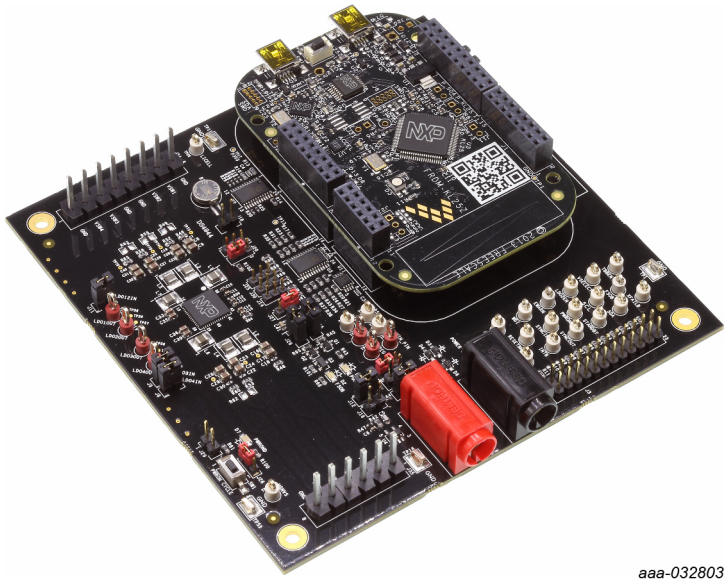

Figure 1. KITPF8121FRDMEVM

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This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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1 Introduction

This document is the user guide for the KITPF8121FRDMEVM evaluation board. This document is intended for the engineers involved in the evaluation, design, implementation, and validation of multi-channel power management integrated circuit PF8121.

The scope of this document is to provide the user with information to evaluate the multi-channel power management integrated circuit PF8121. This document covers connecting the hardware, installing the software and tools, configuring the environment and using the kit.

The KITPF8121FRDMEVM customer evaluation board provides full access to all the features in the PF8121 device.

Table 1. Device support

Evaluation board	PMIC device	Link
KITPF8121FRDMEVM	PF8121	http://www.nxp.com/KITPF8121FRDMEVM

2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for KITPF8121FRDMEVM evaluation board is at http://www.nxp.com/KITPF8121FRDMEVM. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a **Getting Started** tab. The **Getting Started** tab provides quick-reference information applicable to using the KITPF8121FRDMEVM evaluation board, including the downloadable assets referenced in this document.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, ask and answer technical questions, and receive input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 Getting ready

Working with the KITPF8121FRDMEVM requires the kit contents, additional hardware and a Windows PC workstation with installed software.

3.1 Kit contents

- Assembled and tested evaluation board and preprogrammed FRDM-KL25Z microcontroller board in an anti-static bag
- 3.0ft. USB-STD A to USB-B-mini cable
- Quick Start Guide

3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 3.0 V to 5.0 V and a current limit set initially to 1.0 A (maximum current consumption can be up to 7.0 A)

3.3 Windows PC workstation

This evaluation board requires a Windows PC workstation. Meeting these minimum specifications should produce great results when working with this evaluation board.

- USB-enabled computer with Windows 7, Windows 8, or Windows 10

3.4 Software

Installing software is necessary to work with this evaluation board. All listed software is available on the evaluation board's information page at http://www.nxp.com/KITPF8121FRDMEVM or from the provided link.

Software package NXP_FlexGUI_PF8x_Rev_0.7.x or higher contains:

- KL25Z firmware files
- NXP PF8x FlexGUI

4 Getting to know the hardware

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state-of-the-art systems.

4.1 Kit overview

The KITPF8121FRDMEVM is a customer evaluation board featuring the PF8121 power management IC. The kit integrates all hardware needed to fully evaluate the PMIC.

It integrates a communication bridge based on the FRDM-KL25Z freedom board to interface with the FlexGUI software interface to fully configure and control the PF8121 PMIC.

4.1.1 KITPF8121FRDMEVM features

Buck regulators

- SW1, SW2, SW3, SW4, SW5, SW6: 0.4 V to 1.8 V; 2500 mA; 2 % accuracy and dynamic voltage scaling and single, dual, triple or quad-phase configuration
- SW7; 1.0 V to 4.1 V; 2500 mA; 2 % accuracy
- Configurable VTT termination mode on SW6
- Programmable current limit
- Spread-spectrum and manual tuning of switching frequency

LDO regulators

- 4x LDO regulator 1.5 V to 5.0 V, 400 mA: 3 % accuracy with optional load switch mode
- Selectable hardware/software control on LDO2

RTC supply VSNVS 1.8 V/3.0 V/3.3 V, 10 mA

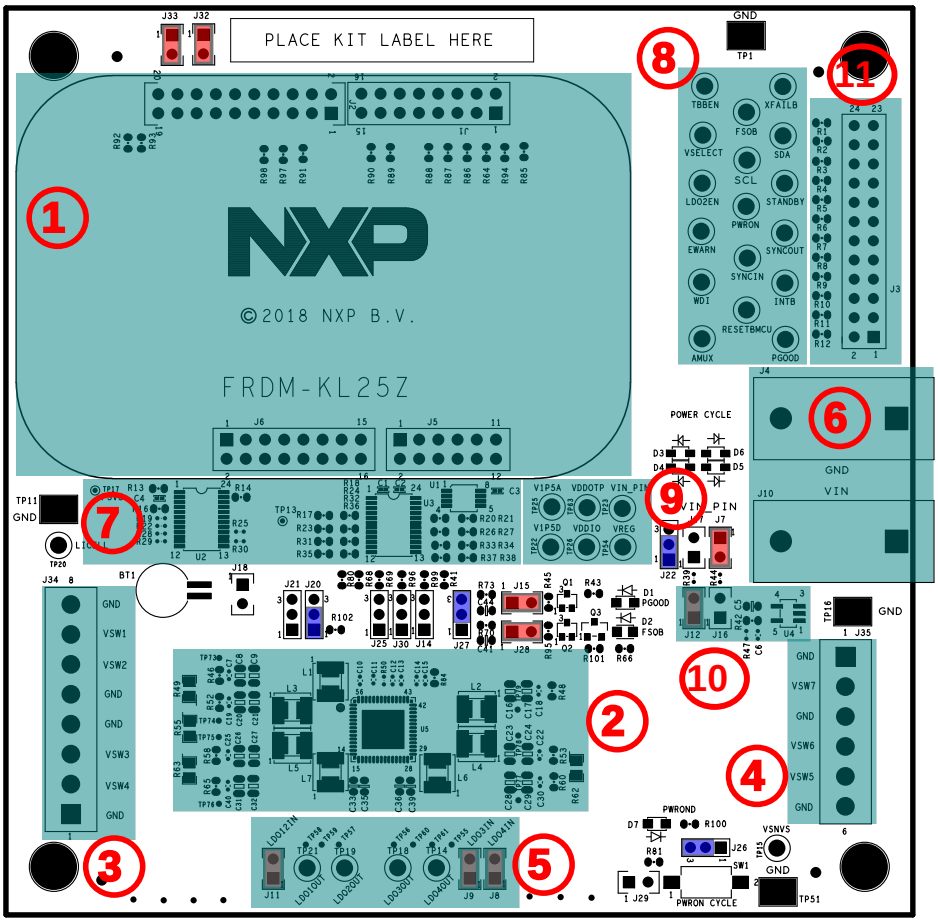
- Battery backed memory including coin cell charger with programmable charge current and voltage

System features

- 2.5 to 5.5 V operating input voltage range
- USB to I^2C communication via the FRDM-KL25Z interface
- Selectable hardwire default PMIC configuration or OTP/TBB operation
- Fast mode I^2C communication at 400 kHz (high speed operation supported by PMIC)
- Advance system monitoring/diagnostic via PMIC and/or system AMUX
- Master/slave interface connector
- Onboard I/O regulator with 1.8 V/3.3 V selectable output voltage

4.2 Kit featured components

Figure 2 identifies important components on the board.



1. FRDM-KL25Z Freedom board connector
2. PF8121 PMIC
3. SW1 to SW4 power connector
4. SW5 to SW7 power connector
5. LDO output test points
6. Input power banana jack
7. External analog multiplexer
8. PMIC I/O test points
9. Analog supplies test points
10. 1.8 V/3.3 V external LDO regulator
11. Master/slave interface connector

Figure 2. Evaluation board featured component locations

4.2.1 PF8121: 12-channel power management integrated circuit for high performance applications

4.2.1.1 General description

The PF8121 is a power management integrated circuit (PMIC) designed for high performance consumer applications. It features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals.

Built-in one time programmable memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C after start up offering flexibility for different system states.

PF8121 is the consumer version of the higher end device, it features seven switching regulators and four LDOs, providing same power management and digital control with standard consumer qualification rating to address a cost effective platform for consumer applications.

4.2.1.2 Features

- Up to seven high efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog timer/monitor
- Voltage and system monitoring circuits
- One time programmable device configuration
- 3.4 MHz I^2C communication interface
- 56-pin 8 x 8 QFN package

4.3 Schematic, board layout and bill of materials

The board layout and bill of materials for the KITPF8121FRDMEVM evaluation board are available at http://www.nxp.com/KITPF8121FRDMEVM.

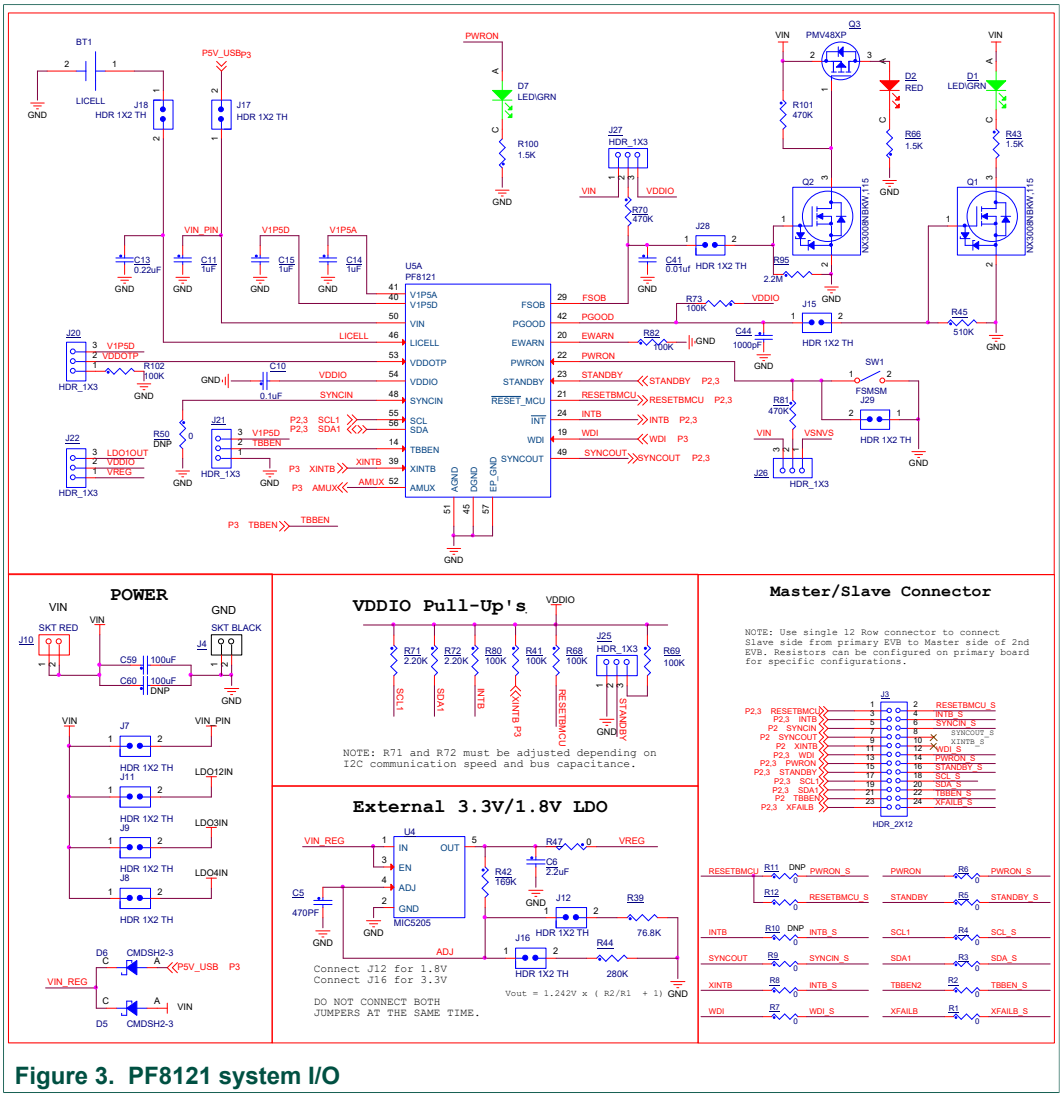


Figure 3. PF8121 system I/O

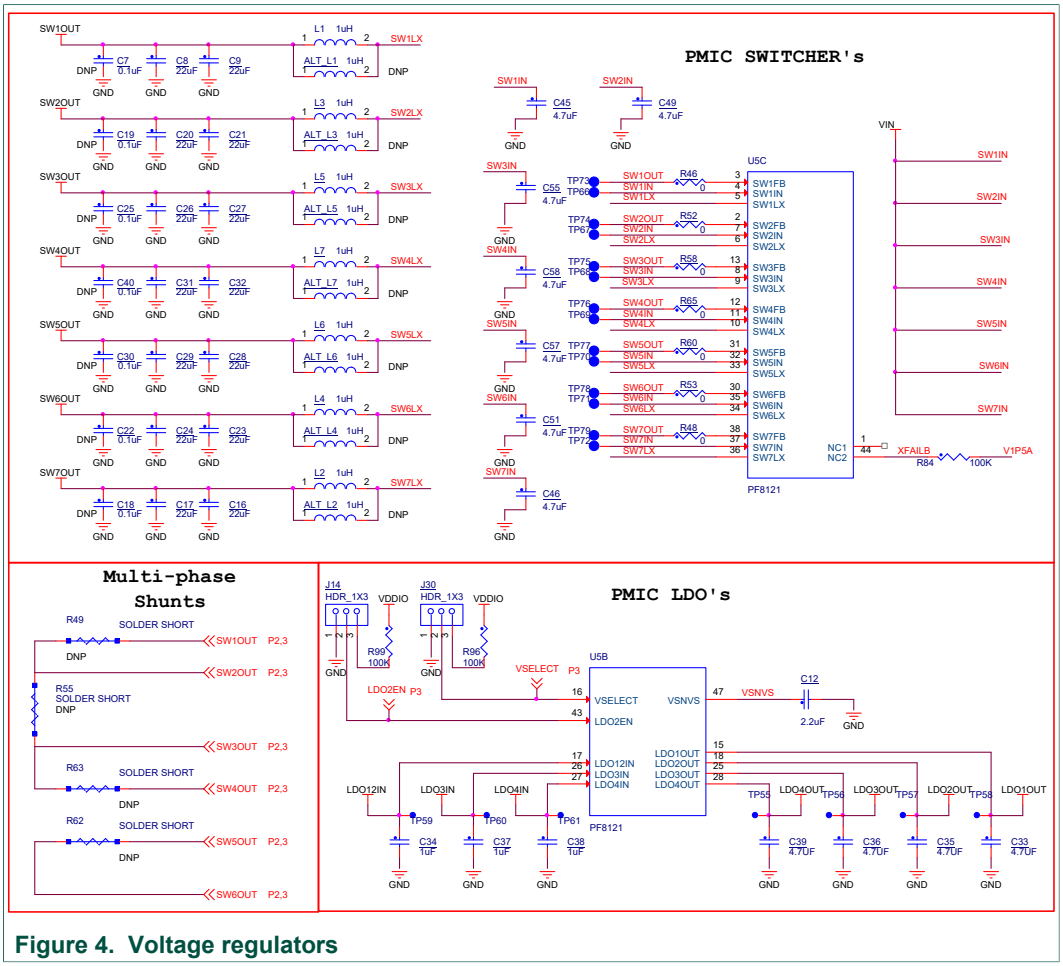


Figure 4. Voltage regulators

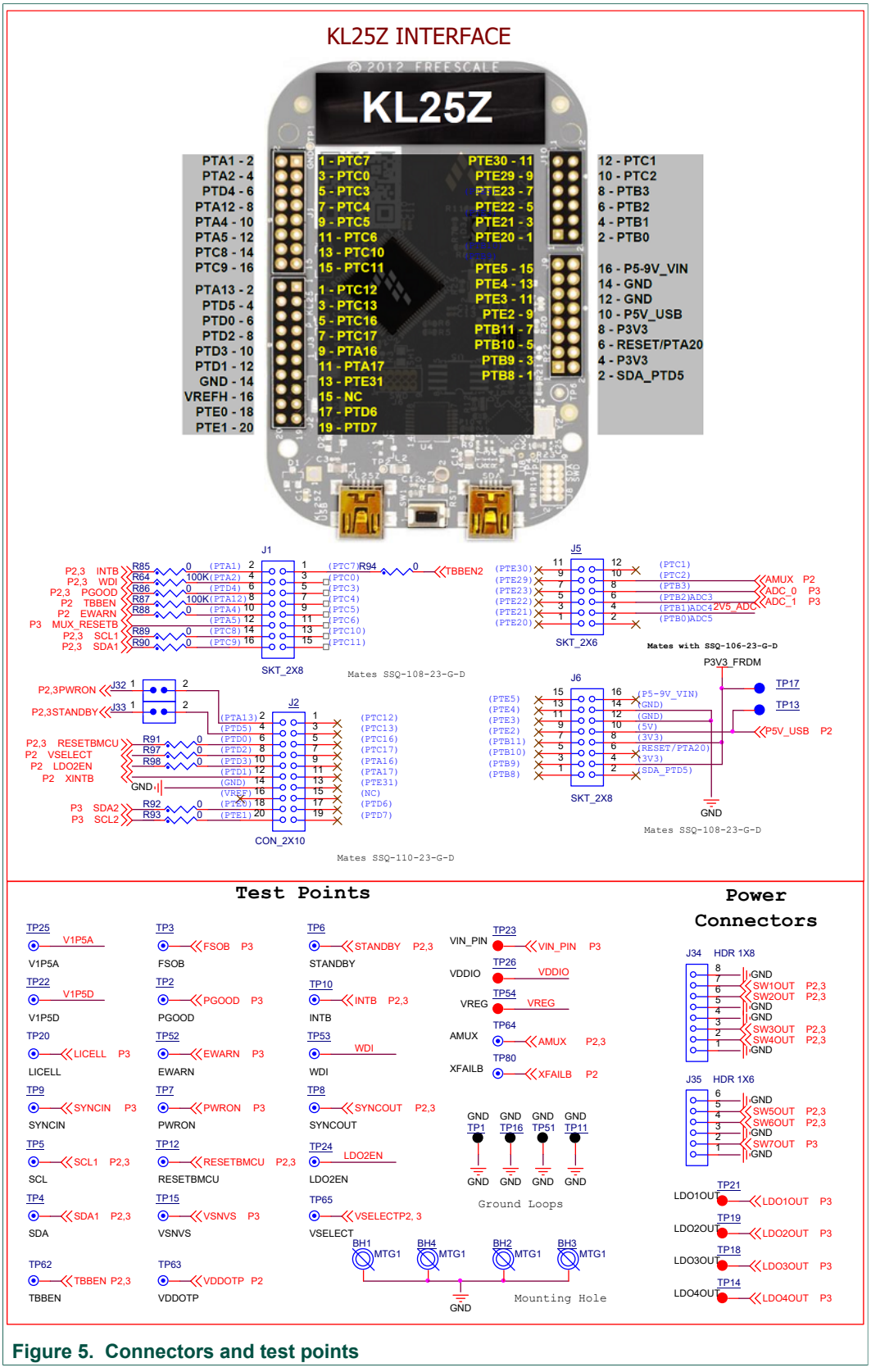


Figure 5. Connectors and test points

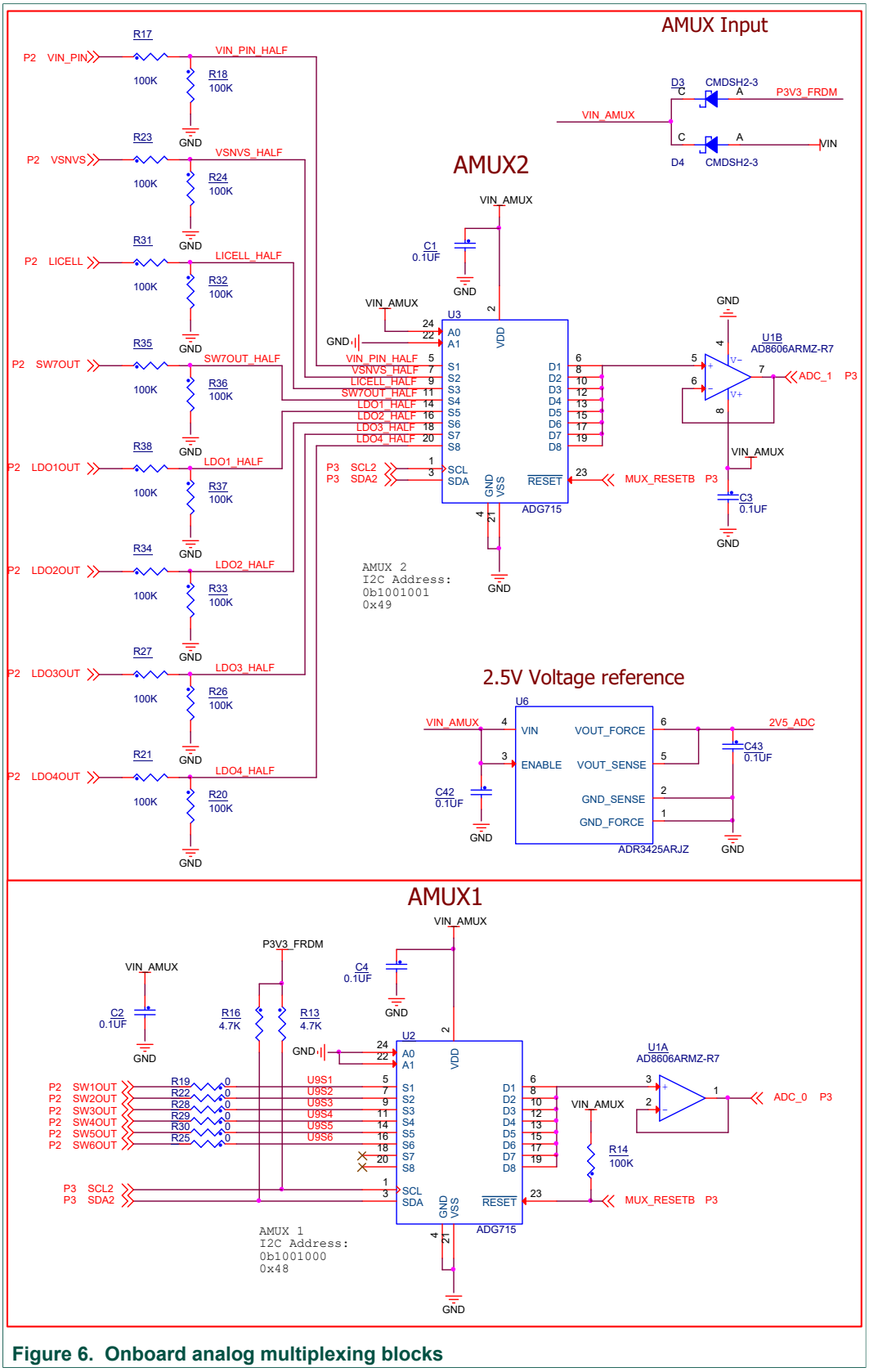


Figure 6. Onboard analog multiplexing blocks

4.4 Default jumper configurations

Table 2. Evaluation board jumper descriptions

Name	Default	Description
J1, J2, J5, J6	—	Freedom board interface
J3	—	Master/slave connector • Odd row is connected directly to pins in the Master board • Even row is used to connect a Slave board signals • Interface connection is made via shunt resistors R1 to R11
J7	Shorted	Connects PMIC VIN to main board VIN node
J8	Shorted	Connects LDO4IN to main board VIN node
J9	Shorted	Connects LDO3IN to main board VIN node
J11	Shorted	Connects LDO12IN to main board VIN node
J12	Shorted	Selects the external LDO voltage • J12 → 1.8 V • J16 → 3.3 V
J16	Open	
J14	Open	LDO2EN pin control • 1-2 → LDO2EN pin pulled low • 2-3 → LDO2EN pin pulled high • Open → full MCU control with no pull up
J15	Shorted	Enables the PGOOD green LED
J17	Open	Supplies PMIC VIN from 5.0 V supply on Freedom Board (used only for demo functional operation, no loading capability in this operation mode)
J18	Open	Connects coin cell to the LICELL node
J20	1-2 shorted	Selects PF8121 default register configuration • 1-2 → OTP mode • 2-3 → Hardwire mode
J21	Open	Enables TBB mode on PF8121 device • 1-2 → TBB mode disabled • 2-3 → TBB mode enabled • Open → MCU has control of this pin
J22	1-2 shorted	Selects VDDIO supply • 1-2 → VDDIO is supplied by external LDO regulator • 2-3 → VDDIO is supplied by LDO1
J25	Open	Selects STANDBY pin voltage level • 1-2 → STANDBY pin low • 2-3 → STANDBY pin high • Open → STANDBY pin controlled by MCU
J26	2-3 shorted	Controls PWRON pull up source • 1-2 → PWRON pulled up to VSNVS • 2-3 → PWRON pulled up to VIN • Open → full MCU control with no pull up
J27	2-3 shorted	Selects pull up for FSOB pin • 1-2 → FSOB pulled up to VIN • 2-3 → FSOB pulled up to VDDIO
J28	Shorted	Enables the FSOB red LED
J29	Open	Pulls down PWRON pin to ground

Name	Default	Description
J30	Open	VSELECT pin control • 1-2 → VSELECT pin pulled low • 2-3 → VSELECT pin pulled low • Open → full MCU control with no pull up
J32	Shorted	PWRON connection from PMIC to MCU
J33	Shorted	STANDBY connection from PMIC to MCU

4.5 Test points

Table 3. Evaluation board test point descriptions

Name (label)	Signal name	Description
Ground test points		
TP1, TP11, TP16, TP51 (GND)	GND	Ground plane test points
Digital I/O signal		
TP2 (PGOOD)	PGOOD	Connected to pin 42 (PGOOD) on PMIC
TP3 (FSOB)	FSOB	Connected to pin 29 (FSOB) on PMIC
TP4 (SDA)	SDA1	Connected to pin 56 (SDA) on PMIC. Main system I^2C bus.
TP5 (SCL)	SCL1	Connected to pin 55 (SCL) on PMIC. Main system I^2C bus.
TP6 (STANDBY)	STANDBY	Connected to pin 23 (STANDBY) on PMIC
TP7 (PWRON)	PWRON	Connected to pin 22 (PWRON) on PMIC
TP8 (SYNCOUT)	SYNCOUT	Connected to pin 49 (SYNCOUT) on PMIC
TP9 (SYNCIN)	SYNCIN	Connected to pin 48 (SYNCIN) on PMIC
TP10 (INTB)	INTB	Connected to pin 24 (INTB) on PMIC
TP12 (RESETBMCU)	RESETBMCU	Connected to pin 21 (RESETBMCU) on PMIC
TP24 (LDO2EN)	LDO2EN	Connected to pin 43 (LDO2EN) on PMIC
TP52 (EWARN)	EWARN	Connected to pin 20 (EWATN) on PMIC
TP53 (WDI)	WDI	Connected to pin 19 (WDI) on PMIC
TP62 (TBBEN)	TBBEN	Connected to pin 14 (TBBEN) on PMIC
TP65 (VSELECT)	VSELECT	Connected to pin 16 (VSELECT) on PMIC
TP80 (XFAILB)	XFAILB	Connected to pin 44 (XFAILB) on PMIC
Analog signals		
TP15 (VSNVS)	VSNVS	Connected to pin 47 (VSNVS) on PMIC
TP20 (LICELL)	LICELL	Connected to pin 46 (LICELL) on PMIC
TP22 (V1P5D)	V1P5D	Connected to pin 40 (V1P5D) on PMIC
TP23 (VIN_PIN)	VIN_PIN	Connected to pin 50 (VIN) on PMIC
TP25 (V1P5A)	V1P5A	Connected to pin 41 (V1P5A) on PMIC
TP26 (VDDIO)	VDDIO	Connected to pin 54 (VDDIO) on PMIC
TP54 (VREG)	VREG	1.8 V or 3.3 V external regulator output
TP63 (VDDOTP)	VDDOTP	Connected to pin 53 (VDDOTP) on PMIC
TP64 (AMUX)	AMUX	Connected to pin 52 (AMUX) on PMIC
LDO test points		
TP14 (LDO4OUT)	LDO4OUT	Power path for the LDO4 output

Name (label)	Signal name	Description
TP18 (LDO3OUT)	LDO3OUT	Power path for the LDO3 output
TP19 (LDO2OUT)	LDO2OUT	Power path for the LDO2 output
TP21 (LDO1OUT)	LDO1OUT	Power path for the LDO1 output
TP55	LDO4OUT sense	LDO4 output sense path. Connected directly to pin 28 (LDO4OUT) on PMIC.
TP56	LDO3OUT sense	LDO3 output sense path. Connected directly to pin 25 (LDO3OUT) on PMIC.
TP57	LDO2OUT sense	LDO2 output sense path. Connected directly to pin 18 (LDO2OUT) on PMIC.
TP58	LDO1OUT sense	LDO1 output sense path. Connected directly to pin 15 (LDO1OUT) on PMIC.
TP59	LDO12IN sense	LDO1 and LDO2 input sense path. Connected directly to pin 17 (LDO12IN) on PMIC.
TP60	LDO3IN sense	LDO3 input sense path. Connected directly to pin 26 (LDO3IN) on PMIC.
TP61	LDO4IN sense	LDO4 input sense path. Connected directly to pin 27 (LDO4IN) on PMIC.
Switching regulator test points		
TP66	SW1IN sense	SW1 input sense path. Connected directly to pin 4 (SW1IN) on PMIC.
TP67	SW2IN sense	SW2 input sense path. Connected directly to pin 7 (SW2IN) on PMIC.
TP68	SW3IN sense	SW3 input sense path. Connected directly to pin 8 (SW3IN) on PMIC.
TP69	SW4IN sense	SW4 input sense path. Connected directly to pin 11 (SW4IN) on PMIC.
TP70	SW5IN sense	SW5 input sense path. Connected directly to pin 32 (SW5IN) on PMIC.
TP71	SW6IN sense	SW6 input sense path. Connected directly to pin 35 (SW6IN) on PMIC.
TP72	SW7IN sense	SW7 input sense path. Connected directly to pin 37 (SW7IN) on PMIC.
TP73	SW1OUT sense	SW1 output sense path. Connected directly to pin 3 (SW1FB) on PMIC through R46.
TP74	SW2OUT sense	SW2 output sense path. Connected directly to pin 2 (SW2FB) on PMIC through R52.
TP75	SW3OUT sense	SW3 output sense path. Connected directly to pin 13 (SW3FB) on PMIC through R58.
TP76	SW4OUT sense	SW4 output sense path. Connected directly to pin 12 (SW4FB) on PMIC through R65.
TP77	SW5OUT sense	SW5 output sense path. Connected directly to pin 31 (SW5FB) on PMIC through R60.
TP78	SW6OUT sense	SW6 output sense path. Connected directly to pin 30 (SW6FB) on PMIC through R53.
TP79	SW7OUT sense	SW7 output sense path. Connected directly to pin 38 (SW7FB) on PMIC through R48.

4.6 Connectors

4.6.1 V_{IN} input power connector

V_{IN} is supplied to the board through standard banana jacks.

Table 4. V_{IN} Banana connectors

Schematic label	Signal name	Description
J4	GND	Main system ground
J10	V_{IN}	Main system input power supply System operating range from 2.5 V to 5.5 V

4.6.2 Switching regulators output power connectors

Table 5. SW1 through SW4 output power connector (J34)

Schematic label	Signal name	Description
J34-1	GND	System ground
J34-2	SW4OUT	SW4 regulator output
J34-3	SW3OUT	SW3 regulator output
J34-4	GND	System ground
J34-5	GND	System ground
J34-6	SW2OUT	SW2 regulator output
J34-7	SW1OUT	SW1 regulator output
J34-8	GND	System ground

Table 6. SW5 through SW7 output power connector (J35)

Schematic label	Signal name	Description
J34-1	GND	System ground
J34-2	SW7OUT	SW7 regulator output
J34-3	GND	System ground
J34-4	SW6OUT	SW6 regulator output
J34-5	SW5OUT	SW5 regulator output
J34-6	GND	System ground

4.6.3 Interface connector

Table 7. Master/slave interface connector (J3)

Schematic label	Signal name	Description
J3-1	RESETBMCU	Direct connection to RESETBMCU pin on board
J3-2	RESETBMCU_S	Connection to external RESETBMU signal from slave PMIC • RESETBMCU_S may be connected to local RESETBMCU pin through R12 (default)
J3-3	INTB	Direct connection to INTB pin on board

Schematic label	Signal name	Description
J3-4	INTB_S	Connection to external INTB signal from slave PMIC • INTB_S may be connected to local INTB pin through R10 (optional) • INTB_S may be connected to local XINTB pin through R8 (default)
J3-5	SYNCIN	Direct connection to SYNCIN pin on board.
J3-6	SYNCIN_S	Connection to external SYNCIN signal from slave PMIC • SYNCIN_S may be connected to local SYNCOUT pin through R9 (default)
J3-7	SYNCOUT	Direct connection to SYNCOUT pin on board
J3-8	n.c.	not connected
J3-9	XINTB	Direct connection to XINTB pin on board
J3-10	n.c.	not connected
J3-11	WDI	Direct connection to WDI pin on board
J3-12	WDI_S	Connection to external WDI signal from slave PMIC • WDI_S may be connected to local WDI pin through R7 (default)
J3-13	PWRON	Direct connection to PWRON pin on board
J3-14	PWRON_S	Connection to external PWRON signal from slave PMIC. • PWRON_S may be connected to RESETBMCU pin through R11 (optional) • PWRON_S may be connected to PWRON pin through R6 (default)
J3-15	STANDBY	Direct connection to STANDBY pin on board
J3-16	STANDBY_S	Connection to external STANDBY signal from slave PMIC • STANDBY_S may be connected to STANDBY pin through R5 (default)
J3-17	SCL1	Direct connection to SCL1 signal on board
J3-18	SCL_S	Connection to external SCL signal from slave PMIC • SCL_S may be connected to SCL1 pin through R4 (default)
J3-19	SDA1	Direct connection to SDA1 signal on board
J3-20	SDA_S	Connection to external SDA signal from slave PMIC • SDA_S may be connected to SDA1 pin through R3 (default)
J3-21	TBBEN	Direct connection to TBBEN pin on board
J3-22	TBBEN_S	Connection to external TBB signal from slave PMIC • TBBEN_S may be connected to TBBEN2 signal controlled by MCU through R2 (default)
J3-23	XFAIL	Direct connection to XFAILB pin on board
J3-24	XFAIL_S	Connection to external XFAILB signal from slave PMIC • XFAILB_S may be connected to XFAILB signal on PMIC through R1 (default)

5 Installing and configuring software and tools

The KITPF8121FRDMEVM uses FlexGUI software for PF8121 device. Prior to the installation of the FlexGUI software and performing device firmware updates (if needed), download and unzip the NXP_FlexGUI_PF8x_REV_0.7.x.zip file to any desired location.

The installation package is available at http://www.nxp.com/KITPF8121FRDMEVM.

5.1 Installing the Java JRE

1. Download Java JRE (Java SE Runtime Environment), available at http://www.oracle.com/technetwork/java/javase/downloads/jre8-downloads-2133155.html (8u162 or newer).
2. Open the installer and follow the installation instructions.
3. Following the successful installation, restart the computer.

5.2 Installing FlexGUI software package

The FlexGUI software installation requires only extracting the zip file in a desired location.

1. If necessary, install the Java JRE and Windows 7 FlexGUI driver.
2. Download the latest FlexGUI (32-bit or 64-bit) version, NXP_FlexGUI_PF8x_REV_0.7.x.zip, available at http://www.nxp.com/KITPF8121FRDMEVM.
3. Extract all the files to a desired location on your PC.

FlexGUI is started by running the batch file, NXP_FlexGUI_PF8x_Rev_0.7.x\NXP FlexGUI\bin\flexgui-app-pf8xxxx.bat.

The FlexGUI Rev 0.7.0 or higher, interfaces with the FRDM-KL25Z freedom board via USB-HID protocol which should be recognized automatically by the Windows OS eliminating the need for any extra hardware drivers. See Section 5.4 "Updating the PF8121 FlexGUI firmware" for details on how to update the FRDM-KL25Z, in case the board is not loaded with the latest firmware with USB-HID support.

5.3 Uninstalling the application

The FlexGUI software does not store any files outside of its installation folder.

To uninstall FlexGUI, delete the flexgui.

5.4 Updating the PF8121 FlexGUI firmware

The FRDM-KL25Z freedom board is used as a communication bridge to interface the FlexGUI with the PMIC and other I^2C devices. The firmware is organized in three levels:

1. At first level, the SDA uses the BOOTLOADER to operate as the main path to flash the functional code of the SDA processor. The BOOTLOADER is preprogrammed on the FRDM-KL25Z freedom boards and cannot be reflashed to avoid permanent damage to the Freedom board.
2. At second level, the SDA provides a *firmware loader* for drag and drop update of the KL25Z MCU firmware.

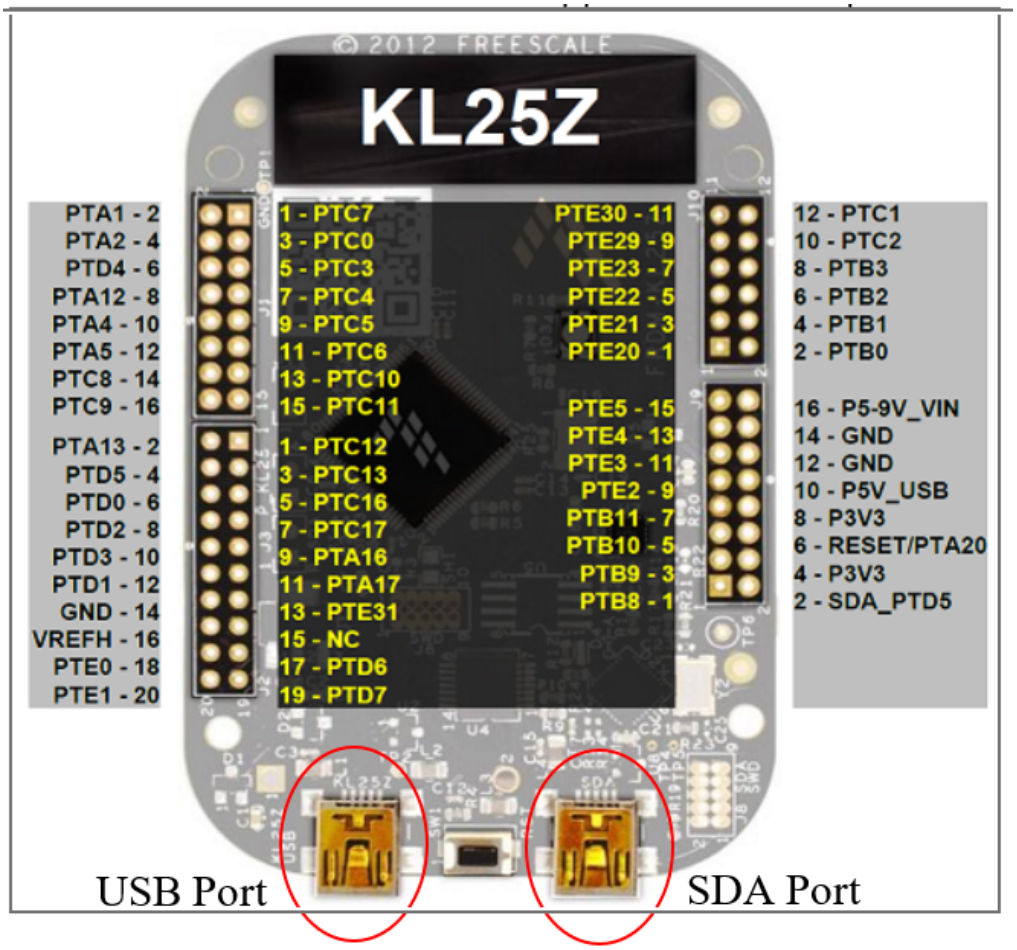
3. At the third level, the KL25Z MCU provides the FlexGUI firmware in charge of converting the USB communication into MCU instructions to control digital I/Os as well as I^2C communication to the PMIC.

If the FRDM-KL25Z is not loaded with the correct firmware to support a future software upgrade, the firmware can be updated in few simple steps.

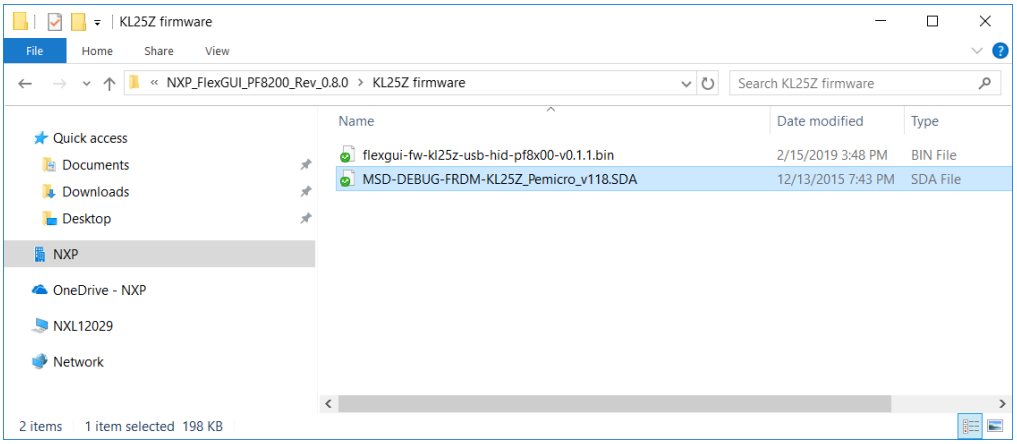
Note: *The following firmware updates are optional and can be skipped if the firmware is up-to-date.*

5.4.1 Flashing the FRDM-KL25Z firmware loader

1. Press the push button on the Freedom board and connect the USB cable into the SDA port on the Freedom board. A new BOOTLOADER device should appear on the left pane of the file explorer.



2. Drag and drop the file *MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA* into the BOOTLOADER drive. File should be located in the *KL25Z firmware* folder.

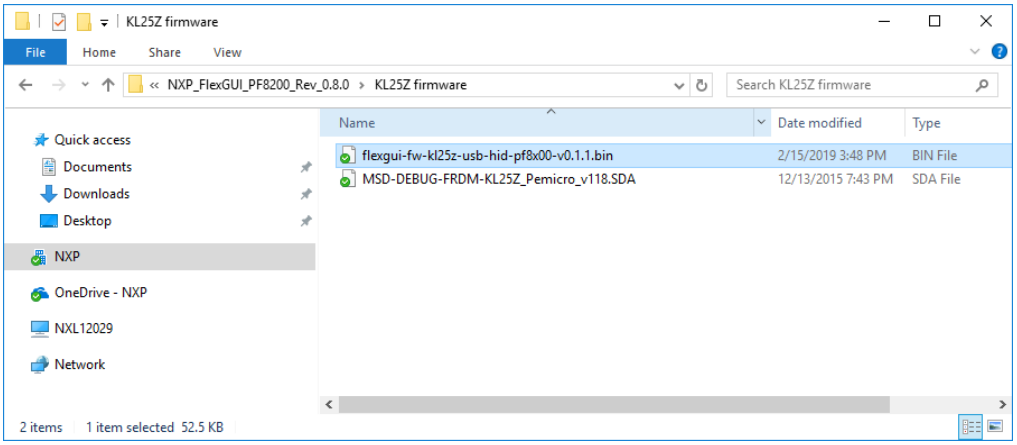


3. Disconnect and reconnect the USB cable into the SDA port (this time without pressing the push button). A new device called *FRDM_KL25Z* is installed on the PC.

5.4.2 Flashing the FlexGUI firmware

If a new software or silicon release requires a firmware update on the FRDM-KL25Z freedom board, use the following procedure to upgrade or downgrade the firmware of the freedom board as needed. Note that this procedure is needed only to update the firmware and may be skipped if no change is needed.

1. Connect the USB cable in the SDA port (without holding the push button).
2. Locate the ".bin" FlexGUI driver to be installed, for example *flexgui-fw-kl25z-usb-hid-pf8x00-v0.1.1.bin*, drag and drop the file into the FRDM_KL25Z driver.



3. Freedom board firmware is successfully loaded.

6 Configuring the hardware for startup

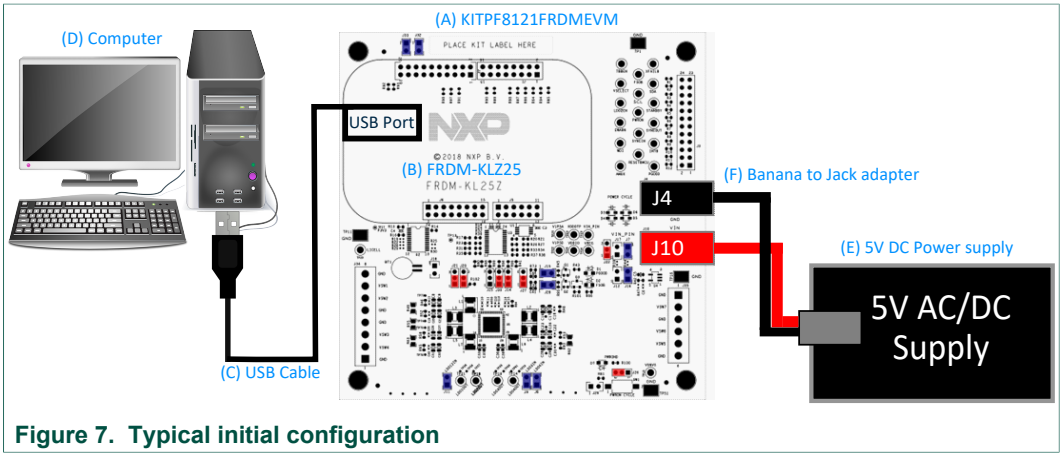


Figure 7. Typical initial configuration

1. With the USB cable connected to the PC and the USB port in the freedom board, apply VIN to the evaluation board.
   - Provide external VIN between 2.5 to 5.5 V on J10 (VIN) and J4 (GND) or
   - Short jumper J17 to provide 3V3 Vin from Freedom board (use this mode of operation for functional demonstration only, no regulation loading allowed in this mode).

   Note: Do not apply power to J10 while J17 is shorted. This could damage the onboard regulator on the FRDM-KL25Z Freedom board.
2. Press **Reset** on the Freedom board, to ensure board is properly recognized.
3. Browse to the *NXP_FlexGUI/bin/* folder and double-click on the **flexgui-app-8xxx.jar** executable to start the application.
4. The FlexGUI launcher is displayed with a list of possible configurations to load the FlexGUI. Select the appropriate option for device and silicon revision to be used. If the device revision populated on the KITPF8121FRDMEVM is not available in the list, please contact your NXP representative to obtain the latest software update suitable for your device.

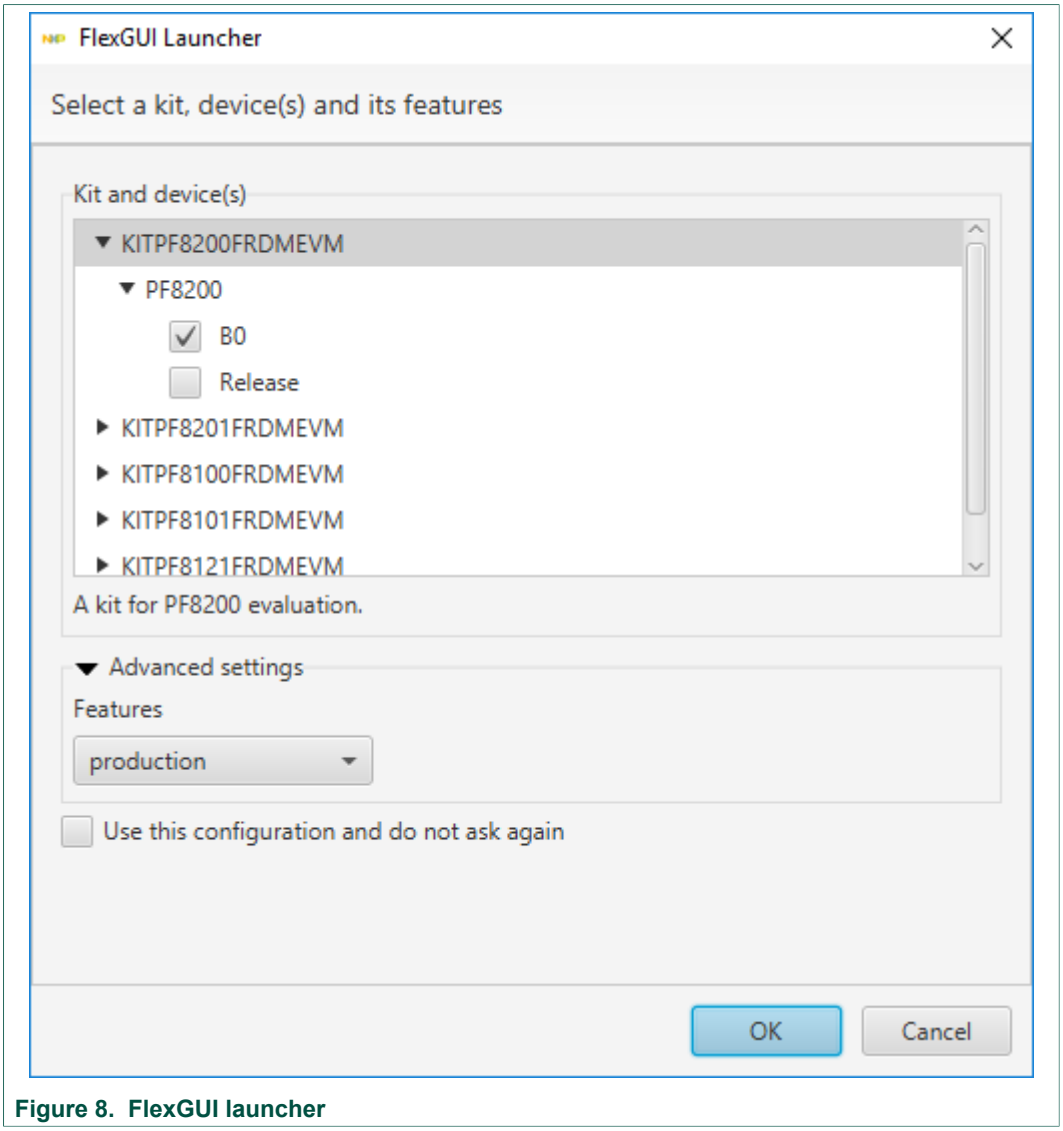


Figure 8. FlexGUI launcher

Silicon revision [1]	Description
B0	Use this configuration if you have received B0 silicon samples for preliminary device evaluation.
Release	Use this configuration if you have received C1 silicon samples or production parts.

[1] During new silicon transition, the file versions should be selected according to the silicon being used.

When the FlexGUI is done loading, the USB-HID connection will automatically search for the KITPF8121FRDMEVM, if a valid board is connected, the corresponding *Vendor ID* and *Product ID* should appear, then click **Start** to create a connection.

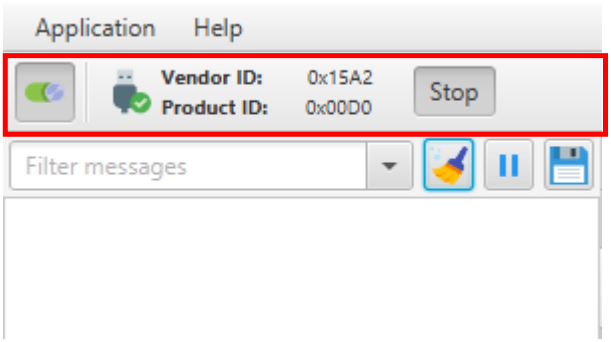


Figure 9. FlexGUI connection

Once the device is connected, the system is ready for Hardwire or TBB operation as desired.

6.1 Operating in Hardwire mode

To operate the board with the default hardwire configuration:

- Open J29 and J26 to allow the MCU to control the PWRON pin
- Short J20 in position 2-3 (VDDOTP = V1P5D)
- Open J21 to allow the MCU to control the TBBEN pin

In Hardwire mode, the device is working with the predefined configuration and supplies will turn on when the PWRON pin is set to high. To generate a power on event, the FlexGUI can be set to *Normal mode* in the mode selection box.

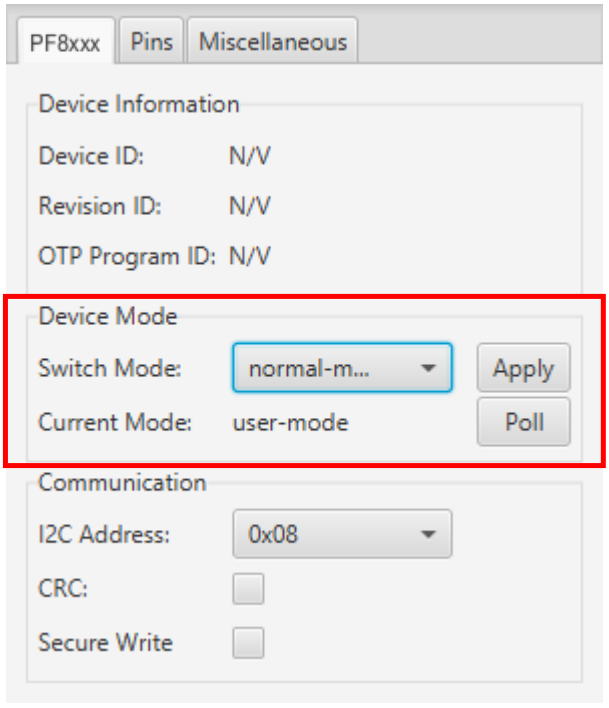


Figure 10. Normal mode operation

Click **Apply** to change the operating mode and start using the PMIC with the default configuration.

See Section 7 "Controlling the PF8121 using FlexGUI" for detail description on how to control the PMIC with the FlexGUI.

6.2 Operating in TBB mode

To operate the board in TBB mode:

- Open J29
- Short J20 in position 1-2 (OTP/TBB operation)
- Open J21 to allow the MCU to control the TBBEN pin

There are two ways to operate the device in TBB mode:

1. Manual configuration of the OTP mirror registers using the TBB mode control.
2. Load the OTP mirror registers with a custom TBB script using the *PF8121 Custom OTP Request Form* provided in the *SCRIPT & FORMS* folder.

6.2.1 Manual TBB configuration

During manual TBB configuration, use the TBB mode selection to enable access to the OTP mirror registers in the PF8121 device.

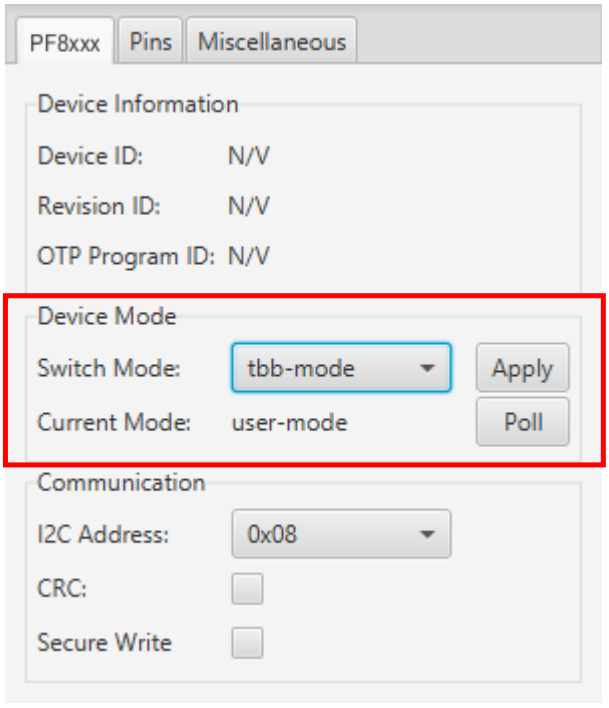


Figure 11. TBB mode operation

Click **Apply** to set the device in TBB mode and manually select the TBB configuration in the mirror registers.

When the FlexGUI is operating in TBB mode, the graphical interface uses command controls to communicate with the OTP mirror registers directly, enabling the user to manually set the default configuration one feature at a time.

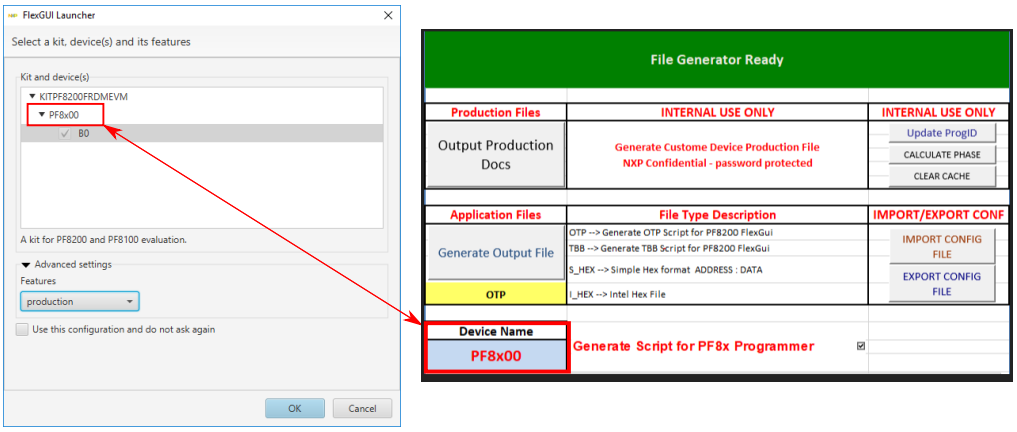
After configuring the features to be used during the device evaluation, change the operating mode to normal mode to generate a power on event and allow command controls to modify the functional I^2C registers again.

Detailed description on how to control the PMIC using the FlexGUI is described in Section 7 "Controlling the PF8121 using FlexGUI".

6.2.2 Generating a TBB script

To load the OTP mirror registers from a TBB script, choose the device configuration and generate the TBB script using the *PF8121 Custom OTP Request Form* provided in the *SCRIPT & FORMS* folder.

1. Use the *PF8121 Custom OTP Request Form* to select the default configuration to be used during the KITPF8121FRDMEVM evaluation. Note that the OTP request form is prepared to generate a TBB script for PF8121, however, make sure you pick the correct device number matching the device soldered on the customer evaluation board.
2. Generate a TBB script using the file generation section on the OTP request form (make sure to fill all required fields marked with a * to enable file generation). When generating a TBB script, it is important to match the device name with the device name in the FlexGUI to ensure proper generation of the script commands.



Silicon revision [1]	OTP request form version
B0	OTP Customer Request Form Rev 2.2 +
C0	OTP Customer Request Form Rev 3.0 +

[1] During new silicon transition, the file versions should be selected according to the silicon revision.

3. Save the generated TBB file in a known location.
4. On the Script Editor, use the command section to load the TBB script created, and then click **Run** to start programming the PMIC.

The device is automatically enabled with the selected TBB configuration after the programming is done.

7 Controlling the PF8121 using FlexGUI

7.1 Application environment

The GUI uses standard application layout divided into several working areas (see Figure 12).

1. Menu and connection toolbar
2. Command log area
3. Global system controls
4. Status bar
5. Device control area

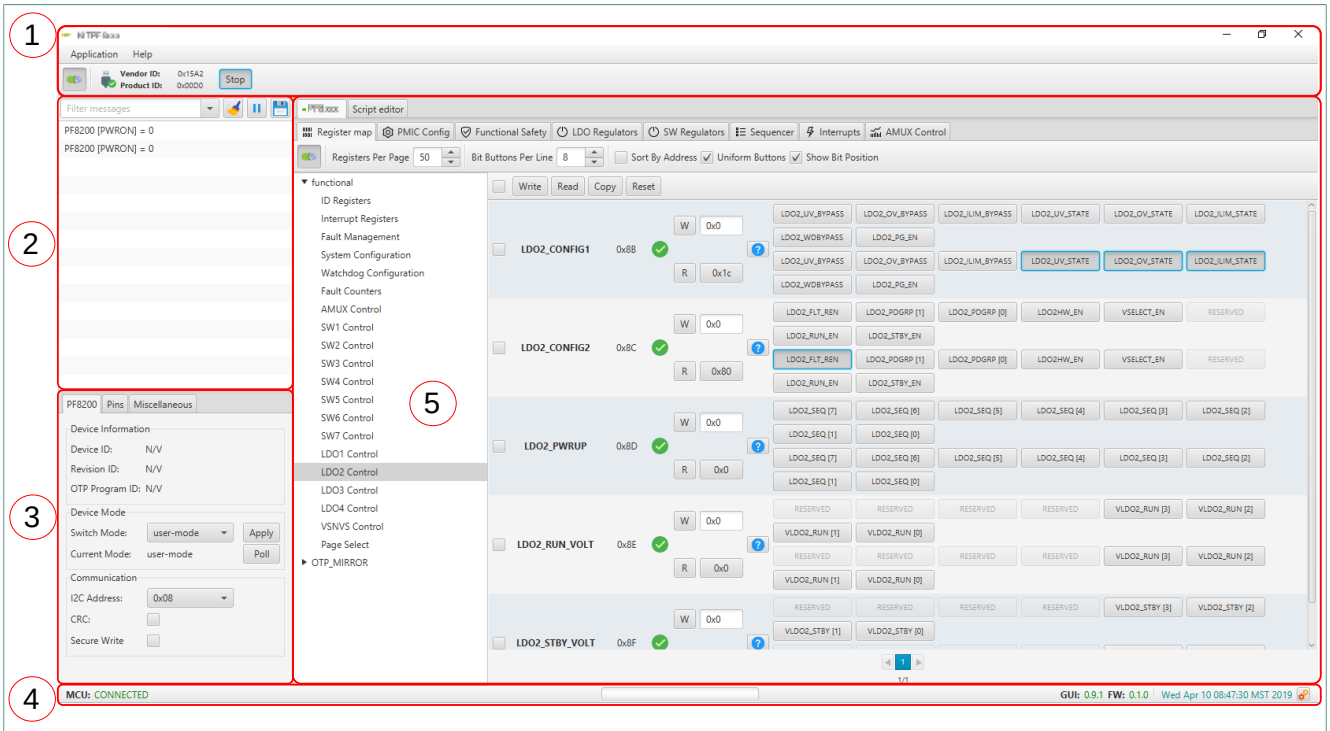


Figure 12. Application environment

7.1.1 Menu and connection toolbar

The menu and application toolbar offer access to various system dialogs as well as communication actions, see Figure 13. It is further divided into following subareas.

Applications menu	• Enables default configuration support • Quits application
Help menu	Provides information regarding the FlexGUI version and support
Hide panel	Hides or shows the global control panel
Communication	Provides board USB ID • Vendor ID: identify vendor ID when a supported board is connected • Product ID: identify product ID when a supported board is connected • Start/Stop: establish connection with the board connected

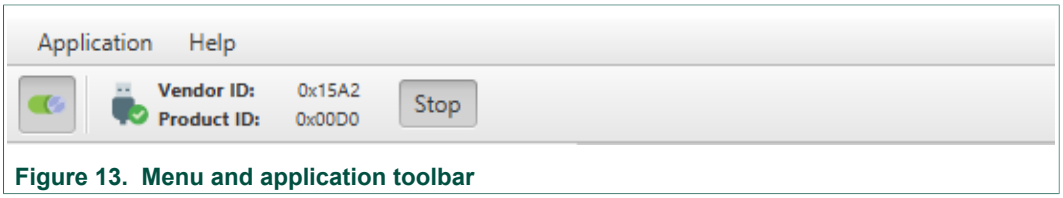


Figure 13. Menu and application toolbar

7.1.2 Command log area

The command log area informs the user about application events. Verbosity level is given by application configuration. User can interact with the area using toolbar on the top, which has following functions, see Figure 14. It is further divided into following subareas.

Filter selection	Enables various filtering schemes to display specific commands as desired
Clear log	Clears all messages from the log area
Pause log	Stops recording any new commands until the log is resumed again
Save log	Saves the content of the log area into a text file

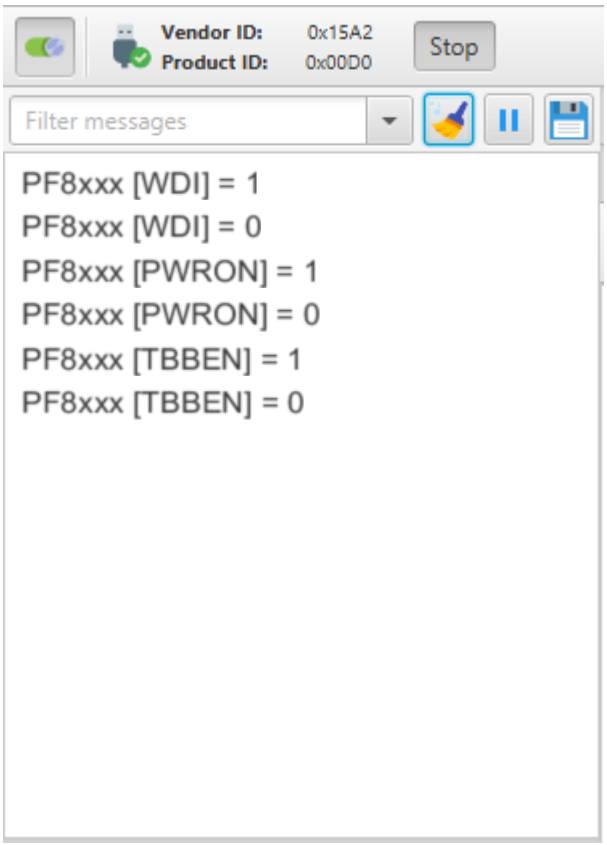


Figure 14. Command log area

7.1.3 Global system controls

The global system control provide access to system configuration controls not related to the PMIC operation, as well as the I/O control signals from the MCU to the PMIC. It is divided into two tabs as shown in Figure 15.

PF8121 system control tab	
Device information	Provides device information of the PMIC connected

Device mode	Selects the mode of operation of the evaluation board to interact and fully showcase all features provided by the PMIC. The system may be operated in four predefined modes: • User mode: no system I/O are modified by the FlexGUI allowing manual control of the PMIC using the Pin control tab. • Normal mode: the FlexGUI sets the TBBEN = low, STANDBY = low, WDI = low and PWRON = high, generating a power-on event. In this mode of operation, the user can control the STANBY pin and the corresponding polarity to set the PMIC in Run or Standby modes. In this mode, the FlexGUI control will configure the functional I^2C registers to modify the system configuration on-the-go. • TBB mode: the FlexGUI sets the TBBEN = high, STANDBY = low, WDI = low and PWRON = low, causing the PMIC to turn off and move to the QPU_OFF state in order to allow the OTP mirror registers to be accessed and modified. In this mode, the FlexGUI uses the PMIC controls to program the default OTP configuration to be used in the next power up event. During TBB mode, only the controls which have OTP bits become available while all other functional bits are disabled until the system is set into Run or Standby modes.
Communication	• I^2C address: selects the default address used to communicate with the PMIC. By default the I^2C address is set to 0x08, but communication must be changed if the PMIC uses another I^2C address as configured in the OTP mirror registers. • I^2C CRC enable: enables the MCU to add CRC calculation to each I^2C transaction. • Secure write enable: enables the MCU to perform automatic proofing to write Secure write registers.
Pin control tab	
LDO2EN	Allows the MCU to control the level of the LDO2EN pin in the PMIC. Use this control in conjunction with the LDO2HW_EN bit to allow the LDO2 output to enable or disable by toggling the pin high or low.
XINTB	Allows the MCU to control the level of the XINTB pin in the PMIC. Use this control to generate an external interrupt on the PMIC.
VSELECT	Allows the MCU to control the level of the VSELECT pin in the PMIC. Use this control in conjunction with the VSELECT_EN bit to allow the LDO2 output to toggle between 1.8 V or 3.3 V by toggling the pin high or low.
STANDBY	Allows the MCU to control the level of the STANDBY pin in the PMIC. Use this control in conjunction with the STANDBYINV bit to force the PMIC in and out of the Standby mode by toggling the pin high or low.
PWRON	Allows the MCU to control the level of the PWRON pin in the PMIC. When the OTP_PWRON_MODE bit is set to level sensitive, use this control to generate a power-on or power-off event by toggling the pin high or low. When the OTP_PWRON_MODE bit is set to Edge sensitive, use this control to generate a rising or falling edge to simulate a push button to generate the corresponding power-on or power-off events.
TBBEN	Allows the MCU to control the level of the TBBEN pin in the PMIC. Use this control to enable debugging conditions as well as grant access to the OTP mirror registers.

WDI	Allows the MCU to control the level of the WDI pin in the PMIC. Use this control in conjunction with the OTP_WDI_INV, to generate a watchdog reset event on a rising or falling edge of the WDI signal.
Input pins	Allows the MCU to read the level of the EWARN and INTB pins. MCU can be programmed to poll the read or perform a single read.
Miscellaneous controls	
Watchdog refresh	Enables the MCU to perform a watchdog refresh with the selected period
System diagnostics	System diagnostic buttons • Use the **ABIST Run** to start the ABIST on-demand test during the system-on states. Results of the ABIST test can be read in the Functional Safety tab. • Use the **INTB Test** to request a 100 µs pulse in the INTB pin. • Use the **SW Shutdown** to request a software shutdown event. The PMIC will restart if a power-up event is present after shutting down.

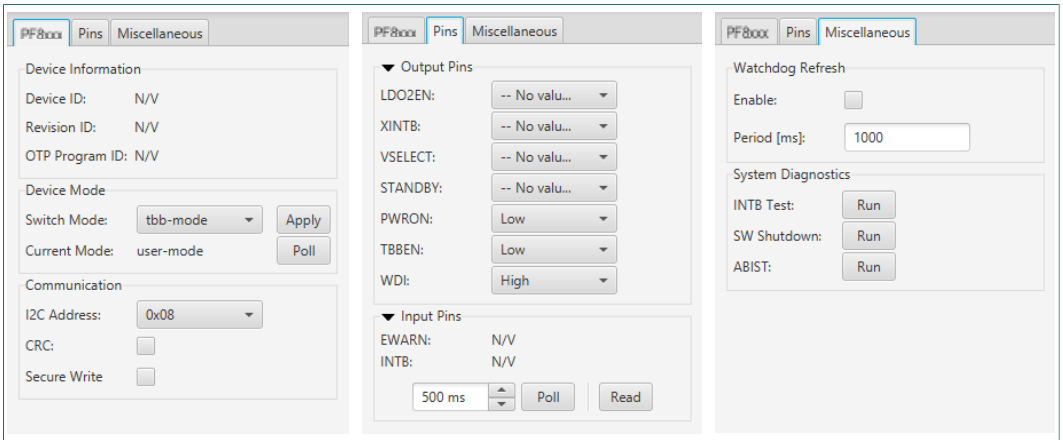


Figure 15. Global system controls

7.1.4 Status bar

Status bar provides a standard overview of application conditions.

Status area	MCU status • CONNECTED: GUI is connected to the MCU • DISCONNECTED: GUI does not have connection to the MCU
Version area	Informs the user about used module versions • GUI: informs the user about version of derivative GUI • Firmware: informs the user about version of used MCU firmware • Build: informs the user about the building date for the current release

7.1.5 Device control area

This area enables the user to interact with all loaded devices. Each device has its own dedicated tab with several subtabs to access all controls dedicated to the specific device loaded, see Figure 16. In addition to the device tab, the FlexGUI provides a Script editor tab to allow sequential configuration and control of one or various devices with a command based script processor.

Script editor	Enables user to create sequences of commands to control the device/s, see Section 7.3 "Working with the Script editor" for details on this generic component
Device control tab	Tabs/components enable user to work with device on high level abstraction of its features/functionality

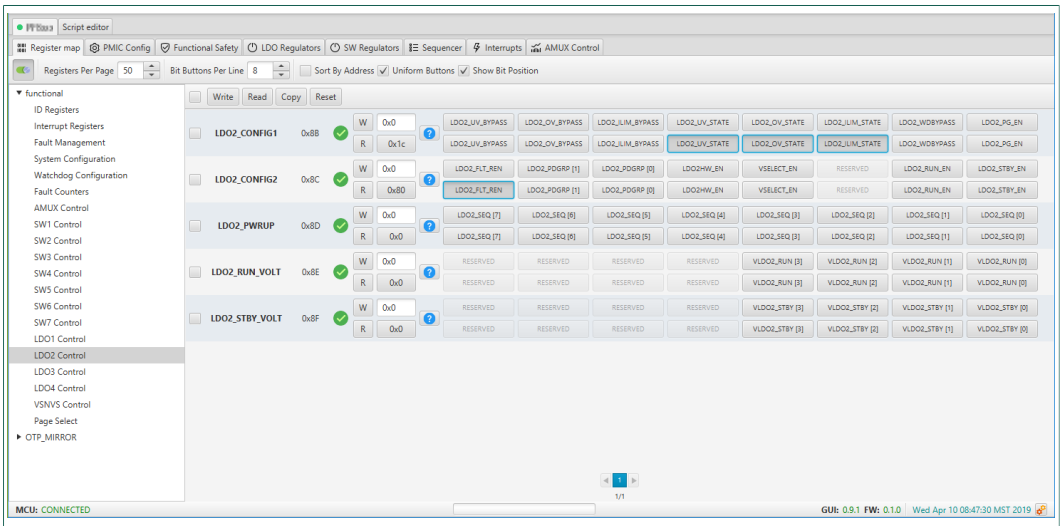


Figure 16. Device control area

7.2 Understanding the PF8121 workspace

The PMIC controls are organized in seven tabs specific to the PF8121 device and one tab providing bit by bit access to the register map of the device. The eight control tabs are listed below and are explained in the following sections.

- Register map
- PMIC configuration
- Fault monitoring
- LDO regulators
- Switching regulators
- Sequencer
- System interrupts
- AMUX control

7.2.1 Register map

The PF8121 registers are organized in register pages or sectors. The FlexGUI organizes the registers in various types and multiple register groups. For detailed view of the PF8121 register map, see PF8121 data sheet.

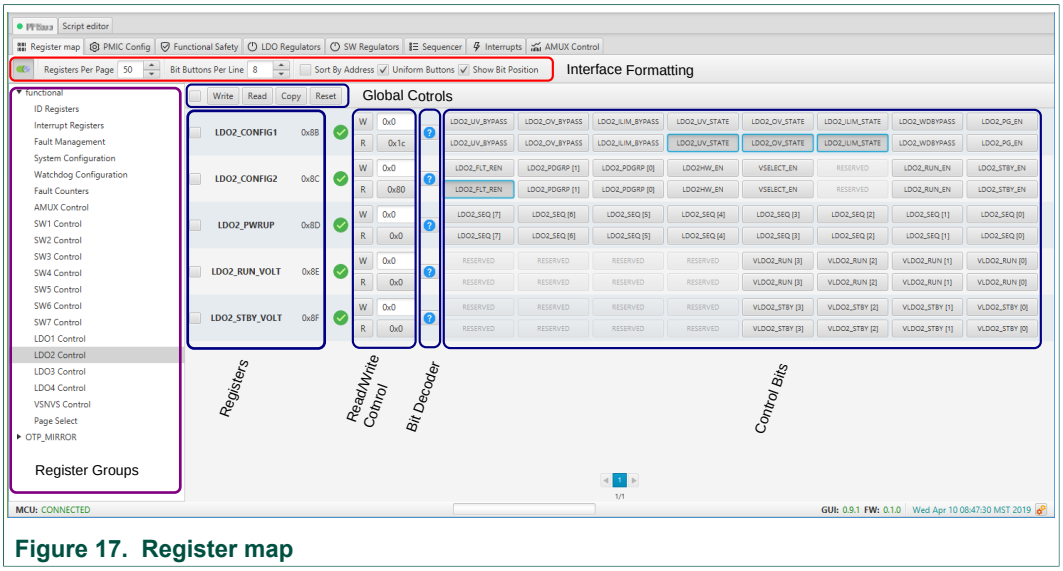


Figure 17. Register map

Each register group contains all registers related to a specific channel or feature. Read/write registers provide independent lines to read and write the values on the selected registers.

Individual registers can be read by clicking the **R** button and can be written by using the **W** button on the corresponding register.

Multiple registers can be read, written, copied or reset using the global register controls.

Use the **Copy** button to copy the latest read value onto the write line.

Use the **Reset** button to undo the changes on the write line and reset to the previous value. When using the global register controls, the selected command will be performed on all registers with the checkbox selected. Only functional and OTP mirror registers are intended for user evaluation.

- Functional registers: provide access to the current configuration of the PMIC. Configuration can be changed and changes will be applied once the command is sent.
- OTP mirror registers: provide access to the default configuration to be used at PWRON event. Note that access to these registers are only meant for debug or development purposes, therefore these registers can only be read or modified when TBBEN is high. The TBBEN can be set high externally via the J21 header or by the MCU via the script editor.
- Use the bit decoder buttons to set the register bit based on its actual functional value.
- The FlexGUI provides useful interface formatting controls as defined below:
  - Hide/show panel: use this button to hide or show the Register group panel, allowing more space to display all register bits in a single line.
  - Register per page: use this selector to chose how many registers are shown at the same time. Register count apply only to registers inside the selected register group. When the GUI is set to display limited number of registers, use the page surfing option at the bottom of the register bit area to find the selected register.
  - Bit buttons per line: use this option to chose how many bits are shown in a single line. This option is useful to force a certain register partition on low resolutions screens.
  - Sort by address: use this option to force the register to display the address in ascending order.
  - Uniform buttons: when this option is selected, the register bits are displayed with a uniform size. Longer names may get truncated to the button size. If this option

is not selected, the buttons will change the size to fit the name of the register bit independently.

– Show bit position: use this option to show the bit position for a specific functional bit group.

7.2.2 PMIC configuration

The PMIC configuration tab provides access to the global configuration of the PMIC.

Figure 18. PMIC configuration

The functions that can be programmed in the PMIC configuration are listed below:

- PWRON: configuration and mode of operation of the PWRON pin
- PGOOD: configuration and control of the PGOOD pin
- STANDBY: configuration of the STANDBY pin
- WDI control: configuration of WDI pin and PMIC reaction when WDI pin toggles
- Coin cell control: configuration of coin cell voltage level and the coin cell charger
- Low power mode: configures the selection of the LP_OFF or QPU_OFF state when device is Off
- Clock management: configuration of the clock frequency, spread spectrum and frequency synchronization pins
- Fault control: configuration of the fault protection mechanisms

- VIN overvoltage lockout: configuration of the OVLO protection circuit
- Thermal monitor: configuration of the thermal monitor
- Watchdog: configuration and control of the internal Watchdog counter
- MCU watchdog management: provides parameters to allow the MCU to clear the internal PMIC watchdog
- I^2C communication: sets the I^2C address and enables the CRC check during I^2C communication (available in OTP only)
- OTP miscellaneous: sets default OTP configuration for various PMIC features.

See PF8121 data sheet for detail description on the PMIC configuration.

7.2.3 Fault monitoring

The fault monitoring tab provide access to the fault monitoring circuits available on the PF8121 devices.

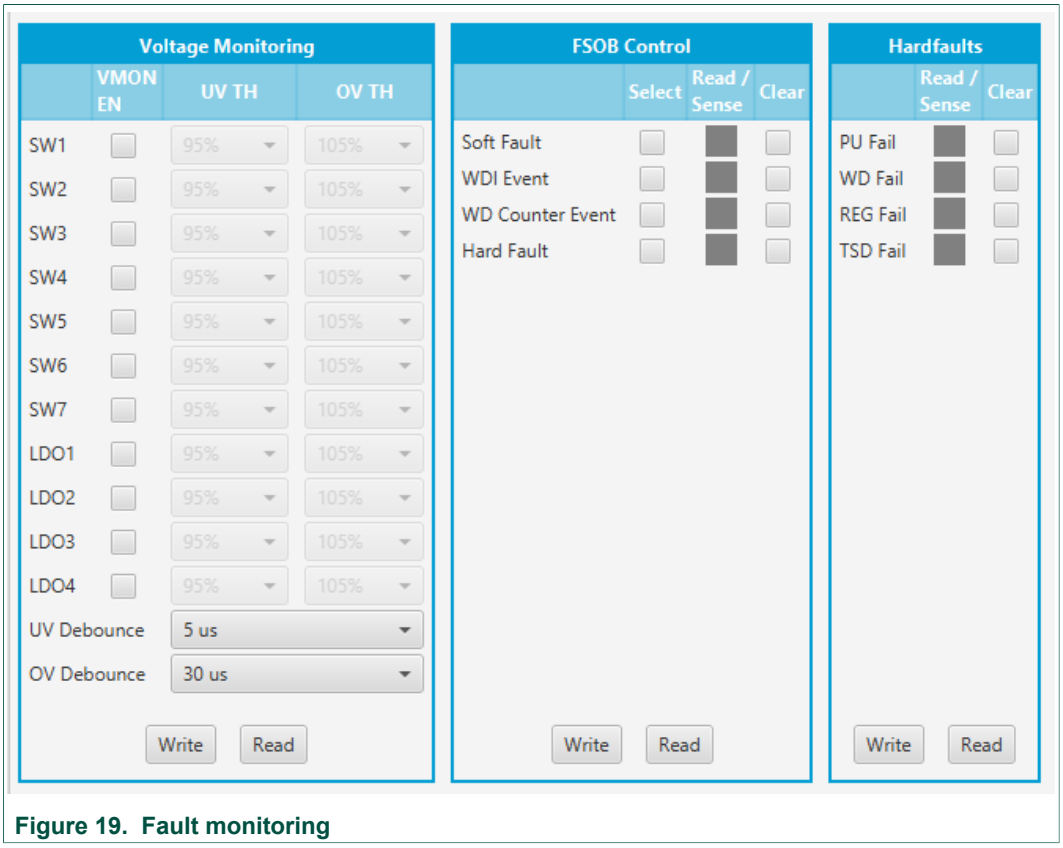


Figure 19. Fault monitoring

Voltage monitoring: the user can perform the following actions using this control:

- Enable or disable the voltage monitor
- Select the OV and UV threshold (in OTP only)
- Select the OV and UV detection debounce
- Monitor/clear the ABIST flags in case of failure

FSOB control: use this control to select the FSOB mode and select/monitor the FSOB reaction on any of the following faults:

- Soft fault
- WDI event

- WD counter event
- Hard fault

Hard faults: use this control to monitor the source for the hard fault causing a power down event.

- Power up fail
- Watchdog fail
- Regulator fail
- Thermal shutdown

7.2.4 LDO regulators

The LDO tab is used to configure and control the LDO regulators.

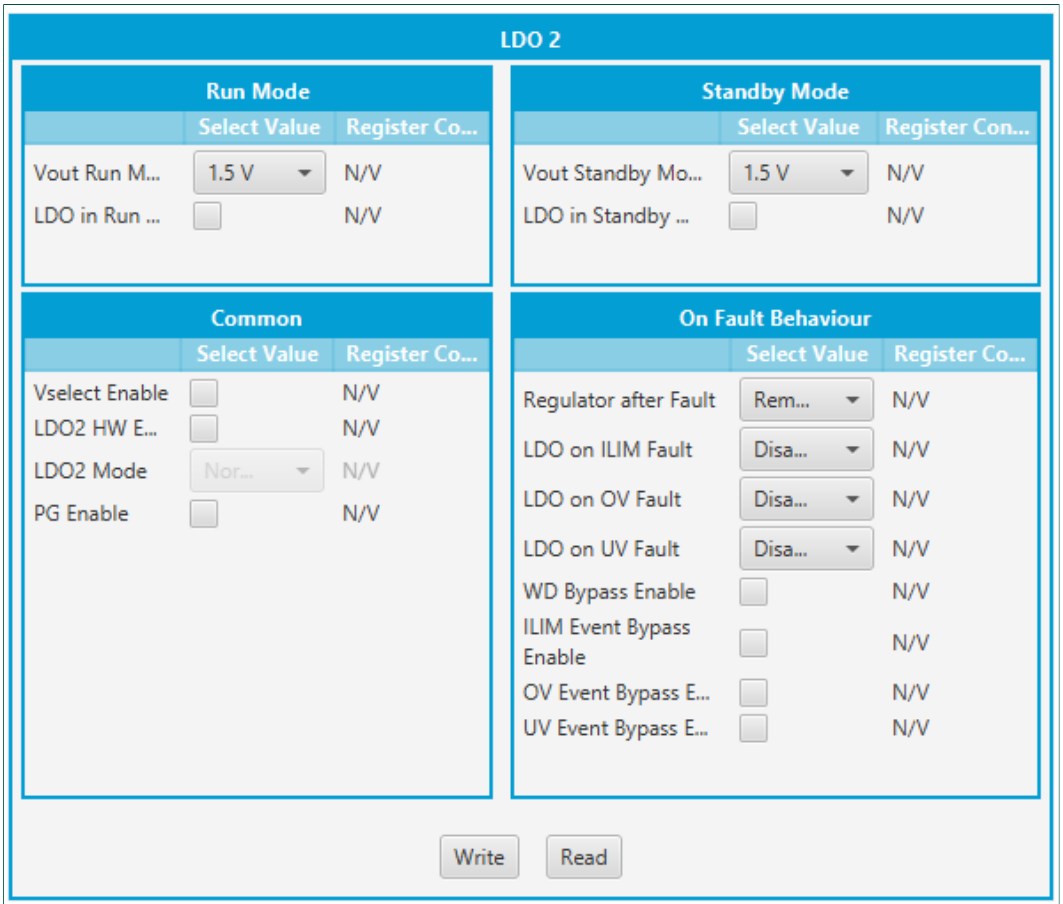


Figure 20. LDO control

Each LDO can change the following features:

- The output voltage in Run and Standby state
- LDO status in Run and Standby state
- LDO operating mode (OTP only)
- Set the reaction of the LDO output on an OV, UV or ILIM event
- Bypass OV, UV or ILIM events
- Bypass reaction during a soft watchdog event
- Enable the LDO to assert he PGOOD pin on an OV or UV fault

- Enable or disable the voltage monitor

In addition, the LDO2 can set the output to be enabled and modified via the LDO2EN and the VSELECT pin.

VSNS can be disabled or changed to a different voltage during the system-on states.

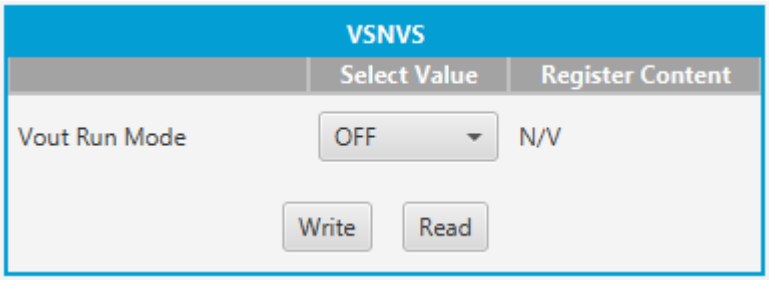


Figure 21. VSNVS control

7.2.5 Switching regulators

The SW regulator tab provides access to all features for each one of the switching regulators.

SW1 to SW6 are valley current mode controlled buck regulators configurable as single, dual, triple and quad phase regulators as described in the PF8121 data sheet.

All regulators capable of multiphase operation share the same feature set as shown in the following figure.

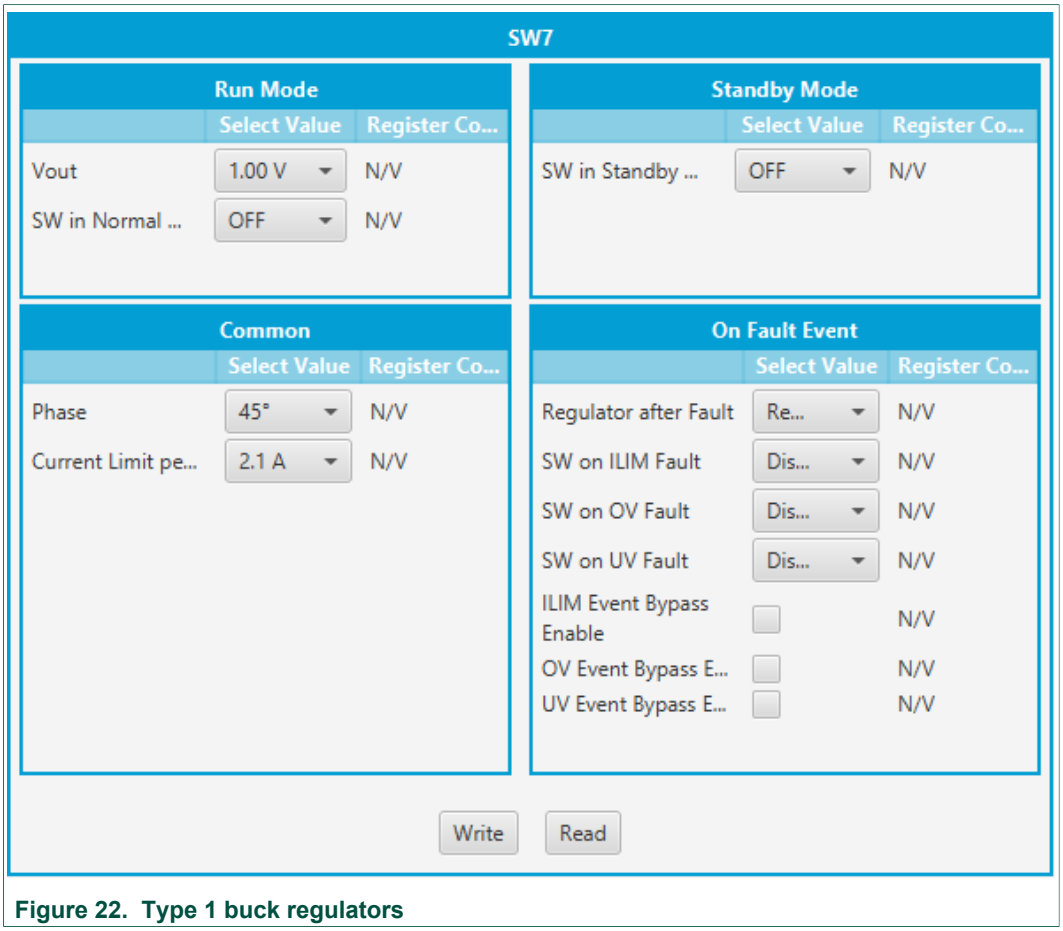


Figure 22. Type 1 buck regulators

SW7 is a peak current mode controlled buck regulator operating in single phase only which provides higher output voltage settings typically used for 3.3 V I/O supply.

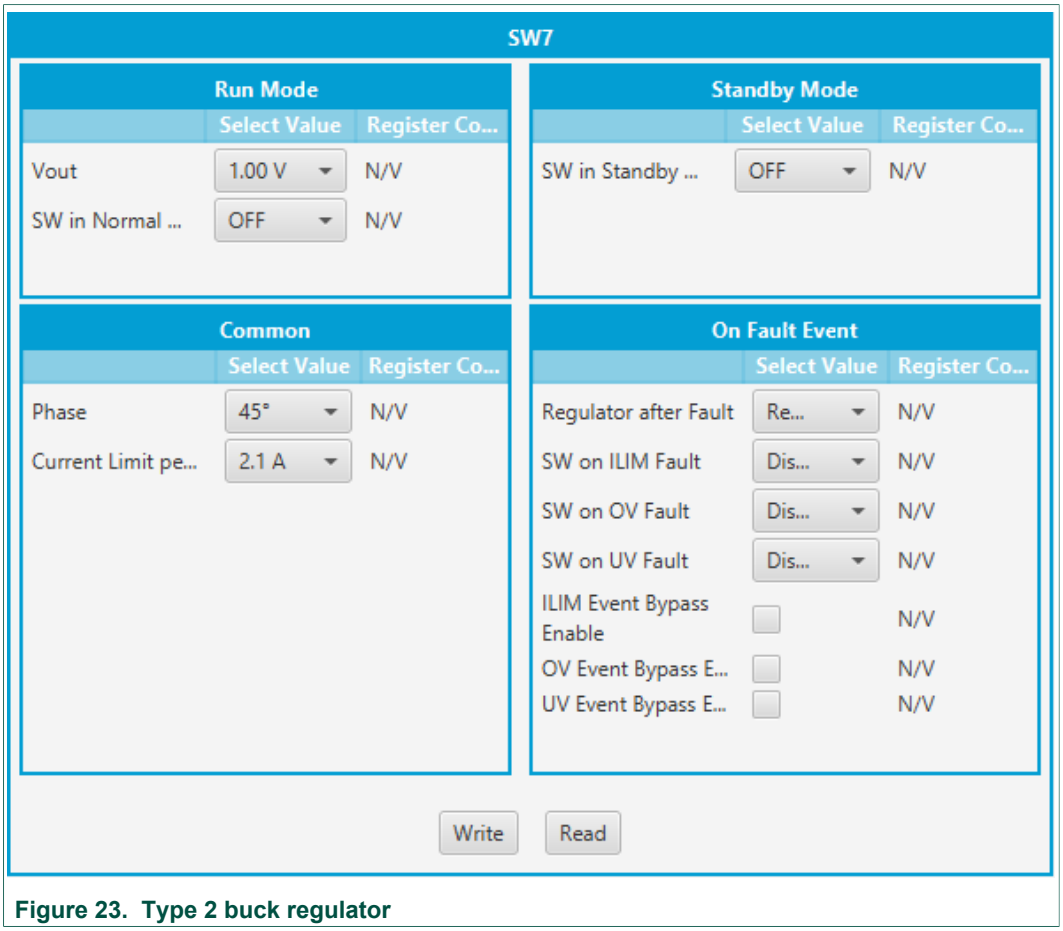


Figure 23. Type 2 buck regulator

SW regulators can modify the following properties:

- Mode of operation in Run state
- Mode of operation in Standby state
- Output voltage in Run state
- Output voltage in Standby state
- The phase of its switching frequency
- Current limit
- DVS ramp rate
- SW6 can additionally be set in VTT mode to follow the voltage on SW5

7.2.6 Sequencer tab

The sequencer tab is used to write the power-up sequence configuration of all regulators and I/Os on the PF8121 PMIC. The sequence graph shows a graphical representation of the selected sequence.

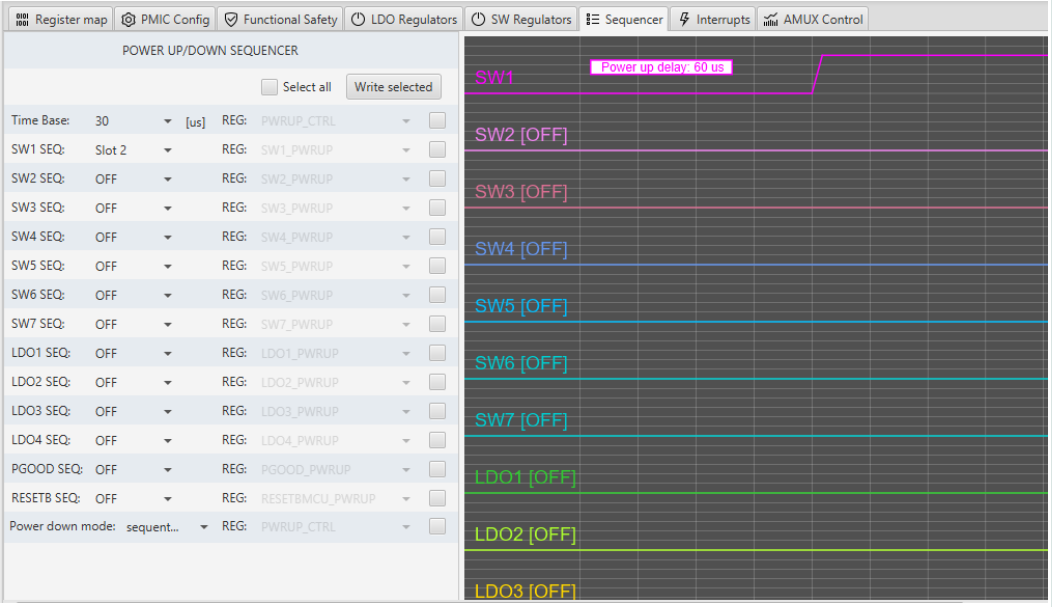


Figure 24. Power up/down sequencer

In Normal mode, writing to the SEQ bits modifies the functional registers to allow a custom power down sequencing when the device is configured to power down in Sequential mode. In TBB mode, writing to the SEQ bits modifies the OTP mirror register to allows a custom power up sequence when OTP/TBB operation is enabled (VDDOTP = GND).

Selecting the power down mode as *Group*, sets the PMIC to power down by groups, allowing the user to temporarily assign each regulator to one of the four power down groups, as well as configuring the group delays used during the power down event. In TBB mode, the FlexGUI grants access to the OTP mirror registers in order to configure the default value of the Group power down registers, however the user can change the power down mode later during the Normal mode if desired.

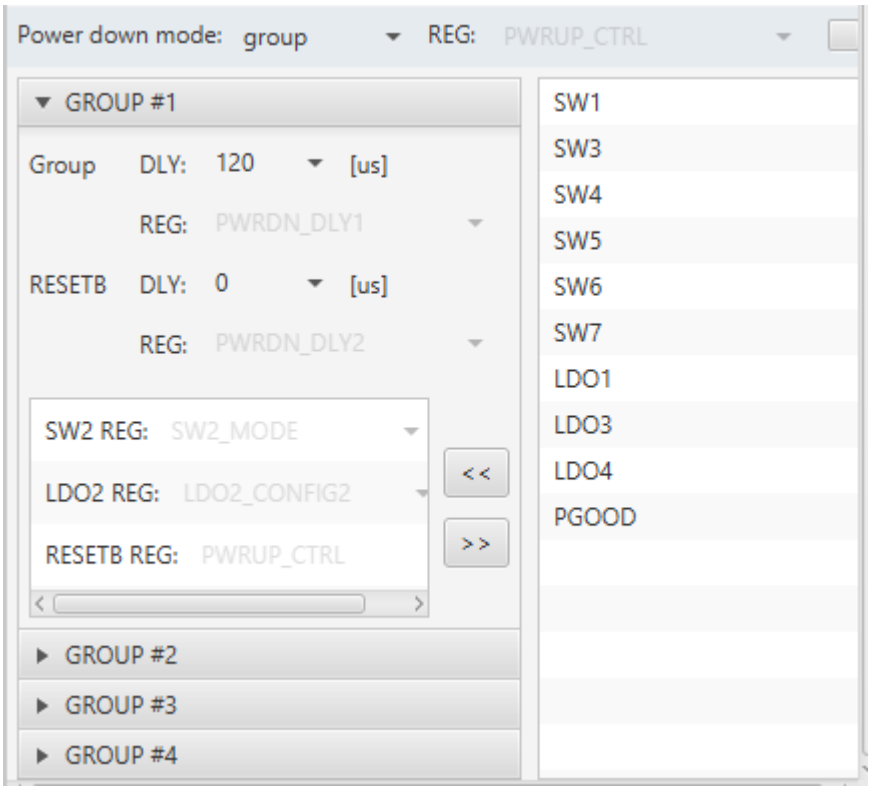


Figure 25. Group power down controls

7.2.7 Interrupt tab

The interrupt tab provides access to all the interrupts, mask and status registers in the PF8121.

One system interrupt register is provided to work as first level detection of a physical interrupt. The system interrupt flags will be asserted only when one or more unmasked interrupts are detected in any of the second level interrupts registers and driving the INTB pin low. Interrupt events that are masked will not be notified in the system interrupt register.

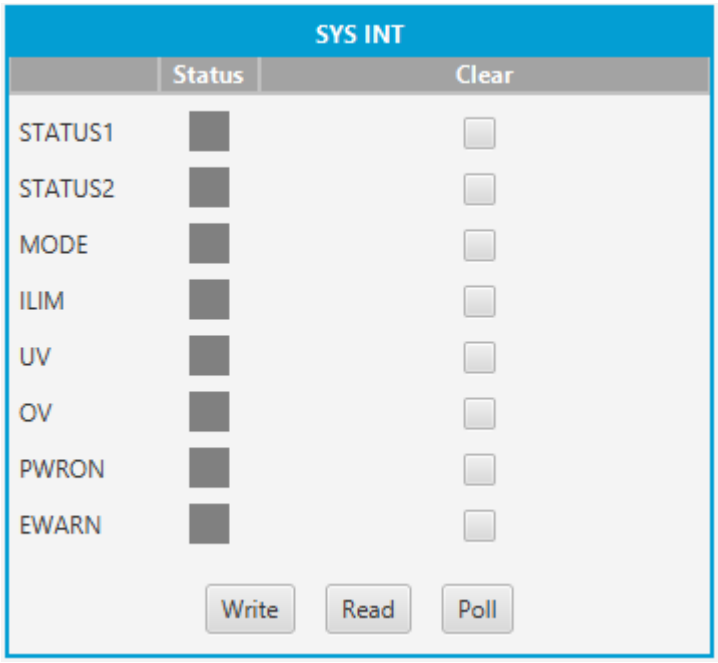


Figure 26. System interrupts

At a second level, the specific interrupt flags are organized in ten registers allowing the system to identify the source of an interrupt in a maximum of three I²C transactions.

Each interrupt event provides 3 bits to allow a flexible interrupt management scheme:

- Status bits: a red box indicates that an event on the corresponding function has occurred. Setting the clear box and writing to the registers will write a 1 to the corresponding latch, causing the interrupt latch to be cleared.
- Mask bits: checking the mask bit prevents the INTB pin to be asserted when the respective event is present.
- Sense bits: when the sense bit is green, the corresponding sense signal is low and when it is red, the corresponding sense signal is high.

Four global interrupt registers are provided to notify global system events such as thermal interrupts, I/O events, global fault events, switching regulator mode transitions, etc.

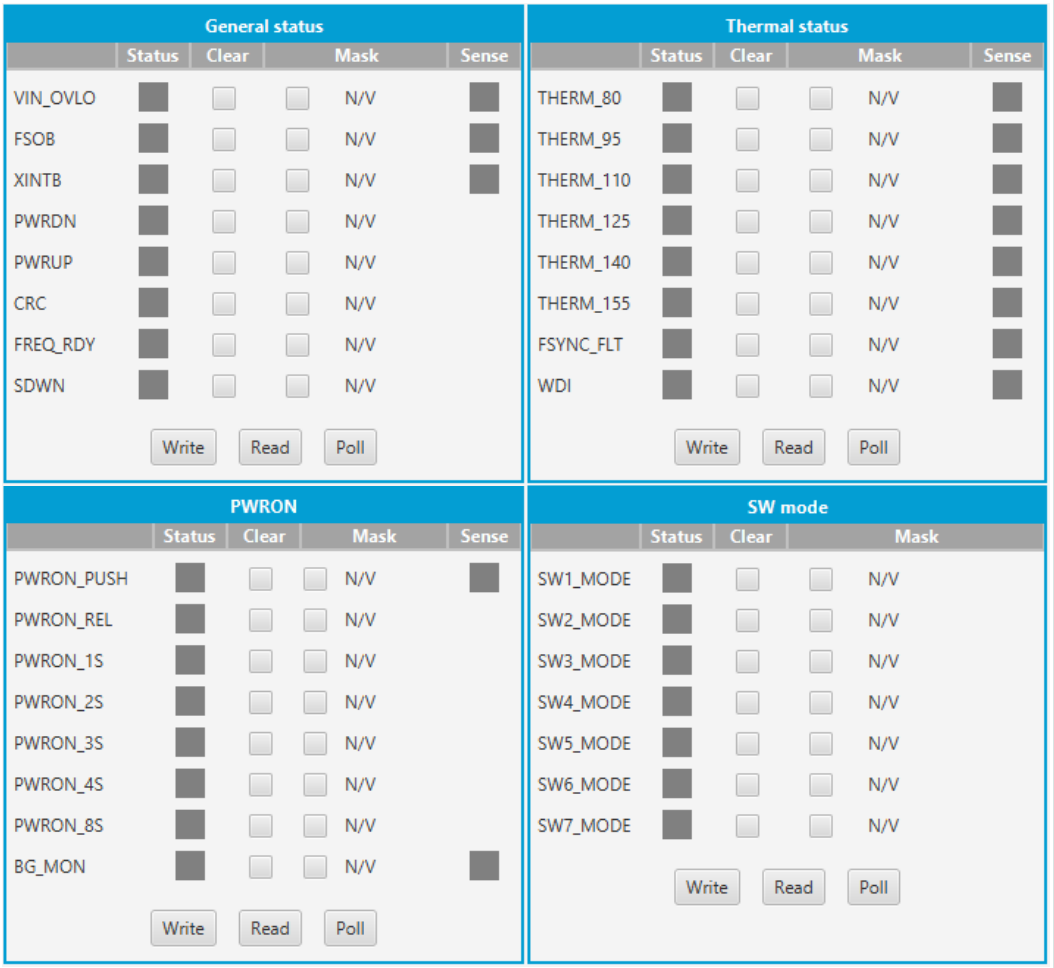


Figure 27. Global interrupts

Three interrupt registers are provided to notify specific OV, UV, and ILIM faults in the switching regulators.

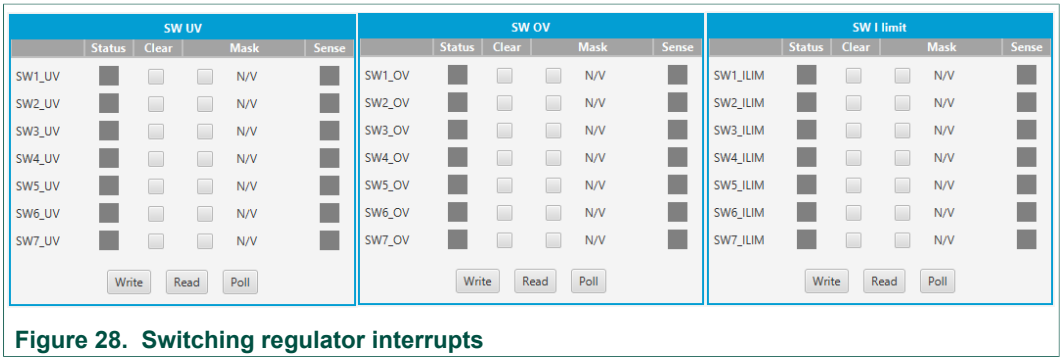


Figure 28. Switching regulator interrupts

Three interrupt registers are provided to notify specific OV, UV, and ILIM faults in the LDO regulators.

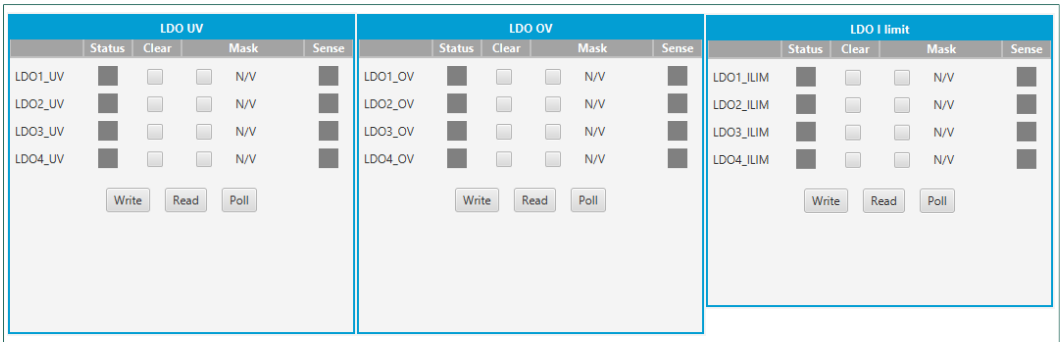


Figure 29. LDO regulator interrupts

See PF8121 data sheet for more details on the specific conditions that may cause any of the interrupt events.

7.2.8 AMUX control

The AMUX control tab provides the ability to automate the AMUX channel selection to display the reading of the selected channels through a polling cycle.

There are two measurement areas, one for voltage measurement and another for temperature measurement. The FlexGUI automatically displays the calculated value to show the real value after applying conversion and scaling factors to eliminate the need for manual calculation using the raw voltage at the AMUX pin.

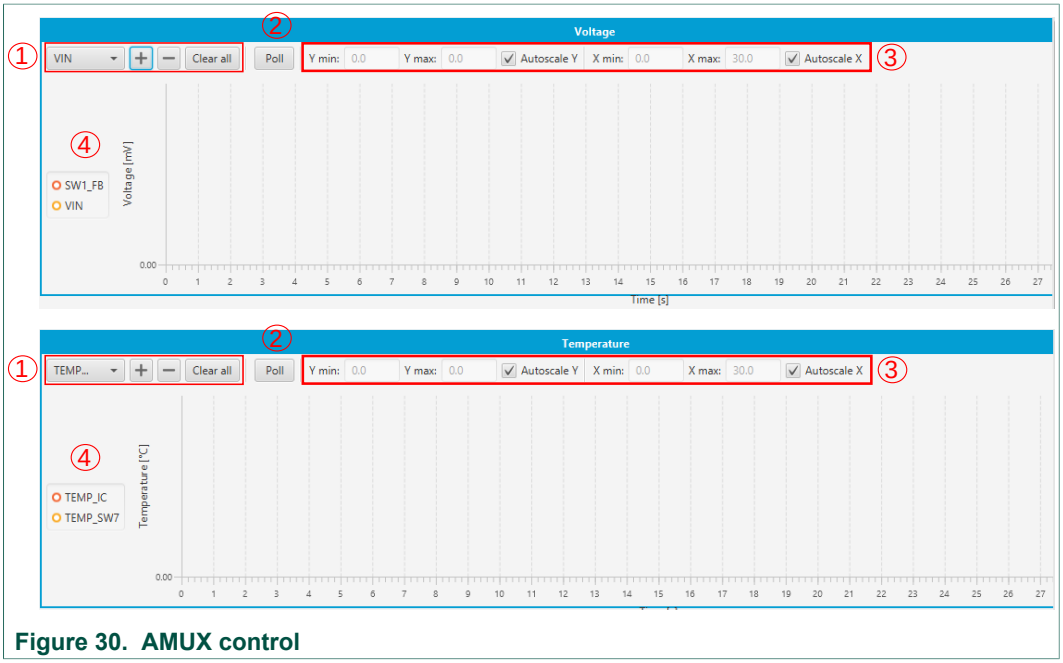


Figure 30. AMUX control

1. **AMUX channel selection:**
   - Use this drop-down list to select the channel to be added to the AMUX polling cycle.
   - Use the + and - buttons to add or remove signal from the polling list.
   - Use the Clear All button to remove all signals from the polling list.
2. **Start polling:**
   - Use the Poll button to start the polling cycle to read the AMUX channels selected in the polling list.

3. **Display scaling:**
   - Use the scaling controls to change the display scale for the AMUX measurements.
4. **Polling list:**
   - The selected channels added to this list will be added to the polling cycle in order to provide real time data for all the channels in the list.

7.3 Working with the Script editor

The script editor is a tool that enables sequential execution of commands, which can access registers, digital and analog pins of a device. The graphical interface facilitates creation and working with commands.

7.3.1 Script editor environment

The graphical interface resides in the Script editor tab, see Figure 31. It consists of three main parts: command generation, script area and script log.

The command generation pane assists the user in the creation of script commands. The script area contains a list of commands to be executed, one command per line. The user can write commands manually or use the command generation pane. Format of commands is described in Section 7.3.2 "Definition of commands". Lastly, the script log shows the results of the script processing. A line in this pane corresponds to the same line in the script control panel.

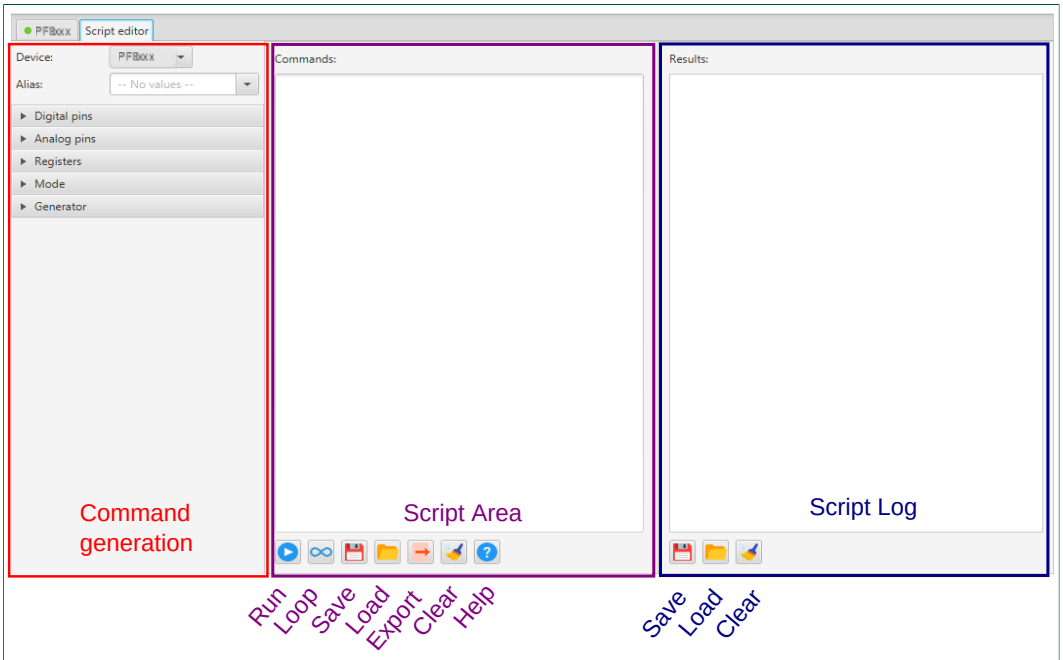


Figure 31. Script editor environment

Following steps describe how to create and execute a simple script:

1. The FlexGUI must be connected to the device.
2. In the command help pane, choose the device for which the script is to be generated. The FlexGUI loads the appropriate values to generate the script commands (i.e. register names, pin names).
3. Create commands to be executed. The user can write the command manually or utilize the command generation pane which offers valid options.

- To automatically generate a command, select the command attributes and the tool inserts a new line into the script control pane. The write register command requires the register value in hexadecimal value (0x prefix, e.g. 0x12).
- I/O control commands can be used to set pin high or low to generate specific events.

4. Execute commands using the Run button. To process the script in a loop, set Run in loop option in the script control pane and then run the script. In this case, the script is processed until the user clicks Stop.
5. The script log provides a summary of all the command executed in the script. Note that results are cleared when another processing begins.

The user can save or load scripts in .txt format. The execution result can also be saved or loaded from a file.

The Export button can be used to export all the SET commands in a simple hex format:

```
<register address>, <register value to be written>,
```

Use the script generation option to create the following commands:

- Read the status of a digital pin
- Set a digital pin high or low
- Select the analog channel to read at the AMUX
- Write a register
- Read a register
- Change the operating mode
- Generate a TBB or OTP script with the data configured in the device control tabs

When working with a pre-generated script in which the device name may not match the script command ID, use the **Device alias** list to allow the FlexGUI to read commands with a different command ID (see Figure 32).

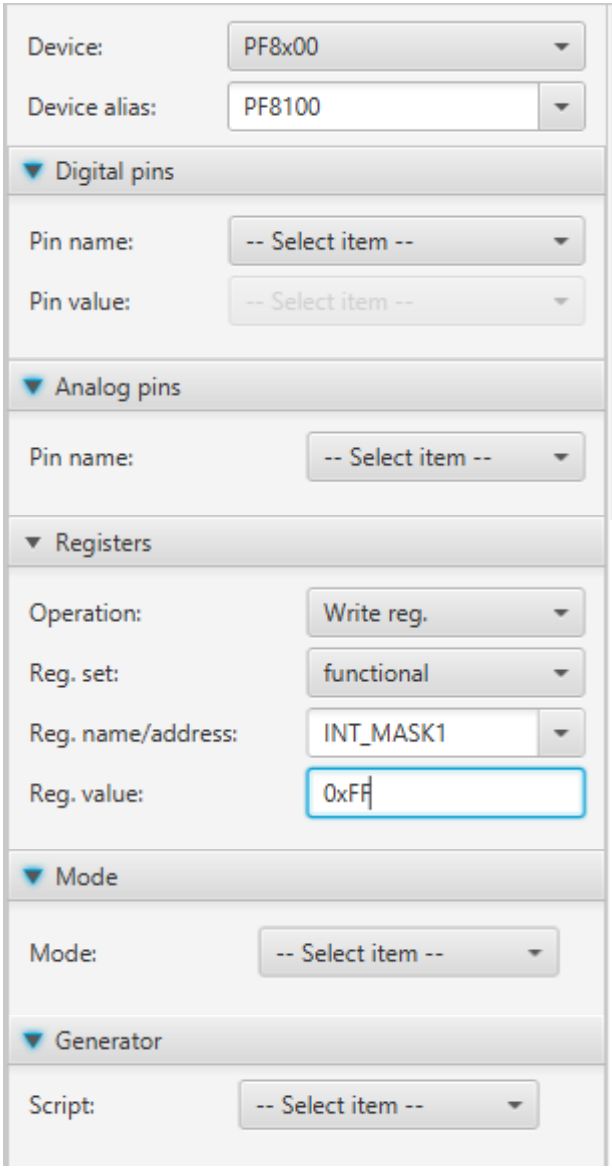


Figure 32. Script generation

7.3.2 Definition of commands

This section describes commands supported by the script editor and their format. All commands are listed in Table 8.

Table 8. Script editor commands

Command name	Description
SET_REG	Sets value of a selected register
READ_REG	Reads value of a selected register
SET_DPIN	Sets value of a selected digital pin
GET_DPIN	Gets value of a selected digital pin
GET_APIN	Gets value of a selected analog pin. Returned value is in mV.

Command name	Description
PAUSE	Shows a dialog with a user defined message. The script execution is paused until the user confirms the dialog.
SET_MODE	Sets the mode of operation

7.3.3 Format of commands

General format of script editor command is as follows:

```
<command name>:<list of parameters separated by a colon>
```

Table 9 shows parameters of script editor commands. All parameters are mandatory.

Table 9. Parameters of script editor commands

Command name	1. item	2. item	3. item	4. item
SET_REG	Device	Reg. set	Reg. name	Reg. value
GET_REG	Device	Reg. set	Reg. name	
SET_DPIN	Device	Pin name	Pin value	
GET_DPIN	Device	Pin name		
GET_APIN	Device	Pin name		
SET_MODE	Device	Mode of operation		
PAUSE	Message			

Device	Device name/ command ID
Reg. set	Register set name. Register set enables association of registers having similar function.
Reg. name	Register name as defined in a data sheet
Reg. address	Register address in the decimal or hexadecimal (with 0x prefix) format
Reg. value	Register value in the decimal or hexadecimal (with 0x prefix) format
Pin name	Name of a digital or analog pin as defined in a device data sheet
Pin value	Value of digital pin. Allowed strings are low and high.
Mode of operation	TBB mode, Normal mode, User mode
Message	A message to be displayed in a dialog. It cannot contain the colon character, which is used as a delimiter of parameters.

8 References

[1] **KITPF8121FRDMEVM** — detailed information on this board, including documentation, downloads, and software and tools
http://www.nxp.com/KITPF8121FRDMEVM

[2] **PF8121** — product information on multi-channel power management integrated circuit
http://www.nxp.com/PF8121

9 Revision history

Revision history

Rev	Date	Description
v.1	20190422	Initial version

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