

UM10664

PCA8885 and PCF8885 evaluation board OM11056

Rev. 1 — 29 January 2013

User manual

Document information

Info	Content
Keywords	Capacitive touch switch, touch sensor, proximity switch, PCF8885, PCA8885, OM11056, evaluation board, I ² C interface
Abstract	The OM11056 is a PCA8885 and PCF8885 evaluation board which can be used to demonstrate and evaluate the 8-channel capacitive touch and proximity switch. The PCB is designed to make it easy to adjust the switch's sensitivity. The board can be powered with 3.3 V or 5 V and the communication will be made through the I ² C interface.



Revision history

Rev	Date	Description
1	20130129	New user manual, first revision

Contact information

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1. Introduction

The PCx8885 is a capacitive touch and proximity sensor with 8 sensor channels. In order to help customers to evaluate NXP's sensor technology and help to optimize their sensor structures, this evaluation board OM11056 has been designed.

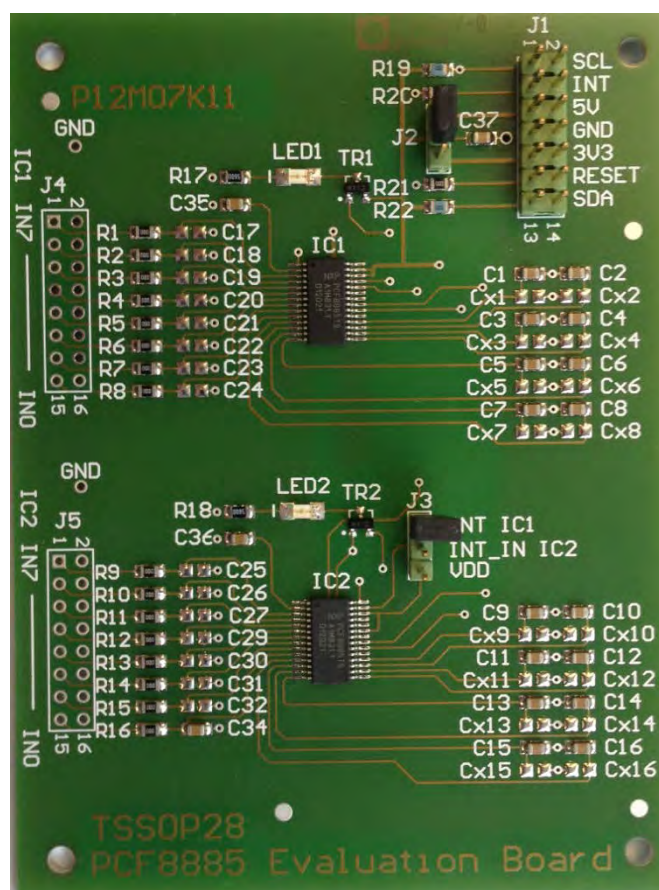


Fig 1. OM11056 evaluation board

1.1 Key features

1. PCB with two PCA8885 packages
2. Sensitivity for each channel can be set individually
3. LEDs to indicate channel activated
4. I²C interface

1.1.1 Schematics

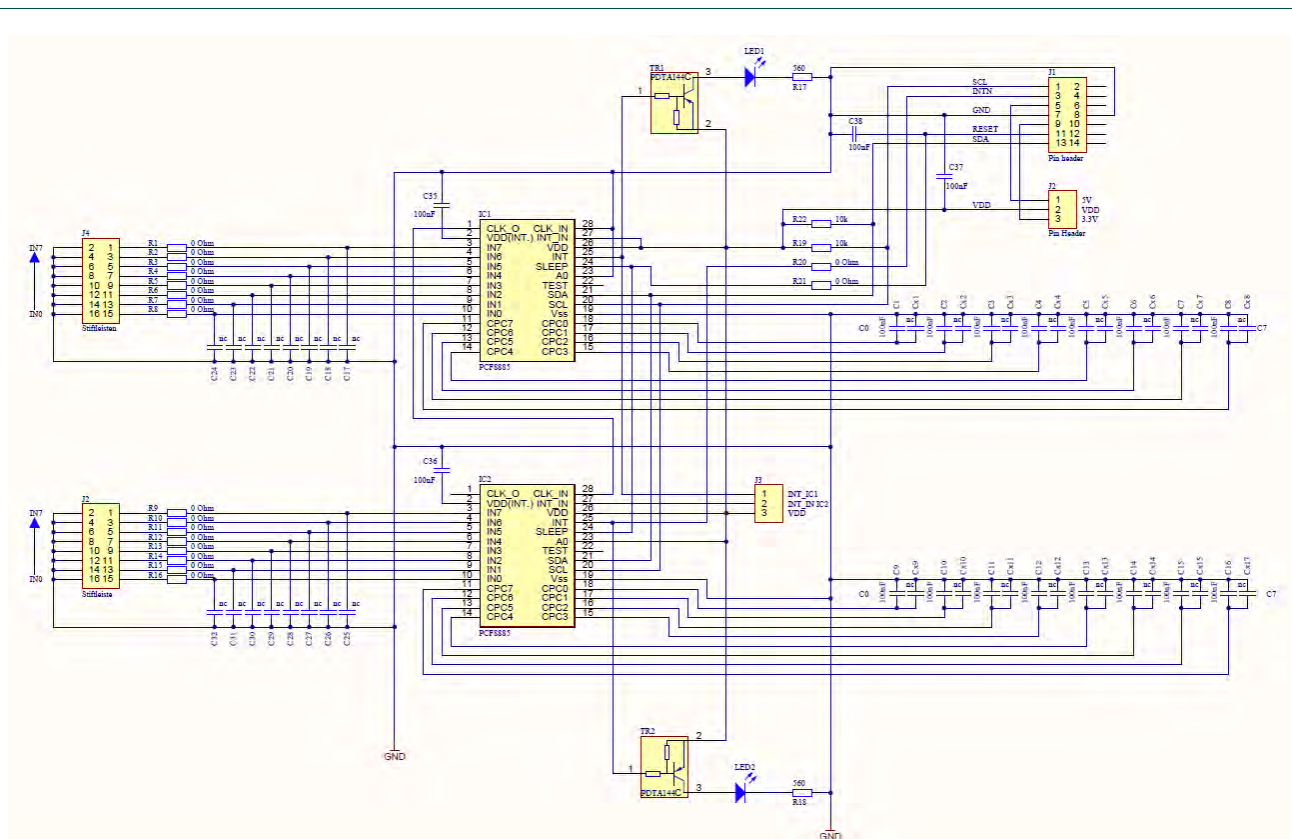


Fig 2. Schematic board layout

1.1.2 I²C interface and supply voltage

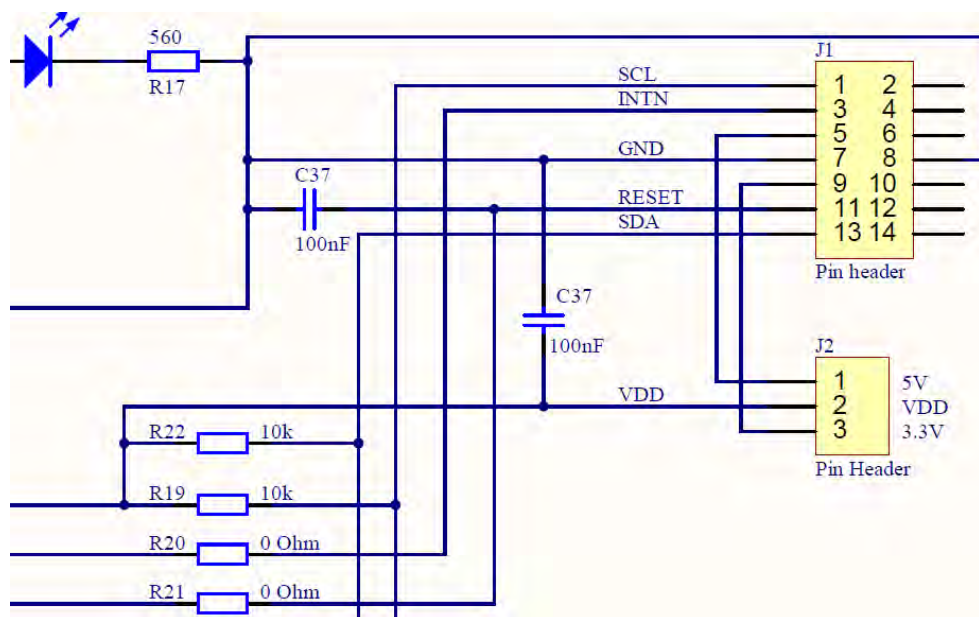


Fig 3. I²C and power connector

Table 1. J1 pin description

Pin	Description
1	I ² C, clock line
3	INT_N, Interrupt output from sensor ICs
5	Supply voltage 5 V
7, 8	GND
9	Supply voltage 3.3 V
11	RESET, this pin is wired to the SLEEP pin of the sensor ICs
13	I ² C, data line
2,4,6, 10, 12, 14	Not used

J2 allows use of two different supply sources.

1.1.3 Cascading two sensor ICs

Two PCF8885 packages can be cascaded to drive either an 8 x 8 matrix key pad or 16 simple touch keys. Cascading means that the sampling clock from the primary IC is fed into the secondary IC for synchronized sampling and the INT_N signals are ORed through the secondary IC. The primary IC will sample at the rising edge of the clock and the secondary IC on the falling edge of the clock. A high sampling rate can be maintained.

A jumper has to be inserted on J3, (pin1-2) to connect the INT_N signal from the primary IC to the secondary IC.

For single chip configuration pin2 should be connected to VDD (pin2-3).

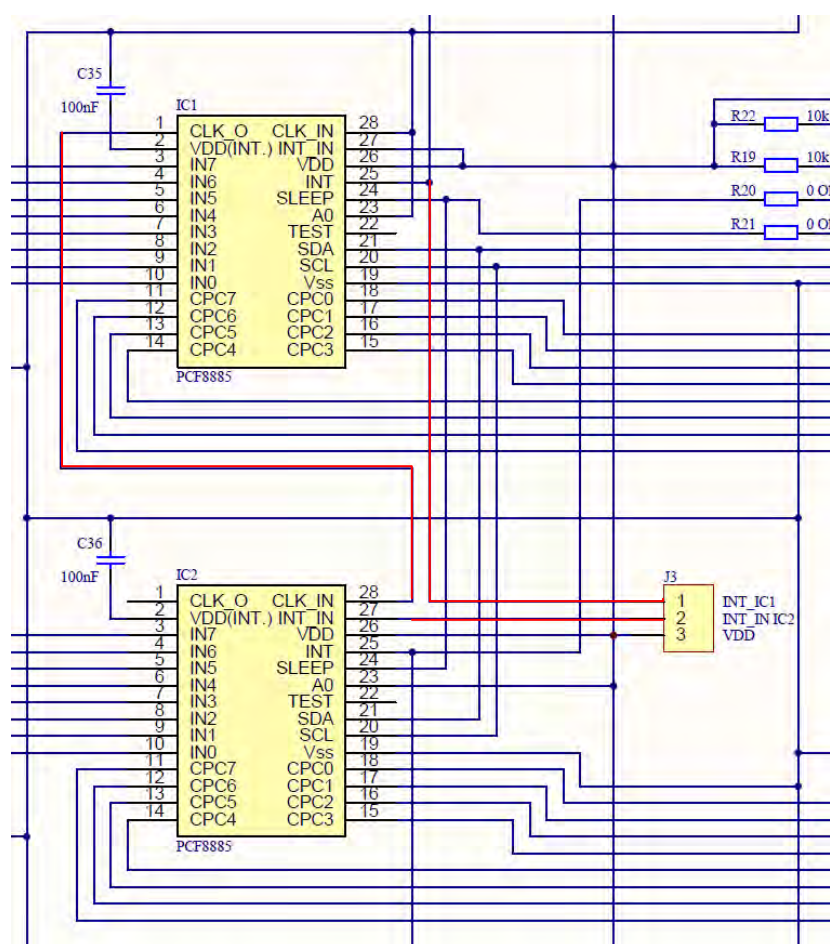


Fig 4. Schematic layout of the cascade

1.1.4 Sensor inputs and sensitivity

Capacitive loads through the entire specification range can be connected to the sensor inputs for the two ICs on the board. For capacitive loads beyond the specification ($> 40 \text{ pF}$), resistors can be mounted in parallel to the sensor input to help the auto-calibration mechanism. In the latter case, the resistor value can start from $100 \text{ k}\Omega$ and down till optimal operation is obtained.

For applications where remote sensor pads are exposed to RF noise, low-pass filters can be built by using the resistors in series (R1 to R8) and the capacitors in parallel (C17 to C24).

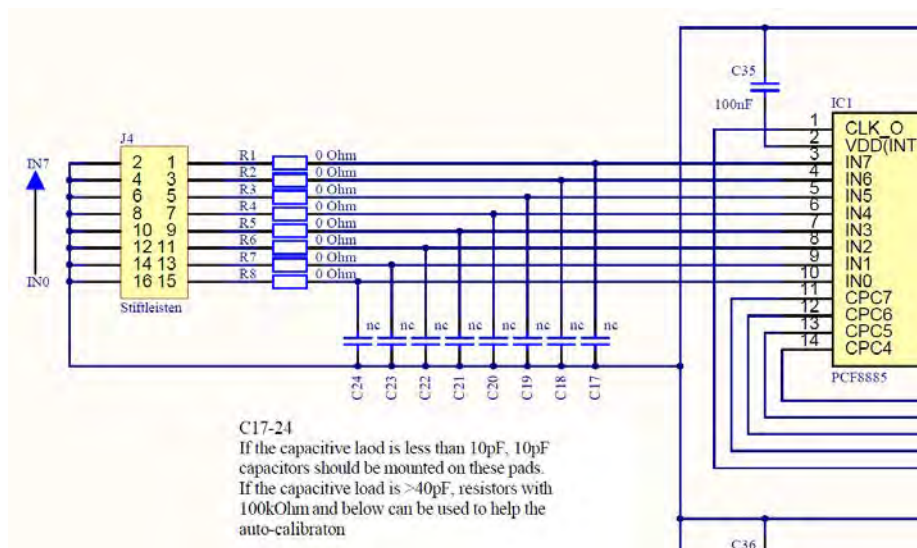


Fig 5. Resistors and capacitors on the board

1.1.5 Setting the sensitivity

The sensitivity is proportional to the CPC capacitor value for each channel. Default capacitance is 100 nF and there are additional pads for capacitors in parallel in case higher sensitivity is required. The CPC capacitors are specified in the range of 100 nF to 470 nF in the datasheet. These limits are only indicative, expected to cover entire range for sensitivity. Based on the size of the sensor pads and surrounding conductors, the CPC capacitance range can be extended both in lower and higher limits to 20 nF to 800 nF .

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