UBA2071; UBA2071A

Half bridge control IC for CCFL backlighting

Rev. 01 — 23 June 2008 Product data sheet

1. General description

The UBA2071 and UBA2071A are high voltage ICs intended to drive Cold Cathode Fluorescent Lamps (CCFLs) or External Electrode Fluorescent Lamps (EEFLs) for backlighting applications. They can drive a half bridge circuit made up of two NMOSFETs with a supply voltage of up to 550 V, so the inverter can be supplied directly from a 400 V PFC bus.

The UBA2071 and UBA2071A contain a controller, a level shifter, a bootstrap diode and drivers for the external half bridge power switches. It also contains a low frequency PWM generator, which can be used to control the brightness level of the lamps, using an analog brightness/dimming control voltage. PWM dimming can also be realized, using a digital PWM input signal. PWM dimming can be synchronized with other ICs. The lamp current is controlled by means of a true zero voltage switching resonant control principle, ensuring lowest possible switch losses in the half bridge power structure.

The UBA2071 is designed to be supplied by a $\Delta V/\Delta t$ supply from the half bridge circuit that it drives. The IC itself needs little current and if the IC is off, a clamp protects the supply voltage from getting too high.

The UBA2071A is designed to be supplied by a fixed 12 V supply. It has a lower supply start voltage and no supply clamp.

2. Features

- Suitable for operating in a very wide inverter supply voltage range (up to 550 V DC).
- Integrated level shifter.
- Integrated bootstrap diode.
- Lamp current control by means of a true zero voltage switching resonant control principle.
- Sample & Hold circuit, maintaining current control value during PWM lamp-off situation.
- Separately definable time constants for current control loop and PWM dimming attack/decay setting.
- Overvoltage control.
- Overcurrent protection.
- Ignition failure detection.
- Hard switching control.
- Arcing detection.
- Open/short pin protections on feedback pins.
- Integrated, programmable fault timer.

- Bidirectional pin acting both as fault signaling output and input, allowing external fault interfacing to operate via the integrated fault timer.
- Brightness level adjustment through PWM dimming.
- Integrated PWM generator.
- Power-down mode.
- Communication pin for master / slave operation.
- DC blocking capacitor pre-charging sequence.
- Supply clamp (UBA2071 only).

3. Applications

- LCD-backlighting, including LCD-TV and LCD-monitor applications. The IC is intended to drive and control a half bridge inverter with resonant load circuit for CCFLs, but can also drive an array of External Electrode Fluorescent Lamps (EEFLs).

4. Quick reference data

Table 1. Quick reference data.

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN} = V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together. Currents are positive when flowing into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{SH}	voltage on pin SH			-	-	550	V
V_{VDD}	voltage on pin VDD			-	-	14	V
I_{VDD}	current on pin VDD	EN pin grounded; V_{VDD} = 14.0 V; UBA2071AT and UBA2071ATS		-	-	0.22	mA
		oscillating at $f_{sw(min)}$; C_{CF} = 100 pF		1.2	1.5	1.8	mA
		disabled; V_{VDD} = 11 V		-	0.16	-	mA
		oscillating; CF = 100 pF; GL and GH open		-	1.5	-	mA
		C_{CF} = 100 pF; V_{PWMD} = H; V_{CSWP} = 0 V		1.0	1.2	1.4	mA
$f_{sw(min)}$	minimum switching frequency	C_{CF} = 100 pF	[1] [2]	10	-	100	kHz
			[1] [2]	38	40	42	kHz
$f_{sw(max)}/f_{sw(min)}$	maximum switching frequency to minimum switching frequency ratio			2.2	2.4	2.6	kHz
$V_{ref(creg)}$	current regulation reference voltage			1.20	1.26	1.32	V

Table 1. Quick reference data.

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN} = V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together. Currents are positive when flowing into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{th(ov)(VFB)}$	overvoltage threshold voltage on pin VFB			2.40	2.50	2.60	V
$t_{to(fault)}$	fault time-out time	C_{CT} = 100 nF		0.85	1.00	1.15	s
$I_{source(drv)}$	driver source current	V_{GL}, V_{GH} = 4 V; V_{VDD} = V_{FS} = 12 V		–105	–90	–75	mA
$R_{sink(drv)}$	driver sink resistance	V_{GL}, V_{GH} = 2 V; V_{VDD} = V_{FS} = 12 V		13.5	16.0	18.5	Ω
f_{PWM}	PWM frequency		[1]	75	-	1000	Hz
δ_{PWMD}	duty cycle on pin PWMD		[3]	12	-	100	%

[1] Given frequency is switching frequency of GL and GH. Sawtooth frequency on CF pin is twice as high.

[2] Can be set by external capacitor

[3] PWMD is active low: A low level on the PWMD pin corresponds with lamps-on. Example: δ_{PWM} = 20 % means PWMD is during 20 % of each cycle low and the lamps are 20 % of the time on, resulting in a light output of 20 %.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
UBA2071T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
UBA2071AT	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
UBA2071TS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
UBA2071ATS	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

6. Block diagram

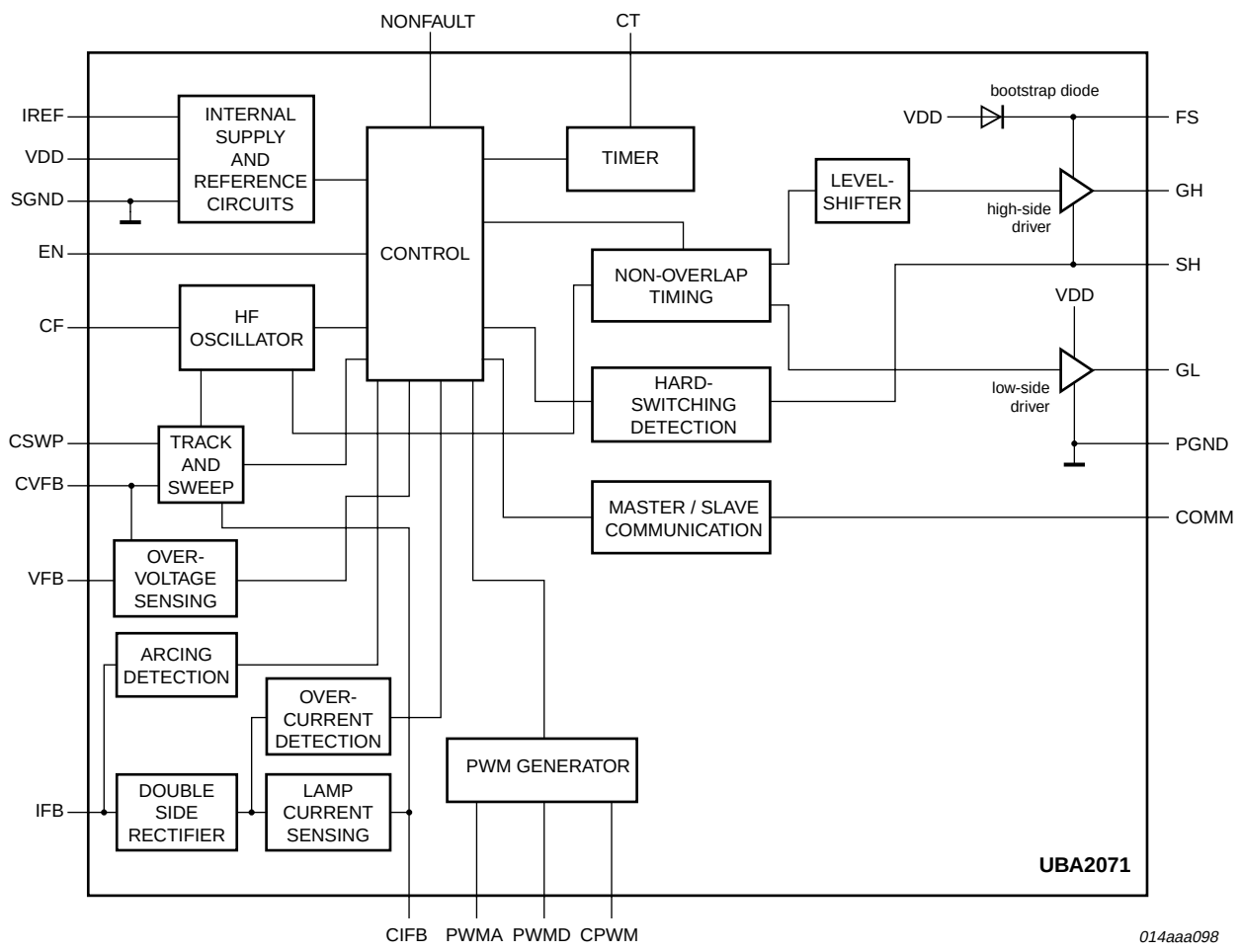


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

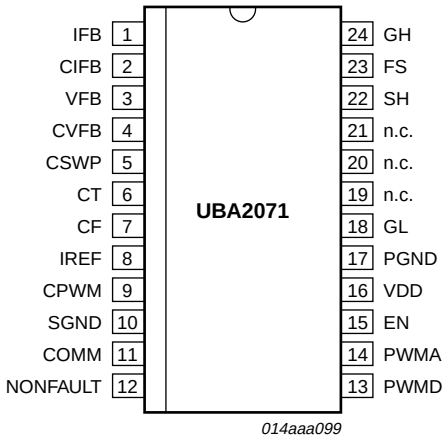


Fig 2. Pin assignment SO24 and SSOP24 package (top view)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description	Function
IFB	1	current feedback input.	Input signal for the lamp current control loop. Should be connected to a voltage proportional to the lamp current.
CIFB	2	current regulation capacitor.	A capacitor must be connected between this pin and the signal ground. It sets the time constant of the lamp current control loop.
VFB	3	voltage feedback input	Input signal for the voltage control loop. Should be connected to a voltage proportional to the transformer output voltage.
CVFB	4	voltage regulation capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time constant of the voltage control loop.
CSWP	5	frequency sweep capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time in which the HF frequency is swept up from regulation level to the maximum frequency and back during PWM dimming.
CT	6	fault timing capacitor	A capacitor must be connected between this pin and the signal ground. It sets the time that a fault condition is allowed before the IC shuts down itself.
CF	7	HF-oscillator timing capacitor	A capacitor must be connected between this pin and the signal ground. It sets the minimum switching frequency of the half bridge.
IREF	8	reference current output	A 33 kΩ resistor must be connected between this pin and the signal ground. The IC uses it to make accurate internal currents.
CPWM	9	PWM timing capacitor	If a capacitor is connected between this pin and the signal ground, it sets the frequency of the PWM oscillator. If this pin is connected to signal ground the internal PWM oscillator is disabled.
SGND	10	signal ground	
COMM	11	master / slave communication	Via this pin the IC can communicate with a dedicated slave device.

Table 3. Pin description *...continued*

Symbol	Pin	Description	Function
NONFAULT	12	status signal input/output	The IC signals a fault condition to external circuits by pulling this pin low. Also external circuits can signal a fault condition to the IC by pulling this pin low.
PWMD	13	digital PWM dimming input/output	Digital output of internally generated PWM signal if a capacitor is connected to the CPWM pin. Digital input of PWM signal if the CPWM pin is connected to signal ground. **Remark:** The signal on the PWMD pin is active low, so low voltage on the PWMD pin means lamps are on.
PWMA	14	analog PWM dimming input	The duty cycle of the internally generated PWM signal is proportional to the voltage on this pin.
EN	15	chip enable input	A low voltage on this pin will reset and shut down the IC. This pin is also used to select between DC blocking capacitor charging mode and normal operation.
VDD	16	supply input	A buffer capacitor must be connected between this pin and power ground.
PGND	17	power ground	return for the low-side driver.
GL	18	low-side driver output	Gate connection of the low-side power switch.
n.c.	19	not connected	HV spacer pin.
n.c.	20	not connected	HV spacer pin.
n.c.	21	not connected	HV spacer pin.
SH	22	high-side source connection	Return for high side gate driver. Must be connected to the source of the high-side half bridge power switch.
FS	23	floating supply	A buffer capacitor must be connected between this pin and the SH pin. This capacitor is charged when the low-side power switch is on and supplies the high-side driver when the high-side power switch is on.
GH	24	high-side driver output	Gate connection of the high-side half bridge power switch.

8. Functional description

The UBA2071 and UBA2071A are designed to drive a half bridge inverter (as shown in Figure 3) with a resonant load. The load consists typically of a transformer with CCFLs or EEFLs.

The IC has an AC lamp current sense input (IFB). It regulates the average absolute value of the lamp current by varying its switching frequency. The load is presumed to be inductive: higher frequency results in lower lamp current.

The UBA2071 and UBA2071A include a PWM dimming function. The ICs switch the lamps on and off with a frequency lower than the lamp current frequency but higher than what the human eye can see. The light output of the lamps can be set by setting the ratio of the on-time and off-time.

These ICs have several forms of protection and the next chapters will describe each function in more detail.

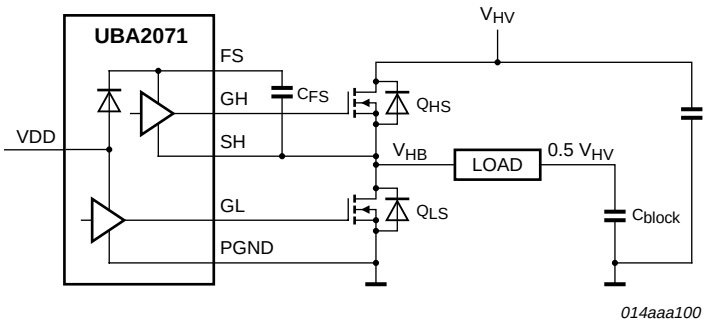


Fig 3. Basic half bridge inverter

8.1 Supply, Start-up and UnderVoltage LockOut (UVLO)

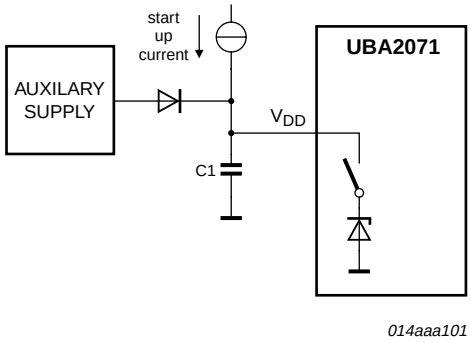


Fig 4. Supply configuration (for UBA2071 only)

The UBA2071 is supplied via the VDD pin as shown in Figure 4. The supply voltage is either made by the inverter itself, using a $\Delta V/\Delta t$ or is a auxiliary fixed supply voltage. A start-up current source that can supply minimal $I_{startup(VDD)}$ is needed for start-up. This can be a resistor to the half bridge supply voltage.

The IC starts up when the voltage at the VDD pin goes over $V_{startup(VDD)}$ and shuts down when the voltage at the VDD pin drops below $V_{stop(VDD)}$ and the output GL is high[1]. The hysteresis between the start and stop levels allows the IC to be supplied by the supply buffer capacitor (C1 in Figure 4) until the auxiliary supply is settled. The auxiliary supply must not exceed the maximum voltage allowed on the VDD pin and has to be above $V_{stop(VDD)}$.

The UBA2071A can directly be supplied by a fixed voltage source on the VDD pin. The voltage supplied by this source has to be above the maximum value of $V_{startup(VDD)}$ but below the maximum of V_{VDD}. Typically it will be a 12 V ± 5 % source.

1. When both GH and GL are low, during the lamps-off period of PWM dimming (PWMD is high), the IC will shut down until the PWMD is low and the GL is high again.

8.2 V_{DD} clamp

When the UBA2071 is disabled (EN pin low) or in the stop state, the V_{DD} clamp is activated. The V_{DD} clamp is an internal active zener limiting the voltage to $V_{clamp(VDD)}$. It prevents the start-up current source from charging the V_{DD} buffer capacitor to too high a voltage.

The maximum current that is allowed to be delivered by the start-up current source is determined by the clamp voltage as stated in Table 6 and the maximum allowed V_{DD} voltage as stated in Table 4.

The UBA2071A has no V_{DD} clamp.

8.3 Enable

The UBA2071 or UBA2071A can be activated or set to standby via the EN pin. If the voltage on the EN pin is below $V_{th(L)(EN)}$, the IC will stop oscillating at the next GL high state[2], and most parts of the internal circuits will shut down. When the EN pin is left open, it is pulled low by an internal bias current of $I_{bias(EN)}$.

When the voltage on the EN pin comes above $V_{th(H)1(EN)}$, the IC will start up in DC blocking capacitor charging mode (see Section 8.8). When the voltage on the EN pin goes over $V_{th(H)2(EN)}$, the IC will start with the initial ignition frequency sweep (see Section 8.8) and subsequently go to normal operation mode again.

8.4 The oscillator

The UBA2071 and UBA2071A have an internal voltage controlled sawtooth oscillator, see Figure 5. Its frequency inverses in proportion to the capacitor connected to the CF pin. The IC switches GL on and GH off during one oscillator period and GL off and GH on during the next oscillator period. This results in a half bridge voltage with a frequency (called the switching frequency f_{sw} from here on) of half the oscillator frequency and with a duty cycle of exactly 50 %.

The oscillator frequency is controlled by changing the charge current at the CF pin. By changing the frequency the lamp current is controlled. It is also used to limit the transformer output voltage and for gradually switching the lamps on and off during PWM dimming.

2. When both GH and GL are low during the lamps off period of PWM dimming (so PWMD is high), the IC will wait with entering the standby state until PWMD becomes low again and GL can be made high.

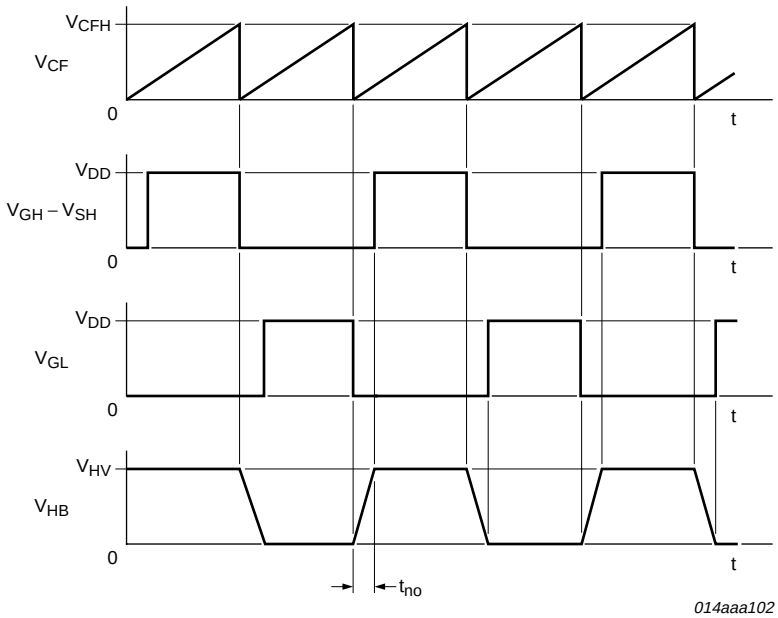


Fig 5. Oscillator, driver and half bridge voltages

8.5 Non-overlap

During each transition between the two states GL high/GH low and GL low/GH high, GL and GH will both be low for a fixed time t_{no} (non-overlap time) to allow the half bridge point to be charged or discharged by the load current (presuming the load always has an inductive behavior), and thus enabling zero voltage switching, see Figure 5.

8.6 Low-side and high-side drivers

The low-side and high-side drivers are identical. The output of each driver is connected to the equivalent gate of an external power MOSFET. The high-side driver is supplied by the bootstrap capacitor, which is charged from the V_{DD} voltage via an internal diode when the low-side power MOSFETs is on. The low-side driver is directly supplied by the V_{DD} voltage.

8.7 DC blocking capacitor charging

When the IC is off, either because V_{VDD} is too low, it is disabled via the EN pin, or it stopped after the time-out period during a fault condition, the low-side power switch (Q_{LS} in Figure 3) is turned on by making GL high. This ensures that the supply buffer capacitor of the floating supply (C_{FS} in Figure 3) is fully charged at start-up. As a side effect the DC blocking capacitor (C_{block} in Figure 3) will be completely discharged at start-up. To prevent large inrush currents during the first switching cycles the UBA2071 and UBA2071A can first charge the DC blocking capacitor at start-up.

When the voltage on the EN pin goes over $V_{th(H)1(EN)}$ after the IC has been disabled (EN pin below $V_{th(L)(EN)}$) the IC will start up in DC blocking capacitor charging mode[3]. When the voltage on the EN pin goes over $V_{th(H)1(EN)}$ after the IC has been off (EN pin below $V_{th(L)(EN)}$ or V_{DD} below $V_{stop(VDD)}$) the IC will start up in DC blocking capacitor charging mode. When the voltage on the EN pin goes over $V_{th(H)2(EN)}$ the IC will continue with the initial ignition frequency sweep and normal operation mode. Figure 6, EN configuration, shows three examples of how the enable input can be used:

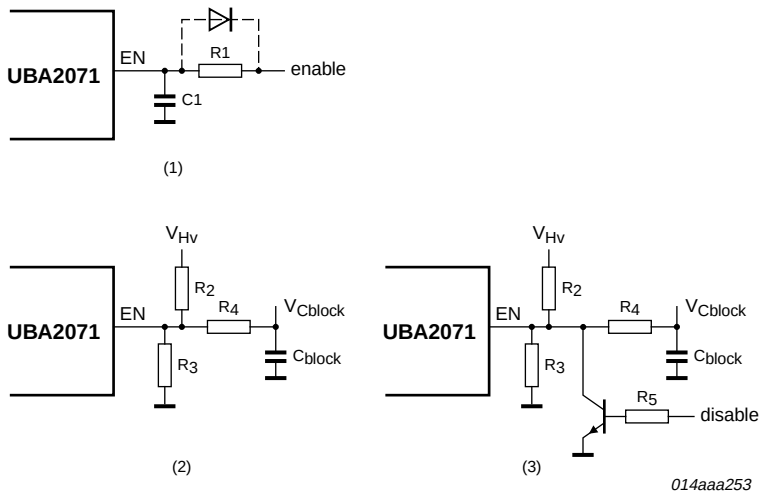


Fig 6. EN configuration

1. Digital enable input with DC blocking capacitor charging. R1 and C1 define a fixed DC blocking capacitor charging time.

   Remark: The digital input signal high level has to be above the maximum value of $V_{th(H)2(EN)}$.

2. Sensing of HV supply and DC blocking capacitor voltages via the EN pin. The IC will start in DC blocking capacitor charging mode if V_{VDD} is above $V_{startup(VDD)}$ and V_{HV} is above $((R2/R4) + (R2/R3) + 1) \times V_{th(H)1(EN)}$. It will then go into initial ignition frequency sweep and normal operation mode once V_{Cblock} has been charged to $(((R4/R2) + (R4/R3) + 1) \times V_{th(H)2(EN)} - R4/R2 \times V_{HV})$.

3. Sensing of HV supply and DC blocking capacitor voltages via the EN pin combined with digital enable input.

In DC blocking capacitor charging mode the low-side power switch (Q_{LS} in Figure 3) is turned on for a period ($(1/f_{sw(max)}) - t_{no}$) and then the high-side power switch (Q_{HS} in Figure 3) is turned on for a period ($(1/f_{sw(max)}) - t_{no}$) followed by a period of ($3/f_{sw(min)}$) during which both power switches are off. This is repeated until the mode is left. When leaving the DC blocking capacitor charging mode by raising the EN pin above $V_{th(H)2(EN)}$, the running cycle of the DC blocking capacitor charging mode will first be completed (see Figure 7).

3. When the enable input is kept high during the time that the IC is off, because the supply voltage is too low, the IC might not start in DC blocking capacitor charging mode.

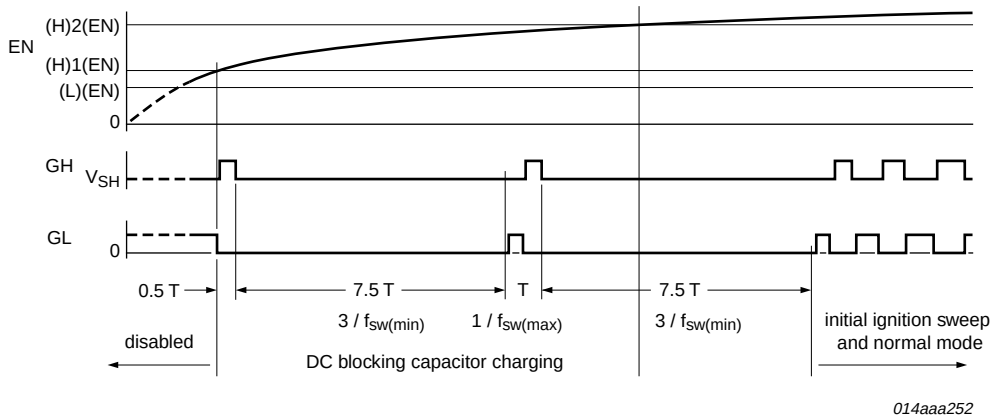


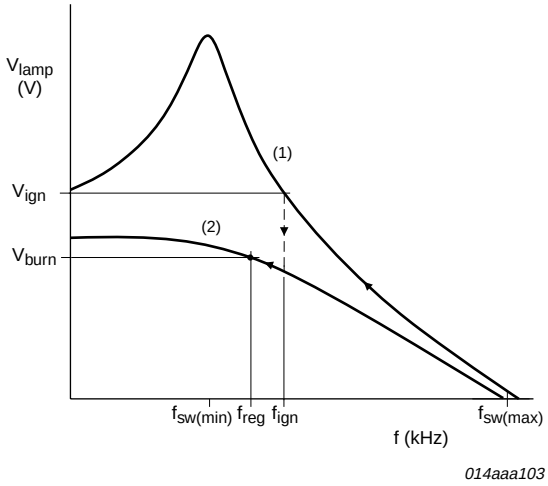
Fig 7. DC blocking capacitor charging mode

Remark: Due to the nature of the charging sequence, V_{Cblock} will automatically be charged to $0.5 \times V_{HV}$ (when given enough time). If the IC is kept in DC blocking capacitor charging mode longer than necessary, V_{Cblock} will remain $0.5 \times V_{HV}$. Therefor the time constant made by R1 and C1 in example A in Figure 6, is not critical. However, since V_{Cblock} cannot become more than $0.5 \times V_{HV}$, it is important to take a lower target value for V_{Cblock} than $0.5 \times V_{HV}$ (with enough margin) in examples B and C of Figure 6, otherwise the IC may get stuck in DC blocking capacitor charging mode.

8.8 Lamp (re-)ignition

The IC starts at its maximum switching frequency $f_{sw(max)}$. The lamp current and the lamp voltage control loops are enabled. The frequency is swept down towards the minimum frequency $f_{sw(min)}$, see Figure 9. During this initial ignition frequency sweep the lamp voltage will increase as the frequency comes closer to the resonant frequency of the unloaded resonance circuit. Once the ignition voltage V_{ign} is reached the lamps will ignite and the lamp voltage will drop[4] to the voltage of the loaded resonance curve, see Figure 8.

4. For CCFLs only.



(1) Indicates lamp-OFF.

(2) Indicates lamp-ON.

Fig 8. Initial ignition of cold cathode fluorescent lamp via frequency sweep and load resonance

Advantage of the sweep rather than a fixed ignition frequency is that sensitivity for spread in resonance frequency is much lower.

Once the lamps are ignited the frequency sweep-down continues, gradually increasing the lamp current (the resonance circuit should now still be inductive, so current increases as frequency drops) until the current regulation level is reached (at $f_{sw} = f_{reg}$). The frequency will not reach $f_{sw(min)}$ if the lamp current comes into regulation. Once it has been detected that the lamps are on (if the average absolute voltage at the current feedback input (pin IFB) is above $V_{th(lod)(IFB)}$) PWM dimming is enabled. See Figure 9.

The initial ignition frequency sweep and the PWM generator are not synchronized. Once the regulation frequency is reached, PWM dimming can start anywhere in its cycle. A small internal PWM dimming enable delay time, $t_{d(en)PWM}$, allows the lamps to settle before PWM dimming starts.

At the start of the lamps-off period of the PWM dimming, the switching frequency is swept up to $f_{sw(max)}$. This reduces the lamp voltage so the lamps go out. If $f_{sw(max)}$ is reached, both GL and GH are made low, so both half bridge powers will be non-conducting. This is indicated by the dotted part of the switching frequency (f_{sw}) line in Figure 9.

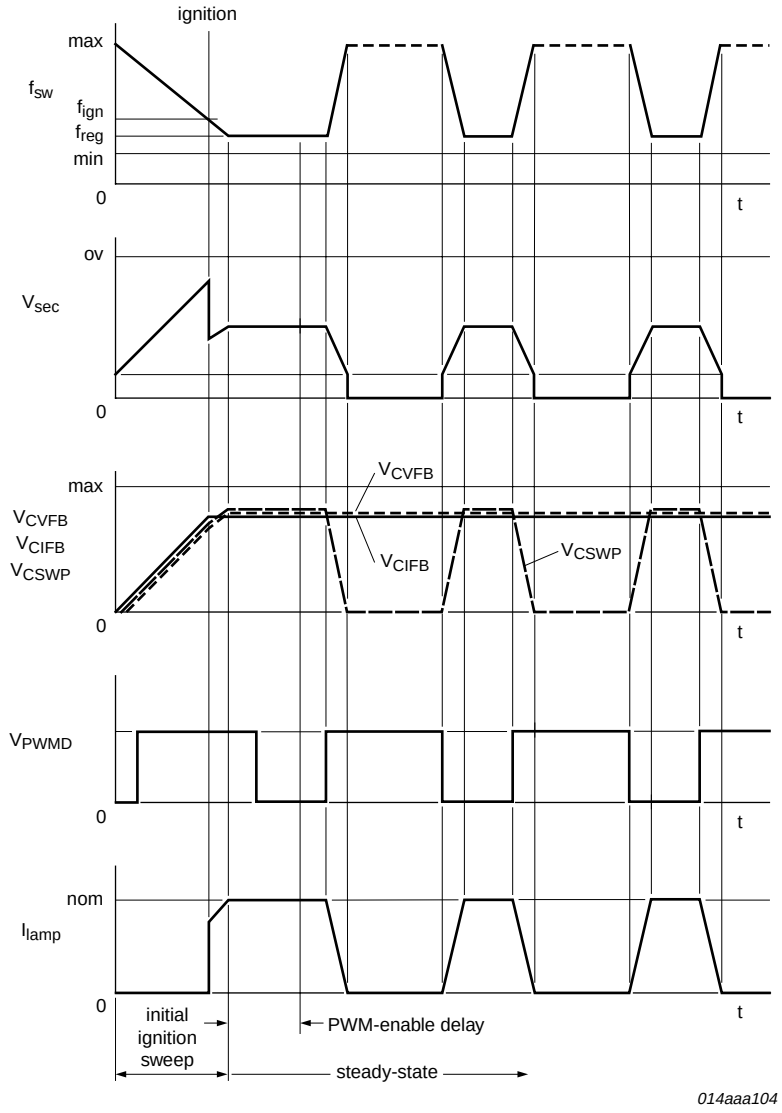


Fig 9. Initial ignition frequency sweep and PWM dimming frequency sweep signals

The lamps start switching again on period GL and GH and the frequency is swept back to the regulation frequency f_{reg}. The duration of the PWM frequency sweep is inverse proportional to the capacitor connected to the CSWP pin.

8.9 Overvoltage control

The overvoltage control circuit is intended to prevent the transformer output voltage from exceeding its maximum rating. It can also be used to regulate the output voltage to the required lamp ignition voltage.

Under normal circumstances the capacitor at the CVFB pin is charged by a constant bias current $I_{ch(CVFB)}$, thus the voltage on the CVFB pin will increase resulting in a decrease of switching frequency. If the IC is in current regulation this bias current will flow away via a tracking circuit which makes the voltage on the CVFB pin following the voltage on the CIFB pin, see Figure 11.

When the voltage on the VFB pin exceeds $V_{th(ov)(VFB)}$, a fault condition is signalled (for handling of fault conditions, see Section 8.14) and the bias current at the CVFB pin changed to the discharge current $I_{dch(CVFB)}$. As a result, the switching frequency increases and the output voltage of the transformer will decrease[5]. As soon as the voltage at the VFB pin drops below $V_{th(ov)(VFB)}$, the CVFB capacitor is charged again and the output voltage of the transformer will increase again. Because the charging and discharging of the CVFB capacitor follows the ripple on the VFB pin voltage, the feedback gain of the voltage control loop is set by the ripple on the feedback signal.

The voltage at the CVFB pin is limited by the oscillator circuit to $V_{CVFB(max)}$ when the minimum switching frequency $f_{sw(min)}$ is reached, see Figure 10. This ensures an immediate frequency increase when overvoltage is detected.

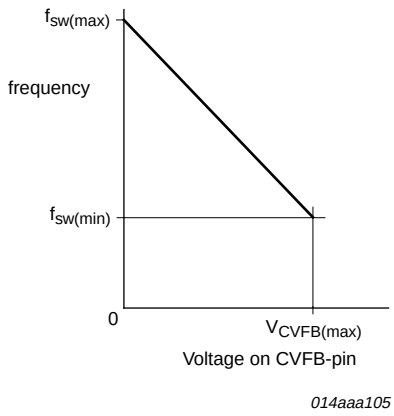


Fig 10. Frequency function of CVFB voltage

8.10 Lamp current control

The lamp current control is always active when the IC is on, except if the lamps are off during PWM dimming. The AC lamp current is sensed by an external resistor connected to the IFB pin, see Figure 11. The resulting AC voltage on the IFB pin is internally Double-Sided Rectified (DSR) and compared to a reference level $V_{ref(creg)}$ by an Operational Transconductance Amplifier (OTA).

When the current is being regulated, switch S1 is closed (conducting). The output current of the OTA is fed into capacitor C1, which is connected to the CIFB pin. So C1 is charged and discharged according to the voltage on the IFB pin.

5. Presuming that the load impedance is in inductive region.

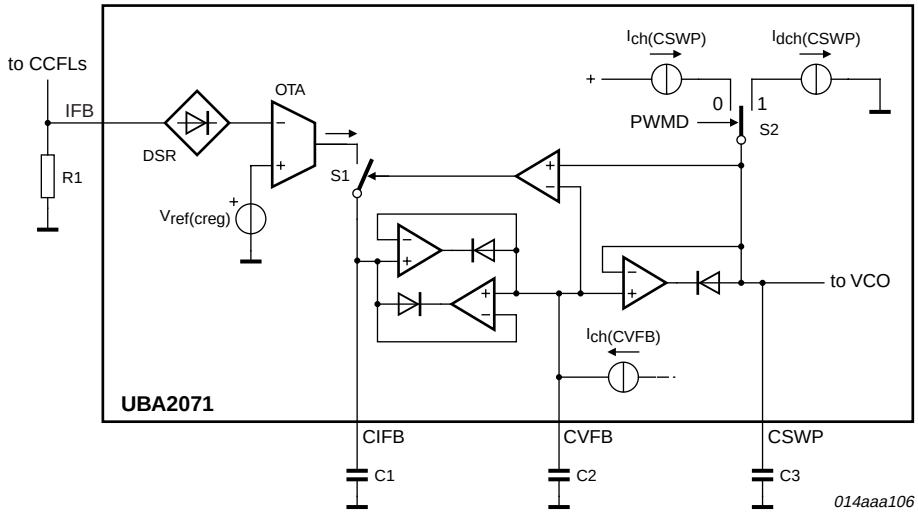


Fig 11. Lamp frequency control circuit

Under normal operating conditions, the voltage across capacitor C2, which is connected to the CVFB pin, will follow the voltage on the CIFB pin. During the lamps-on period of the PWM dimming, the voltage across C3, which is connected to the CSWP pin, will follow the voltage on the CVFB pin and therefore also the voltage on the CIFB pin.

The voltage on the CSWP pin is connected to the VCO input of the HF oscillator and thus controls the switching frequency. If the load is assumed to be inductive an increase in the frequency will cause a decrease in the lamp current, while a decrease in the frequency will cause an increase in the lamp current.

The advantage of having a separate current regulation loop timing capacitor pin CIFB next to the voltage regulation loop timing capacitor CVFB is that time constants for both loops can be set independently. The separate PWM dimming sweep timing capacitor pin CSWP makes it possible to set the PWM dimming sweep speed independent of the current and voltage regulation loops.

8.11 PWM dimming

Pulse Width Modulation (PWM) dimming is a method of reducing the average lamp light output by switching the lamps on and off with a repetition rate or PWM frequency, f_{PWM}, high enough not to be seen by the human eye (but much lower than the inverter frequency f_{sw}). By varying the lamp-on to lamp-off, period ratio, called the duty cycle δ_{PWM}, the light output can be varied over a wide range.

The voltage at the CSWP pin determines the actual switching frequency, it inverses in proportion to the switching frequency. During the lamps-on period of the PWM dimming it follows the voltage at the CVFB pin (the current $I_{ch(CSWP)}$ is drained by the tracking circuit between the CVFB pin and the CSWP pin).

Just prior to transitioning towards the lamps-off period of the PWM dimming the lamp current control loop, see Figure 11, is opened by opening switches S1. The voltage on the CSWP pin is swept down, decaying the lamp current, leading in the PWM lamp-off situation, after which the half bridge switch actions are stopped, resulting in true zero lamp current. see Figure 9. In the meantime the regulation level is preserved in C1 and C2. The

PWM lamp-on situation is reached again through a reverse sequence of events, starting the half bridge actions, increasing the voltage on CSWP, increasing the lamp current back to the controlled value. Switch S1 is closed (conducting) again when the voltage on the CSWP pin has reached the voltage on the CVFB pin again.

The IC waits until the CSWP sweep-up[6] has reached the current/voltage control level at the CVFB pin before sweeping down. This prevents the lamps from going out completely when deep dimming on CSWP pin is combined with a large value capacitor.

After the switching frequency has reached $f_{sw(max)}$, both GL and GH are made low, so both half bridge powers will be non-conducting, see Figure 12. This guarantees zero lamp current during the PWM-off period[7], while the CSWP frequency sweep acts as soft stop and soft restart, of which the softness can be set by the value of the capacitor connected to the CSWP pin.

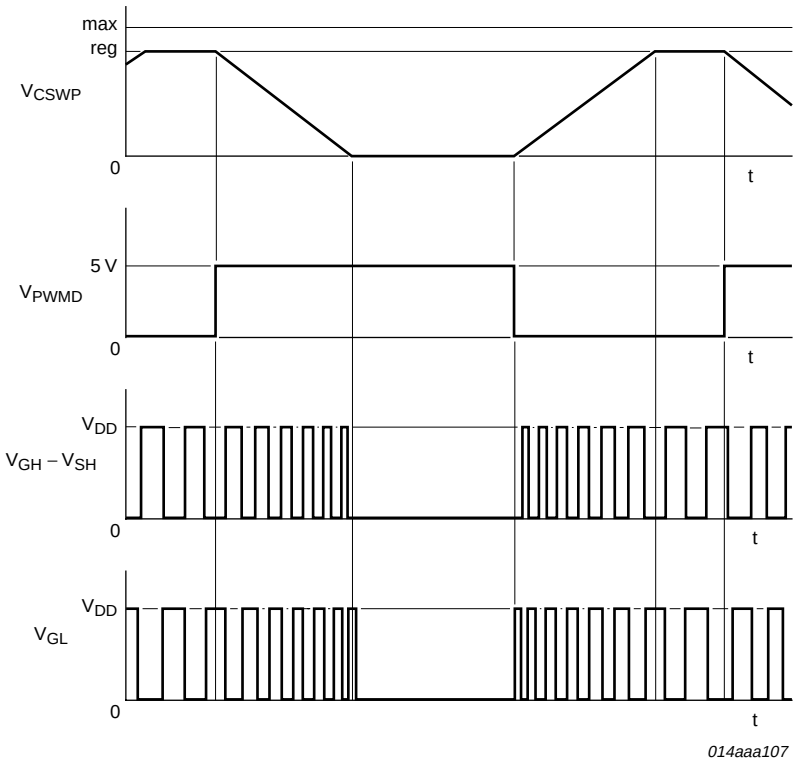


Fig 12. PWM dim cycle waveforms

Three pins are available to configure the internal PWM generator: the CPWM pin, PWMA pin, and the PWMD pin. The two possible PWM configurations are shown in Figure 13. In the analog or master mode the internal PWM generator is active and generating the PWM signal. This signal is put on the PWMD pin, which is automatically configured as an output. The minimum duty cycle of the internal PWM generator is limited to $\delta_{PWM(min)}$.

6. CSWP sweep-up is frequency sweep-down.
7. Until the ringing of voltage on the half bridge point has died away, some (capacitive) current may still cause a light glow at the hot side of the lamps. Therefore it is advised to maximize the attenuation of the ringing circuit (made up by the transformer inductance and the $\Delta V/\Delta t$ limiting capacitor).

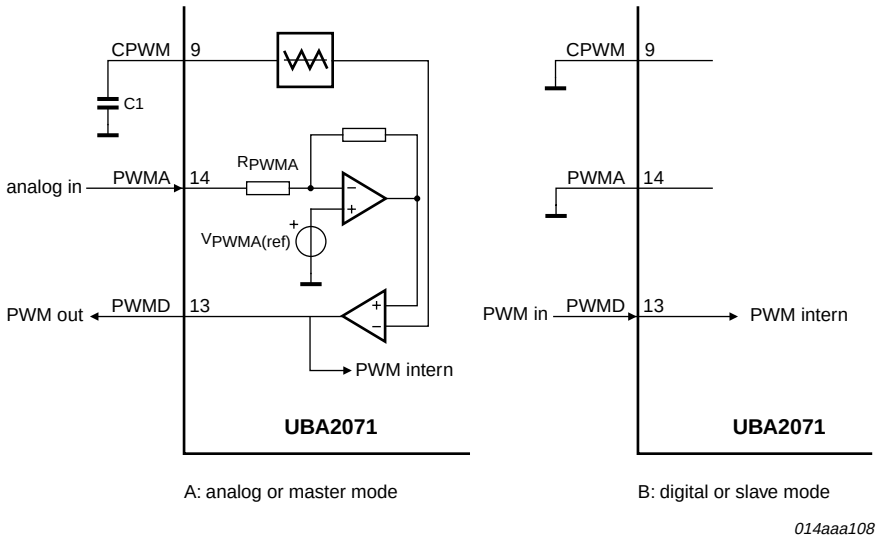


Fig 13. PWM dimming configurations

When the CPWM pin is connected to ground the IC is put in digital or slave mode and the PWMD pin is an input. The internal PWM generator is not used. The IC uses the PWM signal provided on the PWMD pin.

PWM dimming of multiple ICs can be synchronized by configuring one IC as master and the others as slaves and connecting all PWMD pins together.

The PWMD input/output is active low. A voltage below $V_{th(L)(PWMD)}$ on the pin will turn the lamps on, while a voltage above $V_{th(H)(PWMD)}$ will turn the lamps off.

PWM dimming is only enabled in normal mode, when no fault condition exists. The only exception is when an external detected fault condition is entered via the NONFAULT pin, then PWM dimming remains active, see Figure 15.

8.12 The fault timer

The fault timer provides a delay in between the detection of a fault and the shutdown of the IC (enter STOP state). Its time is controlled by a capacitor at the CT pin.

Any fault condition will start the timer. When the timer is activated, the capacitor at the CT pin will be alternatively charged and discharged, see Figure 14. After the fault output delay time, $t_{d(o)fault)}$, the NONFAULT pin is activated (pulled low). This is to signal to any external circuit that a fault has been detected and the IC will stop if that fault continues. After the fault time-out period $t_{to(fault)}$ is reached the IC will enter STOP state.

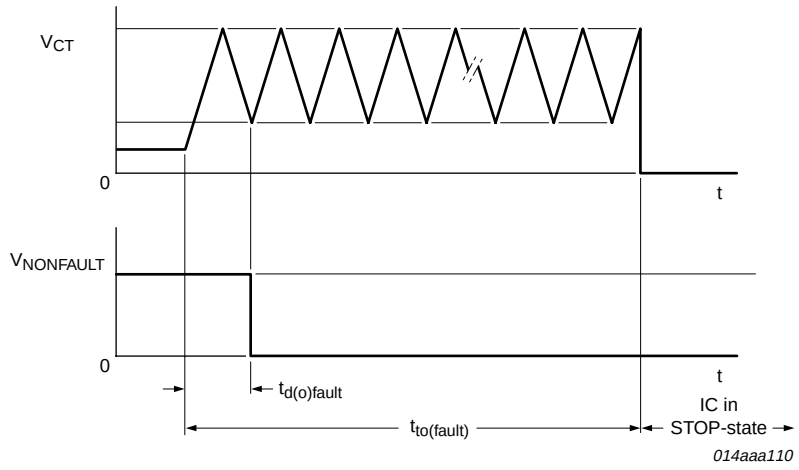


Fig 14. Fault timer waveforms

If the fault timer is inactive, the CT pin voltage is 1 Vbe, about 0.7 V. The CT timer has a protection that prevents the IC to start up if the CT pin is shorted to GND.

8.13 Communication

The UBA2071 and UBA2071A have a dedicated communication pin, the COMM pin, for communicating with a slave half bridge driver (like the UBA2073), for instance for use in a balanced half bridge driver configuration.

Via the COMM pin, a clock signal and a signal to indicate that both half bridge powers are to be turned off are exported and a fault signal is imported. The clock signal is a digital signal with a low level $V_{L(clk)(COMM)}$ and a high level $V_{H(clk)(COMM)}$. To signal that both half bridge powers should be turned off, the voltage at the COMM pin is raised to $V_{O(hbswoff)(COMM)}$.

The UBA2071 and UBA2071A look at the current drawn from the COMM pin during the clock high period for a hard switching signal from the slave half bridge driver. First, a non-overlap time period t_{no} is discarded to prevent that a capacitive load on the communication line is seen as a signal. Then the detected current is averaged over the clock high period before being compared to the reference level $I_{th(det)hsw(COMM)}$. The current value is sampled on the falling edge of the clock signal and held during the clock low period. The received signal is treated as equal to an internal hard switching detection (so PWM dimming will be disabled, switching frequency will be increased and fault timer will be started).

When only the UBA2071 or UBA2071A is used, the COMM pin must be “not connected”.

8.14 Protections

All fault conditions and how they are processed in the IC can be found in Figure 15.

The UBA2071 and UBA2071A have the following protections:

- OverVoltage Protection (OVP),
- OverVoltage Extra protection (OVE),

- OverCurrent Protection (OCP),
- bad contact or ARCing (ARC),
- Ignition Failure (IF),
- open or shorted current feedback (IFB pin open/short),
- open or shorted voltage feedback (VFB pin open/short)
- Hard Switching (HS).

There are also two pins, the NONFAULT pin and the COMM pin, via which a fault can be signalled to the IC, by an external circuit.

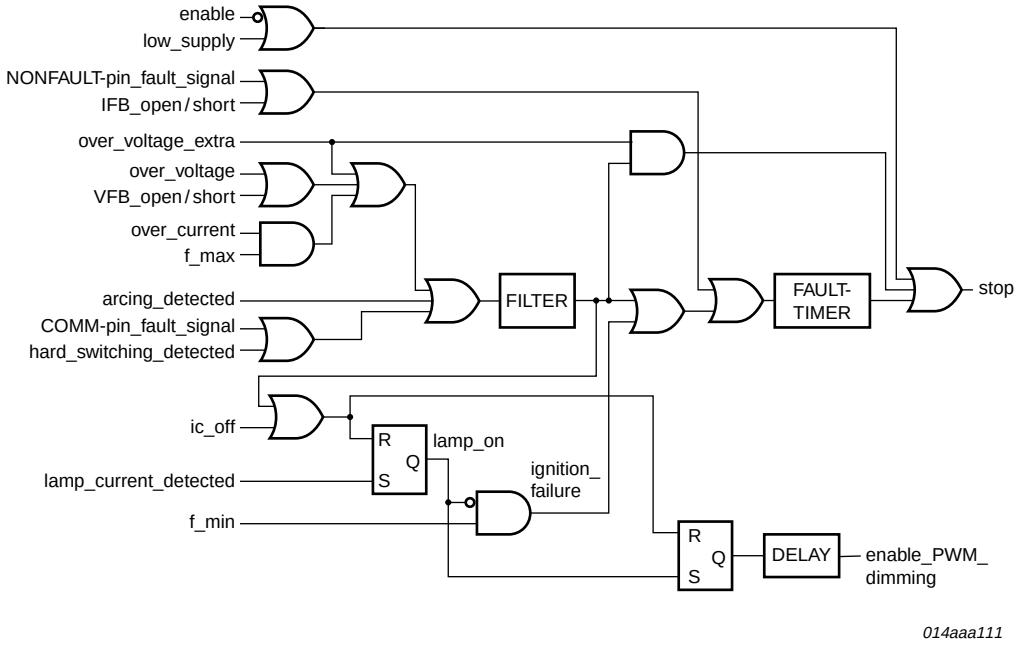


Fig 15. Simplified control schematic

The fault protection functions are explained in the following sections.

8.14.1 Voltage feedback open or short protection

If the VFB pin is left open or shorted to SGND, the voltage at the VFB pin will drop below the VFB open/short protection threshold voltage $V_{th(osp)VFB}$, due to the internal bias resistor $R_{i(VFB)}$. If the voltage at the VFB pin is below $V_{th(osp)VFB}$ continuously or only during a part of each switching cycle the PWM dimming is disabled and the fault timer is started.

To protect the inverter transformer(s) against overvoltage if the voltage feedback loop is broken, the frequency stays at $f_{sw(max)}$ or is increased by discharging the capacitor at the CVFB pin (by $I_{dch(CVFB)}$). For this function the voltage at the VFB pin has to be below $V_{th(osp)VFB}$ during more than 50 % of each switching cycle.

8.14.2 Overvoltage protection

The overvoltage control, see Section 8.9, is intended to prevent the transformer output voltage from exceeding its maximum rating. The overvoltage control level has to be at least at the required lamp ignition voltage, otherwise the lamps may not ignite.

Once the lamps are on and in steady state, the transformer output voltage will usually be about half the required ignition voltage for CCFLs. Thermal design of the transformers is based on this lower voltage, not on the ignition voltage above which the overvoltage control has to be. Hence the circuit might not stay in overvoltage regulation indefinitely. Therefore overvoltage regulation is combined with overvoltage protection.

When the voltage on the VFB pin exceeds the OV reference level $V_{th(ov)(VFB)}$, the CVFB is discharged, an overvoltage fault condition is signalled, PWM dimming is disabled, and the fault timer is started. An internal latch makes the OV fault signal continuously high, even if the voltage at the VFB pin only exceeds $V_{th(ov)(VFB)}$ during part of the output period. So the peak of the voltage on the VFB pin determines if an overvoltage fault condition is seen. An internal filter prevents the overvoltage fault condition from being reset when the voltage at the VFB pin drops below the OV reference level for only one or two hf cycles.

In order to avoid an OV fault condition at the nominal switching frequency (with the lamps operating normally), the voltage ripple on the VFB pin must not be too large.

8.14.3 Hard switching protection

As the UBA2071 and UBA2071A are intended to drive a half bridge at a high voltage, a feature is included to ensure zero voltage switching. The design of the resonant load should guarantee zero voltage switching under normal operating conditions. To prevent overheating due to high switching losses in case of any abnormal operating condition, hard switching of the half bridge is detected internally.

At the moment the high-side switch is turned on, the voltage step at the SH pin is measured. If it is above $V_{th(hsw)(SH)}$ then PWM dimming is disabled and the fault timer is started. Also, the frequency is increased by discharging the capacitor at the CVFB pin (by $I_{dch(CVFB)}$).

8.14.4 Overvoltage extra protection

Though the hard switching protection as described in Section 8.14.3, usually prevents the circuit from getting at the wrong side of the resonance curve of the load (were the load shows capacitive behavior), this might happen for instance when a lamp is suddenly disconnected. The parasitic capacitance of the lamp and its connection wire may make up a significant part of the resonance circuit capacitance, so if a lamp is disconnected the resonance frequency of the remaining load is suddenly higher and the switching frequency might be at the capacitive side. Hard switching will occur and be detected. The result is an increase in the switching frequency, which will make the situation worse: the switching frequency comes closer to the resonance frequency of the remaining load, creating a higher and potentially destructive transformer secondary voltage.

The OverVoltage Extra (OVE), protection prevents damage to the circuit by adding an extra overvoltage protection level with quick response to that. When the voltage on the VFB pin exceeds this OVE level $V_{th(ovextra)(VFB)}$, an OVE fault condition is signalled. The IC will stop if this happens during a couple of subsequent hf cycles. The time it takes before the IC stops depends on a percentage of the time the VFB pin voltage exceeds the OVE level and if hard switching is detected also. Figure 16 shows typical shutdown response

times in case overvoltage and overvoltage extra are detected at the same moment (curve (1)) and if overvoltage, overvoltage extra and hard switching are detected at the same moment (curve (2)). The first parts of the curves are dashed because an internal filter makes that VFB needs to be above $V_{th(ovextra)(VFB)}$ for at least about 1 µs for the overvoltage extra to react at all.

If a normal overvoltage fault was already present for more than about 840 µs before overvoltage extra detection started or hard switching was already detected for more than about 55 µs before overvoltage extra detection started, then the IC will shut down about 1 µs after overvoltage extra is detected.

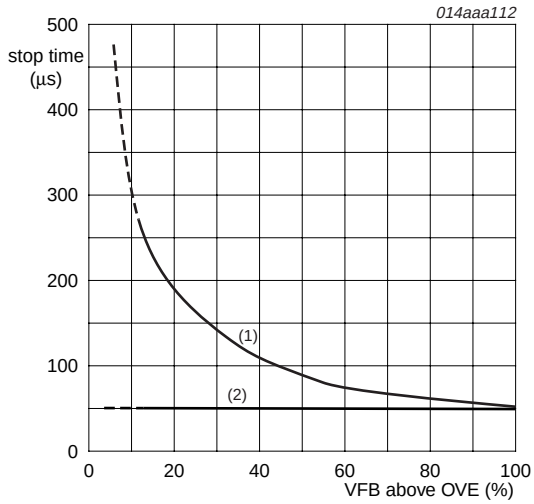


Fig 16. Shutdown time at over voltage extra detection

8.14.5 Current feedback open or short protection

If the IFB pin is left open or shorted to SGND, the peak of the absolute value of the voltage at the IFB pin will be below the IFB open/short protection threshold $V_{th(osp)(IFB)}$ and the fault timer is started.

The IFB open/short protection looks only at the IFB pin voltage if the voltage at the CSWP pin is equal to the voltage at the CVFB pin. During PWM dimming this is when the lamps are on and in current regulation or voltage regulation (so not during PWM lamps-off period and not during the re-ignition frequency sweep).

8.14.6 Overcurrent detection

When the peak of the absolute value of the voltage across the current sense resistor (connected to the IFB pin) exceeds the OC reference level $V_{th(ocd)(IFB)}$ and the IC is oscillating at $f_{sw(max)}$, overcurrent is detected. As result PWM dimming is disabled and the fault timer is started.

8.14.7 Arcing detection

If arcing occurs, for instance due to a bad lamp connection, it causes repetitive short current spikes that can be seen as voltage spikes at the IFB input. The arcing detection circuit is directly connected to the IFB pin, so it can only see spikes with a positive polarity. Usually that will be sufficient. It can detect spikes with amplitude above $V_{th(det)arc(IFB)}$ and a

duration longer than $t_{spike(min)}$. Each spike will trigger an internal one-shot, which signals to the control circuits that arcing has been detected. When arcing is detected, PWM dimming is disabled and the fault timer is started.

8.14.8 Ignition Failure (IF)

When the current control loop comes close to its regulation point, the lamps are assumed to be on (ignited). This is when the average absolute voltage on the IFB pin is above $V_{th(lod)(IFB)}$. If the lamps are not on when the ignition sweep is finished, (switching frequency has reached $f_{sw(min)}$), then an ignition failure is detected, PWM dimming is disabled and the fault timer is started.

8.14.9 The NONFAULT pin

The NONFAULT pin provides bidirectional signalling of the fault status between the IC and any external circuit. When no fault is detected, the voltage on the pin is pulled high to $V_{oc(NONFAULT)}$ by an internal current source.

An external circuit can signal to the IC that a fault has been detected by pulling a current larger than $I_{trig(I)NONFAULT}$ from the NONFAULT pin. The IC will detect the current drawn from the pin and start the fault timer. To prevent interference with the PWM dimming, the IC will only look at the NONFAULT pin during the period when the lamp current regulation loop is closed (when $V_{CSWP} = V_{CVFB}$).

When the IC detects an internal fault, see Section 8.14.2 to Section 8.14.8), it signals this via the NONFAULT pin by pulling the pin down (after the fault output delay time $t_{d(o)fault)}$). At this point the IC can no longer detect the external fault. However, by then the fault timer is already running.

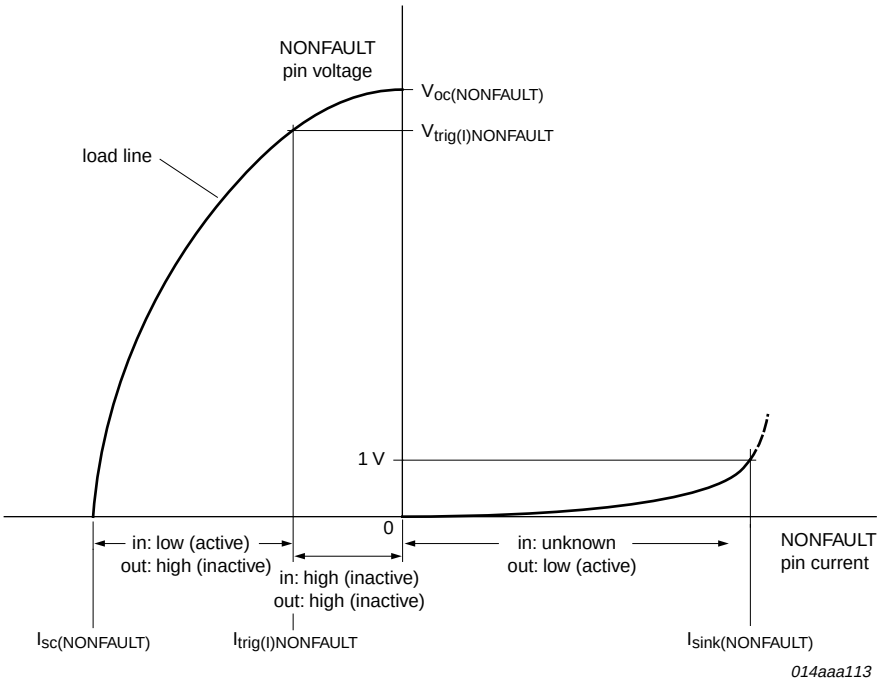


Fig 17. Input and output levels at the NONFAULT pin

The signal from the IC is a voltage signal and the signal to the IC is a current signal. In this way a driving conflict is prevented. Also, it leaves the possibility for the outside world to see the signal from the IC even while a fault condition is being signalled to the IC in the meantime, as illustrated in Figure 18.

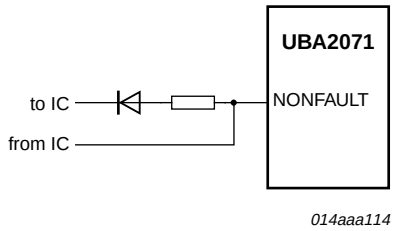


Fig 18. Splitting the NONFAULT pin signals to and from the IC

8.14.10 Fault input via the COMM pin

If a fault is signalled to the IC via the COMM pin this fault is treated identical to hard switching detected, see Section 8.14.3.

9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (SGND pin 10).

Symbol	Parameter	Conditions	Min	Max	Unit
General					
$R_{ref(IREF)}$	reference resistance on pin IREF		30	36	kΩ
SR	slew rate	on pins FS, GH, and SH	–4	+4	V/ns
T_{amb}	ambient temperature		–25	+100	°C
T_j	junction temperature		–25	+125	°C
T_{stg}	storage temperature		–55	+150	°C
Voltages					
V_{SH}	voltage on pin SH		-	550	V
V_{VDD}	voltage on pin VDD		-	14	V
V_{FS}	voltage on pin FS	continuous	0	+570	V
		t < 0.5 s	0	+630	V
		with respect to V_{SH}	–0.3	+14	V
V_{GL}	voltage on pin GL		–0.3	+14	V
V_{GH}	voltage on pin GH	with respect to V_{SH}	–0.3	+14	V
V_{PGND}	voltage on pin PGND		0.0	0.0	V
V_{VDD}	voltage on pin VDD		–0.3	+14	V
V_{COMM}	voltage on pin COMM		–0.3	+14	V
V_{EN}	voltage on pin EN		–0.3	+14	V
V_{PWMA}	voltage on pin PWMA		–0.1	+5	V
V_{PWMD}	voltage on pin PWMD		–0.1	+5	V

Table 4. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to signal ground (SGND pin 10).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{NONFAULT}$	voltage on pin NONFAULT		–0.1	+5	V
V_{VFB}	voltage on pin VFB	continuous	–0.1	+5	V
		t < 1 ms	–0.1	+9	V
V_{IFB}	voltage on pin IFB	continuous	–5	+5	V
		t < 1 ms	–9	+9	V
ESD					
V_{ESD}	electrostatic discharge voltage	human body model:			
		pins IFB, CIFB, VFB, CVFB, CSWP, IREF, CT, CF, CPWM, NONFAULT, COMM, PWMA, PWMD, EN, VDD, and GL	–2	+2	kV
		pins GH, FS, and SH	–1	+1	kV
		machine model:			
		all pins	–250	+250	V

10. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; SO24 package	80	K/W
		in free air; SSOP24 package	111	K/W

11. Characteristics

Table 6. Characteristics

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN} = V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together. GL, GH, COMM, NONFAULT and PWMD pins left open (unless otherwise specified). Currents are positive when flowing into the IC. Parameters valid for all types (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
High voltage						
I_{leak}	leakage current	V_{FS}, V_{GH}, and V_{SH} = 630 V; V_{VDD} = 0 V	-	-	2	µA
Start-up						
$V_{startup(VDD)}$	VDD start-up voltage	UBA2071T and UBA2071TS	11.7	12.1	12.5	V
		UBA2071AT and UBA2071ATS	10.5	10.9	11.3	V
$V_{stop(VDD)}$	stop voltage on pin VDD		9.8	10.1	10.4	V
$V_{hys(VDD)}$	hysteresis voltage on pin VDD	UBA2071T and UBA2071TS	1.8	2	2.2	V
		UBA2071AT and UBA2071ATS	0.6	0.8	1.0	V
$I_{startup(VDD)}$	start-up current on pin VDD	V_{VDD} = 11 V; EN pin grounded	0.13	0.16	0.19	mA

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN} = V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together. GL, GH, COMM, NONFAULT and PWMD pins left open (unless otherwise specified). Currents are positive when flowing into the IC. Parameters valid for all types (unless otherwise specified).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{clamp(VDD)}$	clamp voltage on pin VDD	EN pin grounded; I_{VDD} = 0.22 mA; UBA2071T and UBA2071TS		13	13.35	13.7	V
		EN pin grounded; I_{VDD} = 3 mA; UBA2071T and UBA2071TS		-	-	14.0	V
I_{VDD}	current on pin VDD	EN pin grounded; V_{VDD} = 14.0 V; UBA2071AT and UBA2071ATS		-	-	0.22	mA
Ignition							
$f_{sw(max)}/f_{sw(min)}$	maximum switching frequency to minimum switching frequency ratio			2.2	2.4	2.6	kHz
$V_{CVFB(max)}$	maximum voltage on pin CVFB			-	2.5	-	V
$I_{ch(CVFB)}$	charge current on pin CVFB	V_{VFB} = 2 V; $V_{CVFB(max)}$ = 2 V		–24	–21	–18	µA
$V_{th(lod)(IFB)}$	lamp on detection threshold voltage on pin IFB			0.9	1.05	1.2	V
Normal operation							
I_{VDD}	current on pin VDD	oscillating at $f_{sw(min)}$; C_{CF} = 100 pF		1.2	1.5	1.8	mA
		disabled; V_{VDD} = 11 V		-	0.16	-	mA
		oscillating; CF = 100 pF; GL and GH open		-	1.5	-	mA
$f_{sw(min)}$	minimum switching frequency	C_{CF} = 100 pF	[1][2]	10	-	100	kHz
			[1][2]	38	40	42	kHz
$V_{ref(creg)}$	current regulation reference voltage			1.20	1.26	1.32	V
$V_{IFB(min)}$	minimum voltage on pin IFB	for linear operating range		-	–2.5	-	V
$V_{IFB(max)}$	maximum voltage on pin IFB	for linear operating range		-	2.5	-	V
$R_{i(IFB)}$	input resistance on pin IFB	V_{IFB} = 1 V		-	45	-	kΩ
		V_{IFB} = –1 V		-	24	-	kΩ
$g_{m(OTA)}$	OTA transconductance			14	16.5	19	µA/V
Drivers							
$I_{source(drv)}$	driver source current	V_{GL}, V_{GH} = 4 V; V_{VDD} = V_{FS} = 12 V		–105	–90	–75	mA
$R_{sink(drv)}$	driver sink resistance	V_{GL}, V_{GH} = 2 V; V_{VDD} = V_{FS} = 12 V		13.5	16.0	18.5	Ω
t_{no}	non-overlap time			1.1	1.3	1.5	µs
$V_{Fd(bs)}$	bootstrap diode forward voltage	I_{FS} = 5 mA		1.0	1.5	2.0	V
PWM dimming							
I_{VDD}	current on pin VDD	C_{CF} = 100 pF; V_{PWMD} = H; V_{CSWP} = 0 V		1.0	1.2	1.4	mA
$t_{d(en)PWM}$	PWM enable delay time			3	4	5	ms

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN} = V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together. GL, GH, COMM, NONFAULT and PWMD pins left open (unless otherwise specified). Currents are positive when flowing into the IC. Parameters valid for all types (unless otherwise specified).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PWM}	PWM frequency		[1]	75	-	1000	Hz
		C_{CPWM} = 33 nF		306	324	342	Hz
$I_{ch(CSWP)}$	charge current on pin CSWP	PWMD low; V_{CSWP} = 1 V		–23	–20	–17	µA
$I_{dch(CSWP)}$	discharge current on pin CSWP	PWMD high; V_{CSWP} = 1 V		17	20	23	µA
$R_{i(PWMA)}$	input resistance on pin PWMA			80	100	120	kΩ
$V_{i(PWMA)}$	input voltage on pin PWMA	for minimum PWM duty cycle		-	1.24	-	V
		for maximum PWM duty cycle		-	3	-	V
$\delta_{PWM(min)}$	minimum PWM duty cycle		[3]	-	12	-	%
		CPWM pin connected to SGND	[3]	-	0	-	%
$\delta_{PWM(max)}$	maximum PWM duty cycle		[3]	-	100	-	%
δ_{PWMD}	duty cycle on pin PWMD		[3]	12	-	100	%
$I_{source(PWMD)}$	source current on pin PWMD	V_{PWMD} = 3 V		-	0.6	-	mA
$I_{sink(PWMD)}$	sink current on pin PWMD	V_{PWMD} = 1 V		-	1.2	-	mA
$V_{th(H)(PWMD)}$	HIGH-level threshold voltage on pin PWMD			-	-	1.7	V
$V_{th(L)(PWMD)}$	LOW-level threshold voltage on pin PWMD			0.85	-	-	V
Communication (COMM pin)							
$V_{L(clk)(COMM)}$	clock LOW-level voltage on pin COMM	I_{COMM} = 10 µA		0	0.1	0.2	V
$I_{L(clk)(COMM)}$	clock LOW-level current on pin COMM	V_{COMM} = 1.5 V		-	5.0	-	mA
$V_{H(clk)(COMM)}$	clock HIGH-level voltage on pin COMM	I_{COMM} = –10 µA		4	4.3	4.6	V
$I_{H(clk)(COMM)}$	clock HIGH-level current on pin COMM	V_{COMM} = 2.5 V		-	–4.5	-	mA
$V_{O(hbswoff)(COMM)}$	half bridge switch-off output voltage on pin COMM	PWMD = 5 V		-	12	-	V
$I_{th(det)hsw(COMM)}$	hard switching detection threshold current on pin COMM	Clock = high; PWMD = low		–120	–100	–80	µA
Protections							
$V_{th(osp)(VFB)}$	open/short protection threshold voltage on pin VFB			50	100	150	mV
$V_{th(ov)(VFB)}$	overvoltage threshold voltage on pin VFB			2.40	2.50	2.60	V
$R_{i(VFB)}$	input resistance on pin VFB			500	670	840	kΩ
$I_{dch(CVFB)}$	discharge current on pin CVFB	$V_{VFB} < V_{th(osp)(VFB)}$ or $V_{VFB} > V_{th(ov)(VFB)}$; V_{CVFB} = 2 V		17	20	23	µA
$V_{th(ovextra)(VFB)}$	overvoltage extra threshold voltage on pin VFB			2.9	3.0	3.1	V

Table 6. Characteristics *...continued*

T_{amb} = 25 °C; V_{VDD} = 12 V; R_{IREF} = 33 kΩ; V_{EN} = V_{VDD} and CPWM connected to a capacitor, unless otherwise specified. All voltages are measured with respect to signal ground (SGND, pin 10). SGND and PGND connected together. GL, GH, COMM, NONFAULT and PWMD pins left open (unless otherwise specified). Currents are positive when flowing into the IC. Parameters valid for all types (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th(osp)(IFB)}$	open/short protection threshold voltage on pin IFB		200	250	300	mV
$V_{th(ocd)(IFB)}$	overcurrent detection threshold voltage on pin IFB		2.65	3.0	3.3	V
$V_{th(hsw)(SH)}$	hard switching threshold voltage on pin SH		-	56	-	V
$I_{dch(CVFB)}$	discharge current on pin CVFB	hard switching detected; V_{CVFB} = 2 V	36	41	46	µA
$V_{th(det)arc(IFB)}$	arc detection threshold voltage on pin IFB		-	5	-	V
$t_{spike(min)}$	minimum spike time	to active arcing protection	-	200	-	ns
$t_{d(o)fault}$	fault output delay time	C_{CT} = 100 nF	0.063	0.069	0.075	s
$t_{to(fault)}$	fault time-out time	C_{CT} = 100 nF	0.85	1.00	1.15	s
$V_{oc(NONFAULT)}$	open-circuit voltage on pin NONFAULT		4.7	5.0	5.3	V
$V_{trig(I)NONFAULT}$	input trigger voltage on pin NONFAULT		3.8	4.3	4.8	V
$I_{trig(I)NONFAULT}$	input trigger current on pin NONFAULT		–32	–27	–22	µA
$I_{NONFAULT}$	current on pin NONFAULT	$V_{NONFAULT}$ = 3 V	–230	–195	–160	µA
$I_{sc(NONFAULT)}$	short circuit current on pin NONFAULT	$V_{NONFAULT}$ = 0 V	–260	–220	–180	µA
$I_{sink(NONFAULT)}$	sink current on pin NONFAULT	$V_{NONFAULT}$ = 1 V	0.7	1	1.3	mA
Enable (EN pin)						
$V_{th(H)2(EN)}$	HIGH-level threshold voltage 2 on pin EN		2.65	2.76	2.87	V
$V_{th(H)1(EN)}$	HIGH-level threshold voltage 1 on pin EN		-	-	1.7	V
$V_{th(L)(EN)}$	LOW-level threshold voltage on pin EN		0.9	-		V
$I_{bias(EN)}$	bias current on pin EN			5		µA

[1] Given frequency is switching frequency of GL and GH. Sawtooth frequency on CF pin is twice as high.

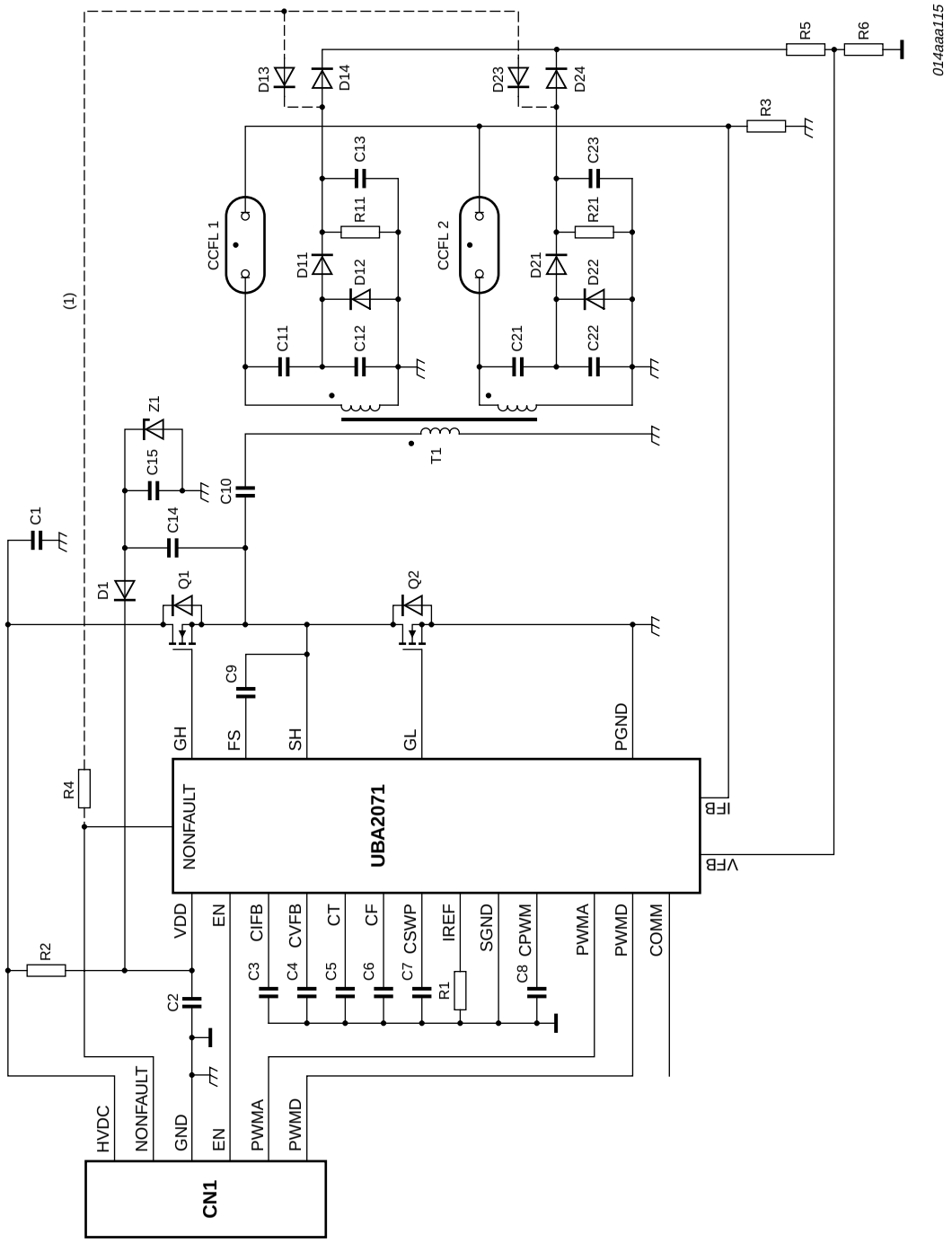
[2] Can be set by external capacitor

[3] PWMD is active low: A low level on the PWMD pin corresponds with lamps-on. Example: δ_{PWM} = 20 % means PWMD is low during 20 % of each cycle and the lamps are on 20 % of the time, resulting in a light output of 20 %.

12. Application information

Figure 19 shows an example backlighting configuration, where the inverter is supplied from a high voltage DC source and the IC is supplied by means of a $\Delta V/\Delta t$ supply (C14, C15, Z1 and D1). Two lamps are connected, each to the output of its own transformer. The leakage inductance of this transformer provides the ballast impedance for the lamps. An analog voltage is converted to a PWM signal to provide for the desired brightness level. Lamp short detection is done via the lamp voltage sensing, D13 and D23, and the NONFAULT pin.

Figure 20 shows an example of a balanced application using one UBA2071 and one UBA2073.



(1) Optional lamp short protection is available via the NONFAULT pin.

Fig 19. Example of single IC backlighting application

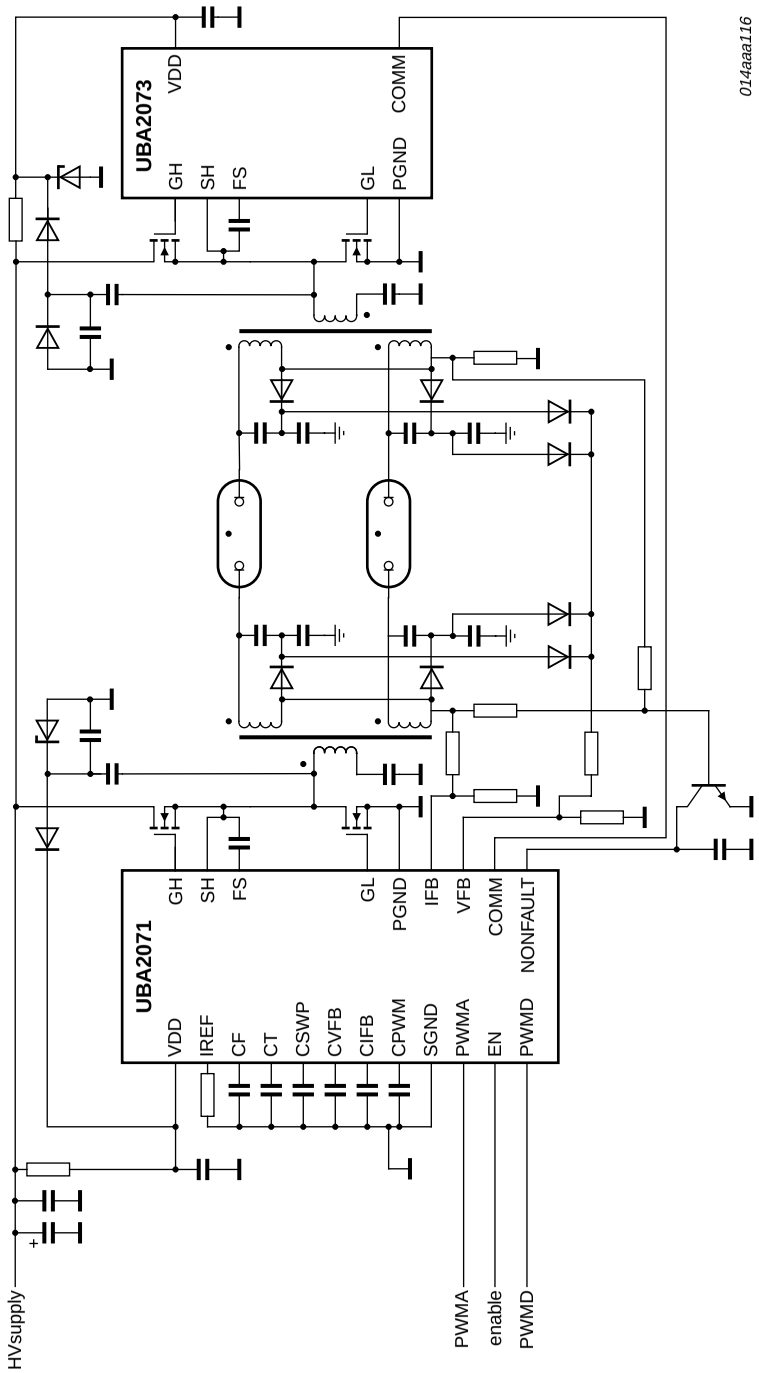
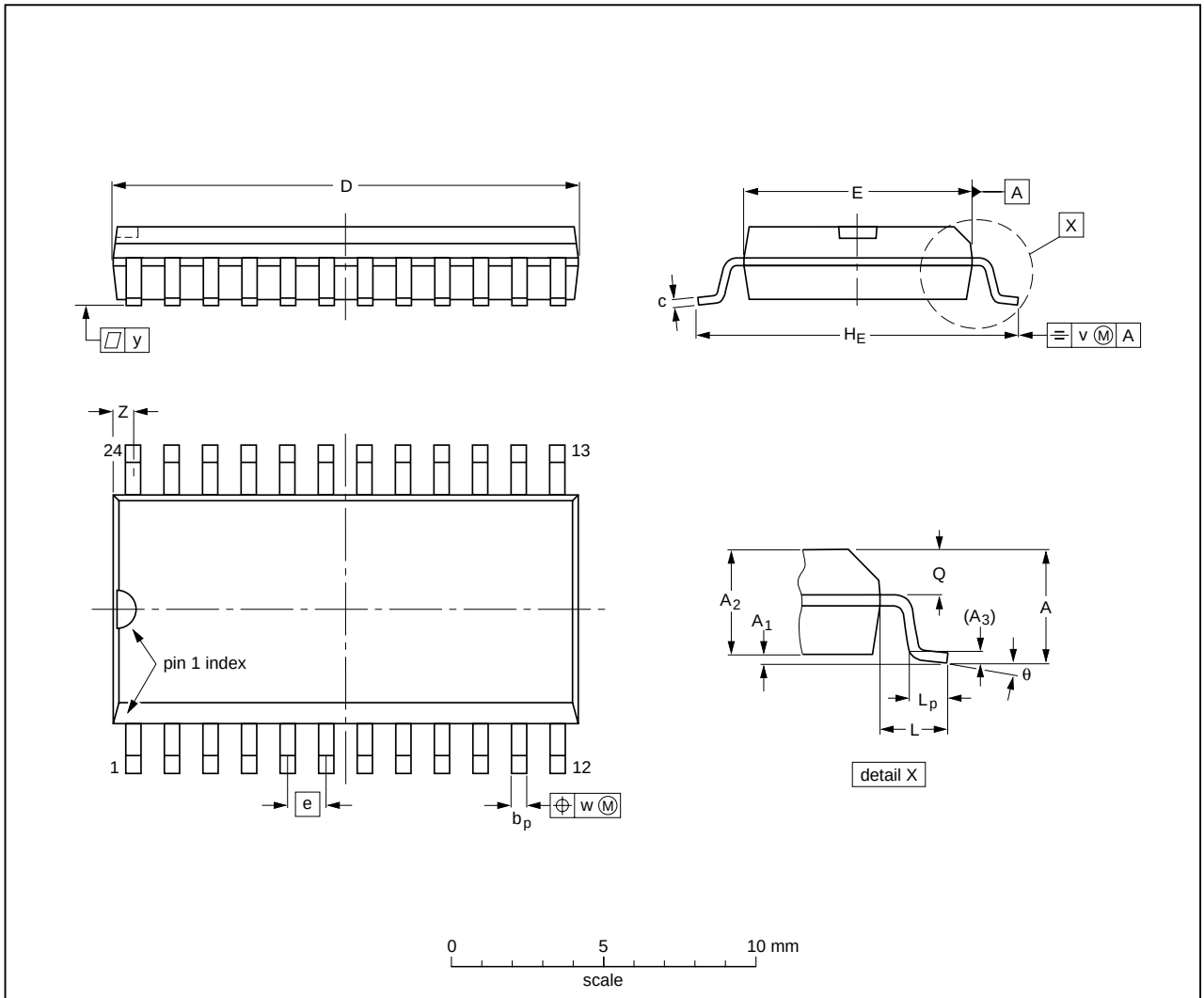


Fig 20. Example of balanced backlighting application

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

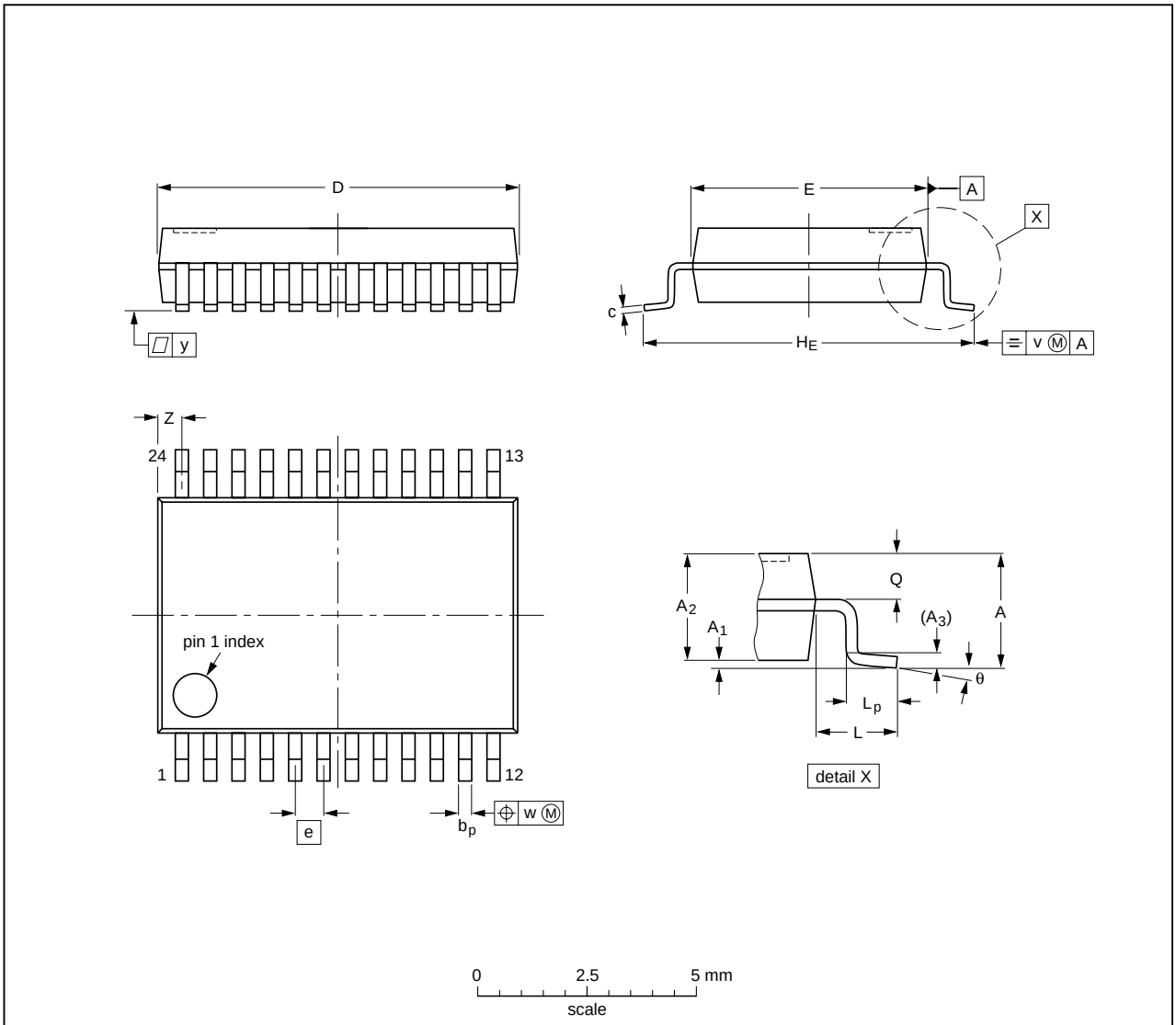
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 21. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 22. Package outline SOT340 (SSOP24)

14. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
UBA2071_A_1	20080623	Product data sheet	-	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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