TJA1448

Dual high-speed CAN transceiver with Standby mode

Rev. 2 — 15 October 2021 Product data sheet

1 General description

The TJA1448 is a member of the TJA144x family of transceivers that provide an interface between a Controller Area Network (CAN) or CAN FD (Flexible Data rate) protocol controller and the physical two-wire CAN bus. TJA144x transceivers implement the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5, and are fully interoperable with high-speed Classical CAN and CAN FD transceivers. All TJA144x variants enable reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

The TJA1448 is intended as a simple replacement for dual high-speed Classical CAN and CAN FD transceivers, such as the TJA1059 from NXP. It offers pin compatibility and is designed to avoid changes to hardware and software design, allowing the TJA1448 to be easily retrofitted to existing applications.

An AEC-Q100 Grade 0 variant, the TJR1448, is available for high temperature applications, supporting operation at 150 °C ambient temperature.

1.1 TJA1448 variants

The TJA1448 comes in three variants. The TJA1448A and TJA1448B are available in SO14 and HVSON14 packages. The TJA1448C comes in a HVSON14 package:

- The TJA1448A is a dual high-speed CAN transceiver with Normal and Standby modes and a VIO supply pin. The VIO pin allows for direct interfacing with 3.3 V and 5 V-supplied microcontrollers.
- The TJA1448B is a high-speed CAN transceiver with Normal and Standby modes.
- The TJA1448C is a dual high-speed CAN transceiver with Normal and Standby modes, a VIO supply pin and RXD latching. The VIO pin allows for direct interfacing with 3.3 V and 5 V-supplied microcontrollers.

2 Features and benefits

2.1 General

- ISO 11898-2:2016, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant
- Standard CAN and CAN FD data bit rates up to 5 Mbit/s
- Low Electromagnetic Emission (EME) and high Electromagnetic Immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- TJA1448A/C only: VIO input for interfacing with 3.3 V to 5 V microcontrollers
- Fully independent control of two transceivers combined monolithically in a single package
- All variants are available in a leadless HVSON14 (3.0 mm x 4.5 mm) package with improved Automated Optical Inspection (AOI) capability; TJA1448A/B available in an SO14 package.

- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Predictable and fail-safe behavior

- Undervoltage detection with defined handling on all supply pins
- Full functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Defined behavior below the undervoltage detection thresholds
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the Off mode threshold
- Internal biasing of TXD and mode selection input pins, to enable defined fail-safe behavior

2.3 Low-power management

- Very low-current Standby mode with host and bus wake-up capability
- TJA1448A/C only: CAN wake-up receiver powered by V_{IO} allowing V_{CC} to be shut down
- CAN wake-up pattern filter time of 0.5 µs to 1.8 µs meeting Classical CAN and CAN FD requirements
- TJA1448C variant offers RXD wake-up latching to enable wake-up source readout in gateway applications

2.4 Protection

- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Thermally protected

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Normal mode				
		both channels recessive	-	8	14	mA
		one channel dominant	-	42	67	mA
		both channels dominant	-	77	120	mA
		both channels in Standby mode				
		TJA1448A/C	-	-	2	µA
		TJA1448B	-	11	18	µA
$V_{uvd(stb)(VCC)}$	standby undervoltage detection voltage on pin VCC		4	-	4.5	V
$V_{uvhys(stb)(VCC)}$	standby undervoltage hysteresis voltage on pin VCC		50	-	-	mV
$V_{uvd(swoff)(VCC)}$	switch-off undervoltage detection voltage on pin VCC	TJA1448B	2.65	-	2.95	V
V_{IO}	supply voltage on pin VIO		2.95	-	5.5	V
I_{IO}	supply current on pin VIO	Normal mode				
		both channels recessive	-	270	750	µA
		one channel dominant	-	360	1000	µA
		both channels dominant	-	450	1250	µA
		both channels in Standby mode	-	11	16	µA
$V_{uvd(swoff)(VIO)}$	switch-off undervoltage detection voltage on pin VIO		2.65	-	2.95	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANHx and CANLx	-8	-	+8	kV
V_{CANH}	voltage on pin CANH	pins CANH1 and CANH2; limiting value according to IEC 60134	-36	-	+40	V
V_{CANL}	voltage on pin CANL	pins CANL1 and CANL2; limiting value according to IEC 60134	-36	-	+40	V
T_{vj}	virtual junction temperature		-40	-	+150	°C

4 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1448AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1448BT			
TJA1448ATK	HVSON14	plastic thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2
TJA1448BTK			
TJA1448CTK			

Table 3. TJA1448 feature overview

See Section 19 for a feature overview of the complete TJx144x/TJx146x/TJF1441 family.

	Modes					Supplies			Data rate		Additional features					
Device[1]	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD	Signal improvement[2]	Wake-up source recognition[3]	Short WUP support [0.5 - 1.8 µs][4]	Single supply pin wake-up[5]	TXD dominant timeout	Local diagnostics via ERR_N pin
TJA1448A	●	●				●	●		●				●	●	●	
TJA1448B	●	●				●			●				●		●	
TJA1448C	●	●				●	●		●			●	●	●	●	

[1] TJA1448 is AEC-Q100 Grade 1.
[2] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.
[3] RXD is held LOW after wake-up request, enabling wake-up source recognition.
[4] WUP = wake-up pattern according ISO11898-2:2016.
[5] Only VIO supply needed for wake-up.

5 Block diagrams

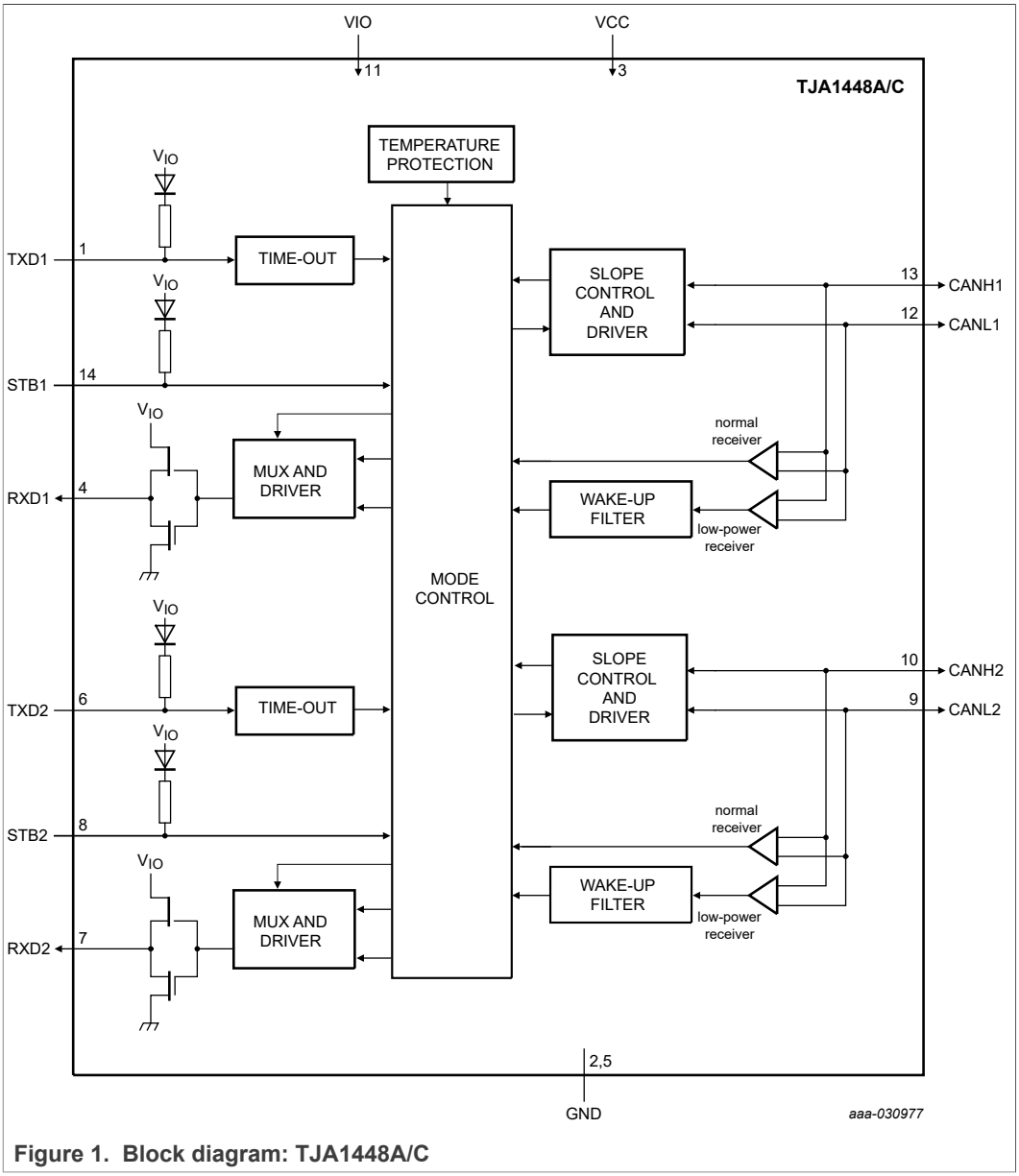


Figure 1. Block diagram: TJA1448A/C

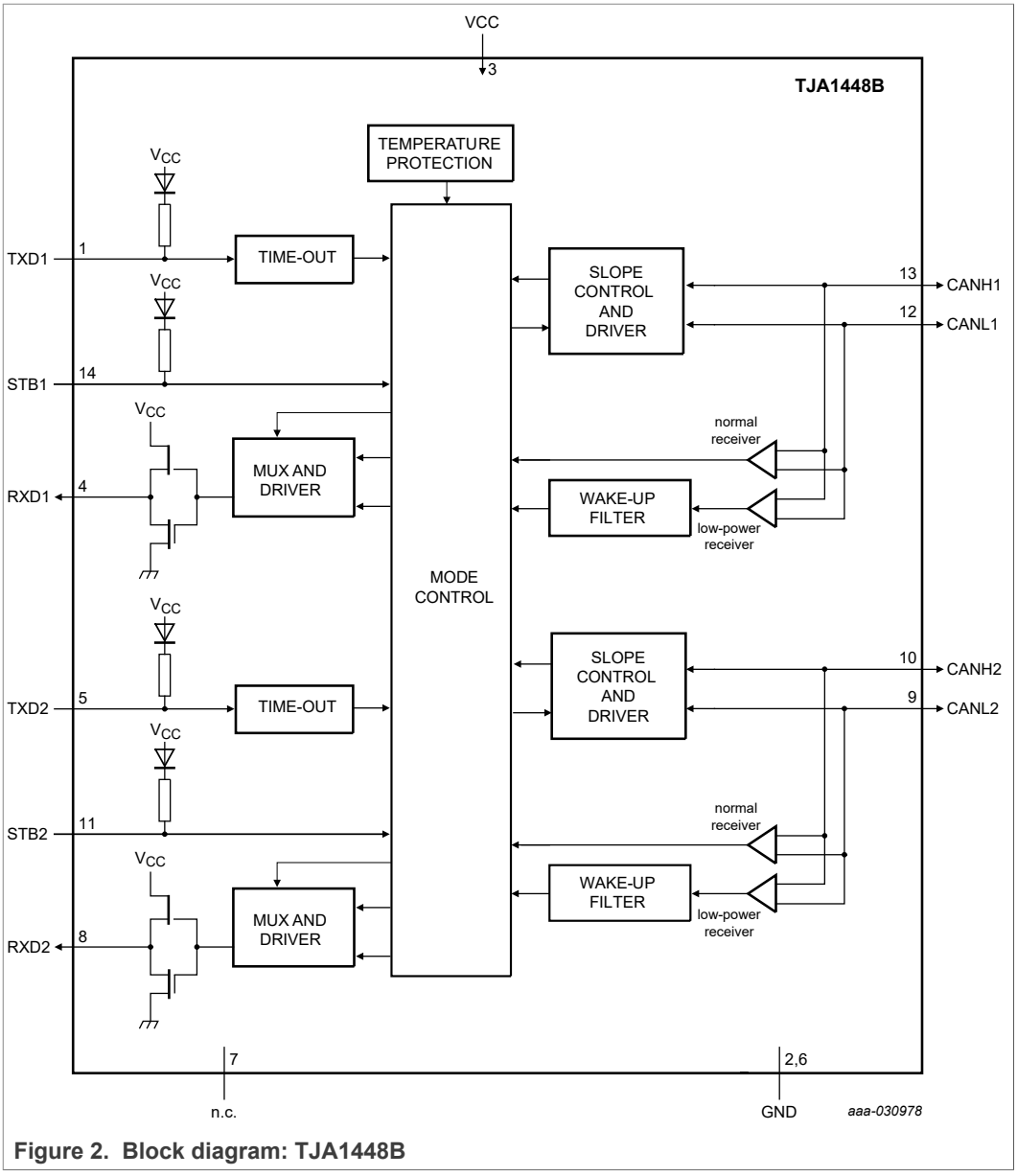
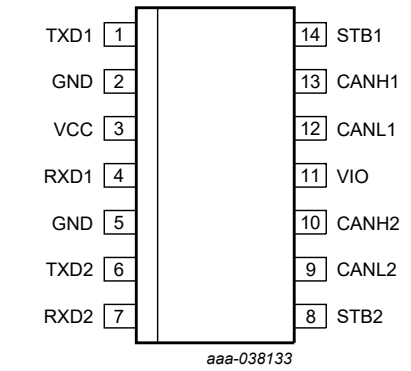


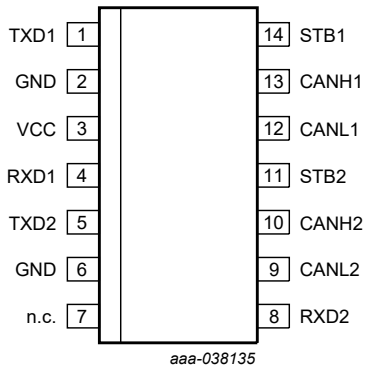
Figure 2. Block diagram: TJA1448B

6 Pinning information

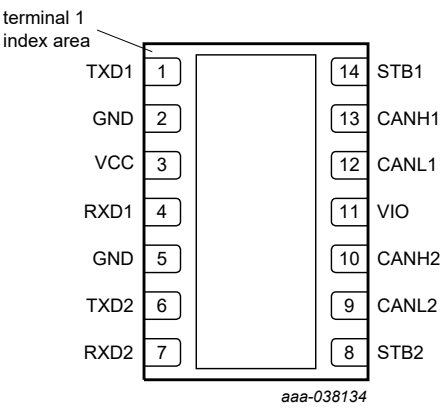
6.1 Pinning



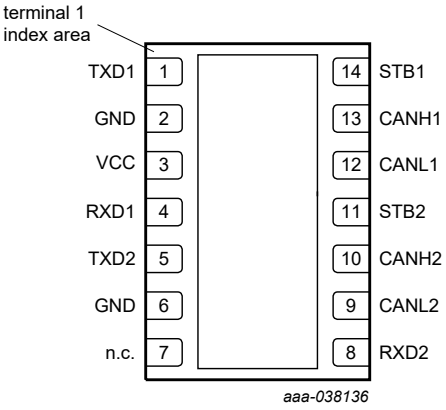
TJA1448AT: SO14



TJA1448BT: SO14



TJA1448ATK/CTK: HVSON14



TJA1448BTK: HVSON14

Figure 3. Pin configuration diagrams

6.2 Pin description

Table 4. Pin description: TJA1448A/C

Symbol	Pin	Type[1]	Description
TXD1	1	I	transmit data input 1; inputs data (from the CAN controller) to be written to CANH1/CANL1 bus lines
GND[2]	2	G	ground
VCC	3	P	5 V supply voltage input
RXD1	4	O	receive data output 1; outputs data read from bus lines CANH1/CANL1 (to the CAN controller)
GND[2]	5	G	ground
TXD2	6	I	transmit data input 2; inputs data (from the CAN controller) to be written to CANH1/CANL1 bus lines
RXD2	7	O	receive data output 2; outputs data read from bus lines CANH2/CANL2 (to the CAN controller)
STB2	8	I	Standby mode control input 2 (HIGH: Standby mode; LOW: Normal mode)
CANL2	9	AIO	LOW-level CAN bus line 2
CANH2	10	AIO	HIGH-level CAN bus line 2
VIO	11	P	supply voltage input for I/O level adapter
CANL1	12	AIO	LOW-level CAN bus line 1
CANH1	13	AIO	HIGH-level CAN bus line 1
STB1	14	I	Standby mode control input 1 (HIGH: Standby mode; LOW: Normal mode)

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.
[2] HVSON package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

Table 5. Pin description: TJA1448B

Symbol	Pin	Type[1]	Description
TXD1	1	I	transmit data input 1; inputs data (from the CAN controller) to be written to CANH1/CANL1 bus lines
GND[2]	2	G	ground
VCC	3	P	5 V supply voltage input
RXD1	4	O	receive data output 1; outputs data read from bus lines CANH1/CANL1 (to the CAN controller)
TXD2	5	I	transmit data input 2; inputs data (from the CAN controller) to be written to CANH2/CANL2 bus lines
GND[2]	6	G	ground
n.c.	7	-	not connected
RXD2	8	O	receive data output 2; outputs data read from bus lines CANH2/CANL2 (to the CAN controller)
CANL2	9	AIO	LOW-level CAN bus line 2
CANH2	10	AIO	HIGH-level CAN bus line 2
STB2	11	I	Standby mode control input 2 (HIGH: Standby mode; LOW: Normal mode)
CANL1	12	AIO	LOW-level CAN bus line 1
CANH1	13	AIO	HIGH-level CAN bus line 1
STB1	14	I	Standby mode control input 1 (HIGH: Standby mode; LOW: Normal mode)

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.
[2] HVSON package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

7 Functional description

7.1 Operating modes

The TJA1448 supports three operating modes per transceiver, Normal, Standby and Off. The operating mode is selected independently for each transceiver via pins STB1 and STB2. See Table 6 for a description of the operating modes under normal supply conditions. Mode changes are completed after transition time $t_{t(moch)}$.

Table 6. Operating modes

Mode	Inputs		Outputs	
	Pin STB1/STB2	Pin TXD1/TXD2	CAN1/CAN2 driver	Pin RXD1/RXD2
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	X	biased to ground	TJA1448A/B: follows BUS when wake-up detected TJA1448C: LOW when wake-up detected
				HIGH when no wake-up detected
Off[1]	X	X	high-ohmic state	high-ohmic state

[1] Off mode is entered when the voltage on pin VIO (TJA1448A/C) or pin VCC (TJA1448B) is below the switch-off undervoltage detection threshold.

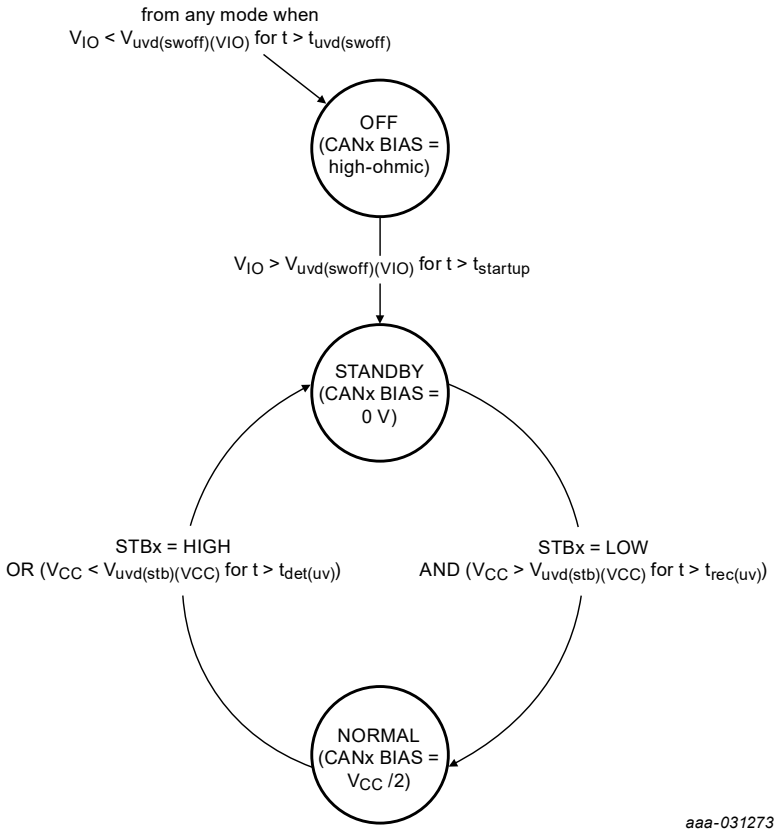


Figure 4. TJA1448A/C state diagram (per channel)

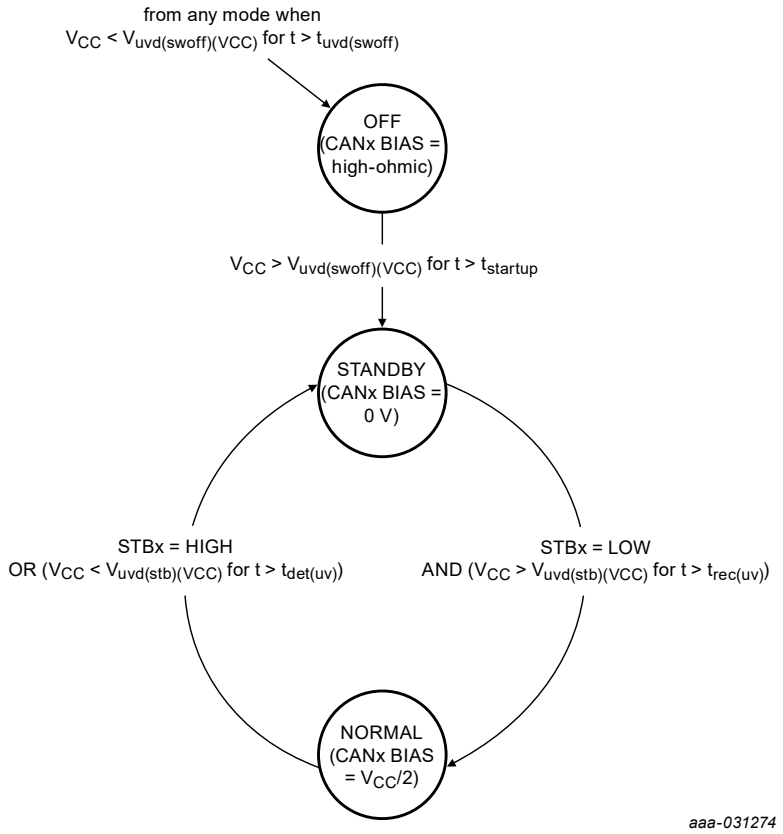


Figure 5. TJA1448B state diagram (per channel)

7.1.1 Off mode

The TJA1448 switches to Off mode from any mode when the supply voltage (on pin VIO in TJA1448A/C and VCC in TJA1448B) falls below the switch-off undervoltage threshold ($V_{uvd(swoff)(VCC)}$ or $V_{uvd(swoff)(VIO)}$). This is the default mode when the supply is first connected.

In Off mode, the CAN pins and RXDx pins are in a high-ohmic state.

7.1.2 Standby mode

When the supply voltage (V_{IO} for TJA1448A/C or V_{CC} for TJA1448B) rises above the switch-off undervoltage detection threshold, the TJA1448 starts to boot up, triggering an initialization procedure. The TJA1448 switches to the selected mode after $t_{startup}$.

Standby mode is selected when pin STBx goes HIGH. In this mode, the transceiver is unable to transmit or receive data and a low-power receiver is activated to monitor the bus for a wake-up pattern. The transmitter and Normal-mode receiver blocks are switched off and the bus pins are biased to ground to minimize system supply current. Pin RXDx in the TJA1448A/B follows the bus after a wake-up request has been detected. In the TJA1448C, RXDx is forced LOW when a wake-up request is detected.

A transition to Normal mode is triggered when STBx is forced LOW (provided V_{CC} > $V_{uvd(stb)(VCC)}$ and V_{IO} > $V_{uvd(swoff)(VIO)}$ in the TJA1448A/C).

If V_{CC} is below $V_{uvd(stb)(VCC)}$ when STBx goes LOW (with $V_{IO} > V_{uvd(swoff)(VIO)}$ in TJA1448A/C and $V_{CC} > V_{uvd(swoff)(VCC)}$ in TJA1448B), the TJA1448 will remain in Standby mode. Pending wake-up events will be cleared and differential data on the bus pins converted to digital data via the low-power receiver and output on pin RXDx.

In the TJA1448A/C, the low-power receiver is supplied from V_{IO} and can detect CAN bus activity when V_{IO} is above $V_{uvd(swoff)(VIO)}$ (even if V_{IO} is the only available supply voltage).

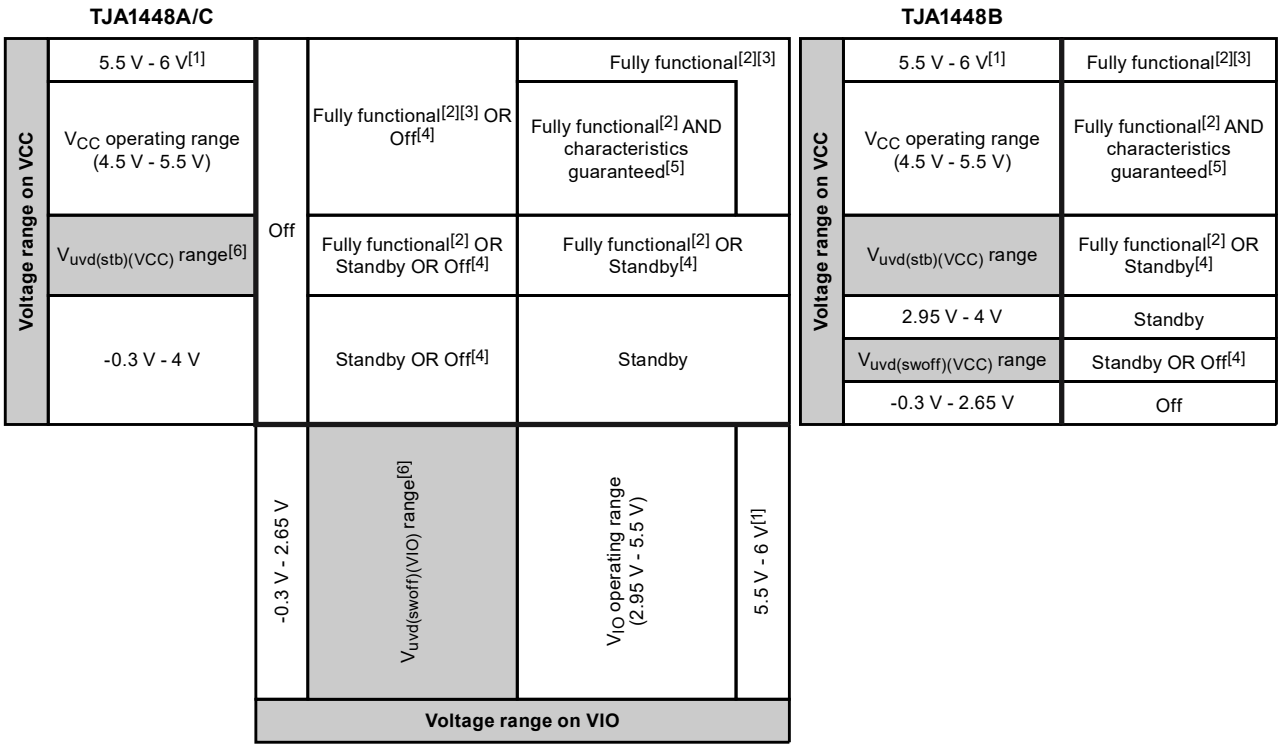
7.1.3 Normal mode

A LOW level on pin STBx selects Normal mode, provided the supply voltage on pin VCC is above the standby undervoltage detection threshold, $V_{uvd(stb)(VCC)}$.

In this mode, the transceiver can transmit and receive data via bus lines CANHx and CANLx. Pin TXDx must be HIGH at least once in Normal Mode before transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXDx. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

7.1.4 Operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in Figure 6 and in the state diagrams (Figure 4 and Figure 5).



[1] 6 V is the IEC 60134 Absolute Maximum Rating (AMR) for VCC and VIO (see Limiting values table). Above the AMR, irreversible changes in characteristics, functionality or performance may occur. Returning from above AMR to the operating range, datasheet characteristics and functionality cannot be guaranteed.
[2] Target transceiver functionality as described in this datasheet is applicable.
[3] Prolonged operation of the device outside the operating range may impact reliability over lifetime. Returning to the operating range, datasheet characteristics are guaranteed provided the AMR has not been exceeded.
[4] For a given value of V_{CC} (and V_{IO} in TJA1448A/C), a specific device will be in a single defined state determined by its undervoltage detection thresholds ($V_{uvd(stb)(VCC)}$, $V_{uvd(swoff)(VIO)}$ and $V_{uvd(swoff)(VCC)}$). The actual thresholds can vary between devices (within the ranges specified in this data sheet). To guarantee the device will be in a specific state, V_{IO} and V_{CC} must be either above the maximum or below the minimum thresholds specified for these undervoltage detection ranges.
[5] Datasheet characteristics are guaranteed within the V_{CC} and V_{IO} operating ranges. Exceptions are described in the Static and Dynamic characteristics tables.
[6] The following applies to TJA1448A/C:
- If both V_{CC} and V_{IO} are above the undervoltage threshold, the device is fully functional.
- If V_{CC} is below and V_{IO} above the undervoltage threshold, the device is in Standby mode.
- If V_{IO} is below the undervoltage threshold, the device is in Off mode, regardless of V_{CC}.

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Figure 6. TJA1448 supply voltage ranges and gap-free operation

7.2 Remote wake-up (via the CAN bus)

In Standby mode, the TJA1448 wakes up when a dedicated wake-up pattern (specified in ISO 11898-2: 2016) is detected on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{wake(busdom)}$ and $t_{wake(busrec)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 7 for TJA1448A/B wake-up timing

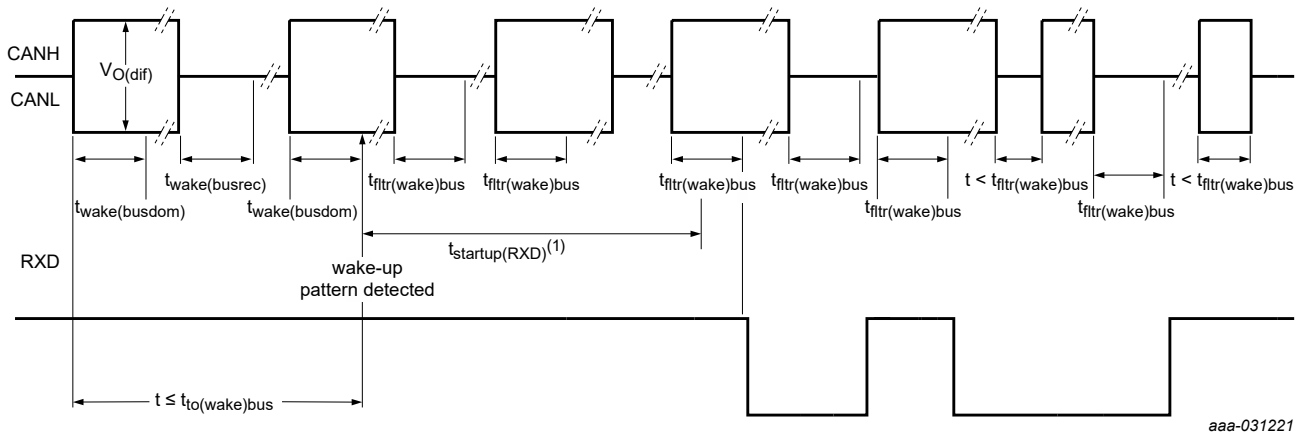
and Figure 8 for TJA1448C wake-up timing). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event. Pin RXDx remains HIGH until the wake-up event has been triggered.

After a wake-up sequence has been detected, the TJA1448A/B remains in Standby mode with the bus signals reflected on RXDx after $t_{startup(RXD)}$. Note that dominant or recessive phases lasting less than $t_{fltr(wake)bus}$ will not be detected by the low-power differential receiver and will not be reflected on RXDx in Standby mode (see Figure 7).

The TJA1448C also remains in Standby mode after a wake-up sequence has been detected, but pin RXDx switches LOW after $t_{startup(RXD)}$ (see Figure 8).

A wake-up event is not flagged on RXDx if any of the following events occurs while a valid wake-up pattern is being received:

- The device switches to Normal mode
- The complete wake-up pattern was not received within $t_{to(wake)bus}$
- A V_{CC} or V_{IO} switch-off undervoltage is detected ($V_{CC} < V_{uvd(swoff)(VCC)}$ or $V_{IO} < V_{uvd(swoff)(VIO)}$; see Section 7.3.3)



(1) During $t_{startup(RXD)}$, the low-power receiver is on but pin RXDx is not active (i.e. HIGH/recessive). The first dominant pulse of width ≥ $t_{fltr(wake)bus}$ that ends after $t_{startup(RXD)}$ will trigger RXDx to go LOW/dominant.

Figure 7. TJA1448A/B wake-up timing

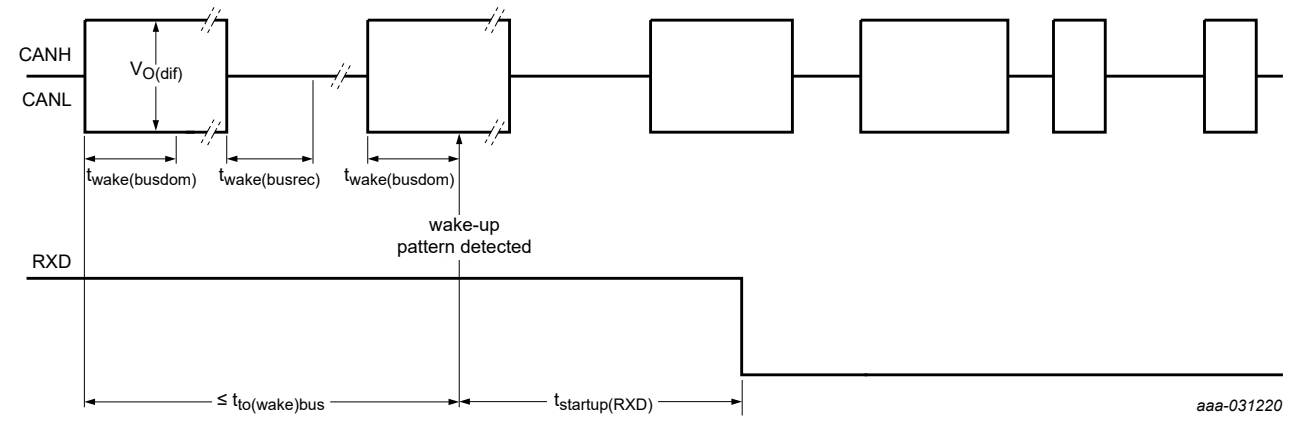


Figure 8. TJA1448C wake-up timing

7.3 Fail-safe features

7.3.1 TXD dominant timeout function

A hardware and/or software application failure in Normal mode that caused pin TXDx to be held LOW would drive the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out function prevents such a network lock-up. A 'TXD dominant timeout' timer is started when pin TXDx goes LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. The TXD dominant time-out timer is reset when pin TXDx is set HIGH.

7.3.2 Internal biasing of TXDx and STBx input pins

Pins TXDx and STBx have internal pull-ups to V_{CC}/V_{IO} to ensure a safe, defined state in case one, or both, of these pins is left or becomes floating. Pull-up resistors are active on these pins in all states; they should be held at the V_{CC}/V_{IO} level in Standby mode to minimize supply current.

7.3.3 Undervoltage detection on pins VCC and VIO

If V_{CC} drops below the standby undervoltage detection threshold ($V_{uvd(stb)(VCC)}$) for $t_{det(uv)}$, both transceivers switch to Standby mode. The logic state of pin STBx is ignored until V_{CC} has recovered.

In the TJA1448A/C, if V_{IO} drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)(VIO)}$) for $t_{uvd(swoff)}$, both transceiver switch to Off mode and disengage from the bus (high-ohmic) until V_{IO} has recovered.

In the TJA1448B, if V_{CC} drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)(VCC)}$) for $t_{uvd(swoff)}$, both transceivers switch to Off mode and disengage from the bus (high-ohmic) until V_{CC} has recovered.

7.3.4 Overtemperature protection

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the CAN bus drivers are disabled. When the junction temperature drops below $T_{j(sd)rel}$, the CAN bus drivers recover once TXDx has been reset to HIGH and Normal mode is selected (waiting for TXDx to go HIGH prevents output driver oscillation due to small variations in temperature).

7.3.5 I/O levels

Pin VIO on the TJA1448A/C should be connected to the same supply voltage used to supply the microcontroller (see Figure 1). This adjusts the signal levels on pins TXDx, RXDx and STBx to the I/O levels of the microcontroller, allowing for direct interfacing without additional glue logic. Pin VIO also provides the internal supply voltage for the low-power differential receiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC.

All I/O levels are related to V_{CC} in the TJA1448B and are, therefore, compatible with 5 V microcontrollers. Spurious signals from the microcontroller on pins STB1 and STB2 are filtered out with a filter time of $t_{filtr(IO)}$.

8 Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	pins VCC, VIO (TJA1448A), TXDx, STBx	-0.3	+6	V
			-	+7[2]	V
		pins CANHx, CANLx	-36	+40	V
		pin RXDx			
		TJA1448A/C	-0.3	V_{IO}+0.3[3]	V
		TJA1448B	-0.3	V_{CC}+0.3[3]	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL	between pins CANH1 and CANL1 and between CANH2 and CANL2	-40	+40	V
V_{trt}	transient voltage	on pins CANHx, CANLx [4]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [5]			
		on pins CANHx, CANLx	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [6]	-4	+4	kV
		on pins CANHx, CANLx [7]	-8	+8	kV
		Charged Device Model (CDM) [8]			
		on corner pins	-750	+750	V
		on any other pin	-500	+500	V
T_{vj}	virtual junction temperature	[9]	-40	+150	°C
T_{stg}	storage temperature	[10]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.
[3] Subject to the qualifications detailed in Table notes 1 and 2 above for pins VCC, VIO, TXDx and STBx.
[4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637.
[5] Verified by an external test house according to IEC TS 62228, Section 4.3.
[6] According to AEC-Q100-002.
[7] Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 1 and Figure 2). HBM pulse as specified in AEC-Q100-002 used.
[8] According to AEC-Q100-011.
[9] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[10] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 8. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO14	62	K/W
		HVSON14	42	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]	HVSON14	10	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	SO14	8	K/W
		HVSON14	4	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).

[2] Case temperature refers to the center of the heatsink at the bottom of the package.

10 Static characteristics

Table 9. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1448A/C); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(stb)}$	standby undervoltage detection voltage	[2]	4	-	4.5	V
$V_{uvhys(stb)}$	standby undervoltage hysteresis voltage		50	-	-	mV
$V_{uvd(swoff)}$	switch-off undervoltage detection voltage	TJA1448B [2]	2.65	-	2.95	V
I_{CC}	supply current	Normal mode				
		both channels recessive; $V_{TXDx} = V_{IO}$[3]	-	8	14	mA
		one channel dominant; one channel recessive; $t < t_{to(dom)TXD}$	-	42	67	mA
		both channels dominant; V_{TXDx} = 0 V; $t < t_{to(dom)TXD}$	-	77	120	mA
		both channels dominant; V_{TXDx} = 0 V; short circuit on bus lines; -3 V < ($V_{CANHx} = V_{CANLx}$) < +40 V	-	-	250	mA
		Standby mode				
		TJA1448A,C; T_{vj} < 85 °C	-	-	2	µA
		TJA1448B; T_{vj} < 85 °C	-	11	18	µA
I/O level adapter supply; pin VIO (TJA1448A/C)						
V_{IO}	supply voltage		2.95	-	5.5	V

Table 9. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1448A/C); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{uvd(swoff)}$	switch-off undervoltage detection voltage	[2]	2.65	-	2.95	V
I_{IO}	supply current	Normal mode				
		both channels recessive; $V_{TXDx} = V_{IO}$	-	270	750	µA
		one channel dominant; one channel recessive	-	360	1000	µA
		both channels dominant; V_{TXDx} = 0 V	-	450	1250	µA
		Standby mode; T_{vj} < 85 °C	-	11	16	µA
CAN transmit data input; pins TXD1 and TXD2						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$[3]	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$[3]	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
C_i	input capacitance	[4]	-	-	10	pF
CAN receive data output; pins RXD1 and RXD2						
I_{OH}	HIGH-level output current	$V_{RXDx} = V_{IO}$[3] - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	V_{RXDx} = 0.4 V; bus dominant	1	-	10	mA
Standby control input; pins STB1 and STB2						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$[3]	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$[3]	V
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
C_i	input capacitance	[4]	-	-	10	pF
Bus lines; pins CANH1, CANH2, CANL1 and CANL2						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} ≥ 4.75 V; R_L = 50 Ω to 65 Ω				
		pin CANHx	2.75	3.5	4.5	V
		pin CANLx	0.5	1.5	2.25	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANHx} + V_{CANLx}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz [4] [5]	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{cm(step)}$	common mode voltage step	[4] [5] [6]	-150	-	+150	mV

Table 9. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1448A/C); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{cm(p-p)}$	peak-to-peak common mode voltage	[4] [5] [6]	-300	-	+300	mV
$V_{O(dif)}$	differential output voltage	dominant; Normal mode; V_{TXDx} = 0 V; $t < t_{to(dom)TXD}$; $V_{CC} \geq 4.75$ V				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω [4]	1.5	-	5	V
		recessive; no load				
		Normal mode; $V_{TXDx} = V_{IO}$[3]	-50	-	+50	mV
		Standby mode	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXDx} = V_{IO}$[3]; no load	2	2.5	3	V
		Standby mode; no load	-0.1	-	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	-12 V ≤ V_{CANHx} ≤ +12 V; -12 V ≤ V_{CAxNL} ≤ +12 V				
		Normal mode	0.5	-	0.9	V
		Standby mode	0.4	-	1.1	V
$V_{rec(RX)}$	receiver recessive voltage	-12 V ≤ V_{CANHx} ≤ +12 V; -12 V ≤ V_{CANLx} ≤ +12 V				
		Normal mode	-4	-	+0.5	V
		Standby mode	-4	-	+0.4	V
$V_{dom(RX)}$	receiver dominant voltage	-12 V ≤ V_{CANHx} ≤ +12 V; -12 V ≤ V_{CANLx} ≤ +12 V				
		Normal mode	0.9	-	9	V
		Standby mode	1.1	-	9	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	-12 V ≤ V_{CANHx} ≤ +12 V; -12 V ≤ V_{CANLx} ≤ +12 V; Normal mode	50	-	-	mV
$I_{O(sc)}$	short-circuit output current	-15 V ≤ V_{CANHx} ≤ +40 V; -15 V ≤ V_{CANLx} ≤ +40 V	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	-27 V ≤ V_{CANHx} ≤ +32 V; -27 V ≤ V_{CANLx} ≤ +32 V; Normal mode; $V_{TXD} = V_{IO}$[3]	-3	-	+3	mA
I_L	leakage current	$V_{CC} = V_{IO}$ = 0 V or pins shorted to GND via 47 KΩ; $V_{CANHx} = V_{CANLx}$ = 5 V	-10	-	+10	µA
R_i	input resistance	-2 V ≤ V_{CANLx} ≤ +7 V; -2 V ≤ V_{CANHx} ≤ +7 V	25	40	50	kΩ
ΔR_i	input resistance deviation	0 V ≤ V_{CANLx} ≤ +5 V; 0 V ≤ V_{CANHx} ≤ +5 V	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	50	80	100	kΩ

Table 9. Static characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1448A/C); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{i(cm)}$	common-mode input capacitance	[4]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[4]	-	-	10	pF
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[4]	180	-	200	°C
$T_{j(sd)rel}$	release shutdown junction temperature	[4]	175	-	195	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
[3] V_{CC} in TJA1448B
[4] Not tested in production; guaranteed by design.
[5] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C_{SPLIT}) is shown in Figure 15.
[6] See Figure 11

11 Dynamic characteristics

Table 10. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1448A/C); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics; $t_{bit(TXD)}$ ≥ 200 ns; see Figure 9, Figure 10 and Figure 14						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	-	102.5	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	-	102.5	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	-	115	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	-	115	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	215	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	215	ns
CAN FD timing characteristics according to ISO 11898-2:2016; see Figure 10 and Figure 14						
$t_{bit(bus)}$	transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	-	530	ns
		$t_{bit(TXD)}$ = 200 ns	155	-	210	ns
Δt_{rec}	receiver timing symmetry	$t_{bit(TXD)}$ = 500 ns	-65	-	+40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-	+15	ns
$t_{bit(RXD)}$	bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	-	550	ns
		$t_{bit(TXD)}$ = 200 ns	120	-	220	ns
Dominant time-out time; pins TXD1 and TXD2						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [2] [3]	0.8	-	9	ms
Bus wake-up times; pins CANH1, CANH2 and CANL1, CANL2; see Figure 7 and Figure 8						
$t_{wake(busdom)}$	bus dominant wake-up time	Standby mode [2] [4]	0.5	-	1.8	µs
$t_{wake(busrec)}$	bus recessive wake-up time	Standby mode [2] [4]	0.5	-	1.8	µs
$t_{to(wake)bus}$	bus wake-up time-out time	Standby mode [2] [3]	0.8	-	9	ms
$t_{fltr(wake)bus}$	bus wake-up filter time	TJA1448A/B; Standby mode [2]	-	-	1.8	µs
Mode transitions						
$t_{t(moch)}$	mode change transition time	[2]	-	-	50	µs
$t_{startup}$	start-up time	[2]	-	-	1	ms
$t_{startup(RXD)}$	RXD start-up time	after wake-up detected [2] [5]	4	-	20	µs
IO filter; pins STB1 and STB2						
$t_{fltr(IO)}$	IO filter time	[6]	1	-	5	µs
Undervoltage detection; see Figure 4 and Figure 5						
$t_{det(uv)}$	undervoltage detection time	on pin VCC [2]	-	-	30	µs
$t_{uvd(swoff)}$	switch-off undervoltage detection time	on pin VCC; TJA1448B [2]	-	-	30	µs

Table 10. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.95 V to 5.5 V (TJA1448A/C); R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		on pin VIO; TJA1448A/C [2]			30	µs
$t_{rec(uv)}$	undervoltage recovery time	on pin VCC [2]	-	-	50	µs

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.
[4] A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.
[5] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see Figure 7 and Figure 8.
[6] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

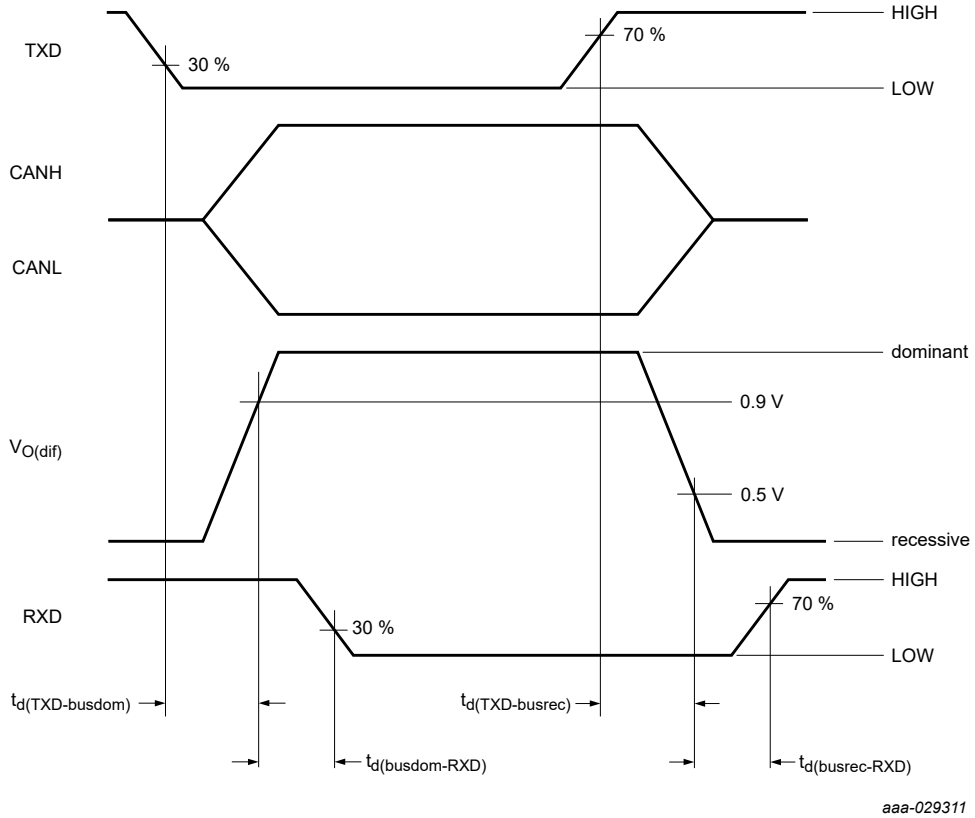


Figure 9. CAN transceiver timing diagram

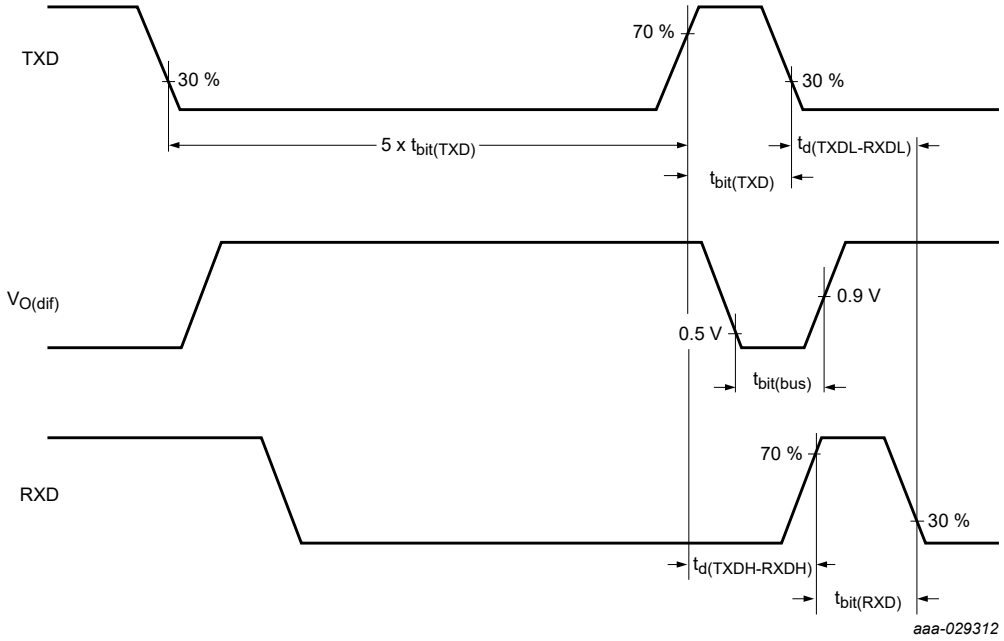


Figure 10. CAN FD timing definitions according to ISO 11898-2:2016

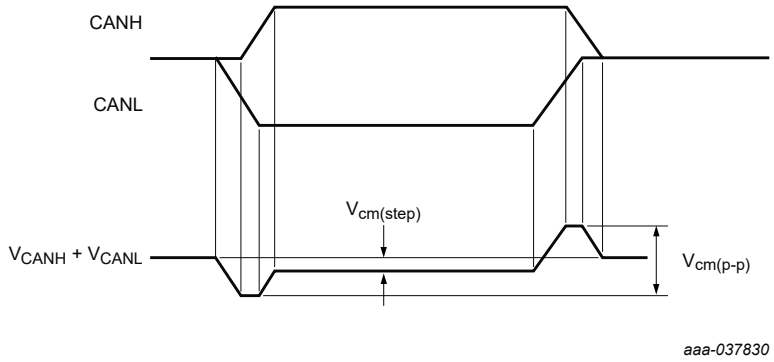
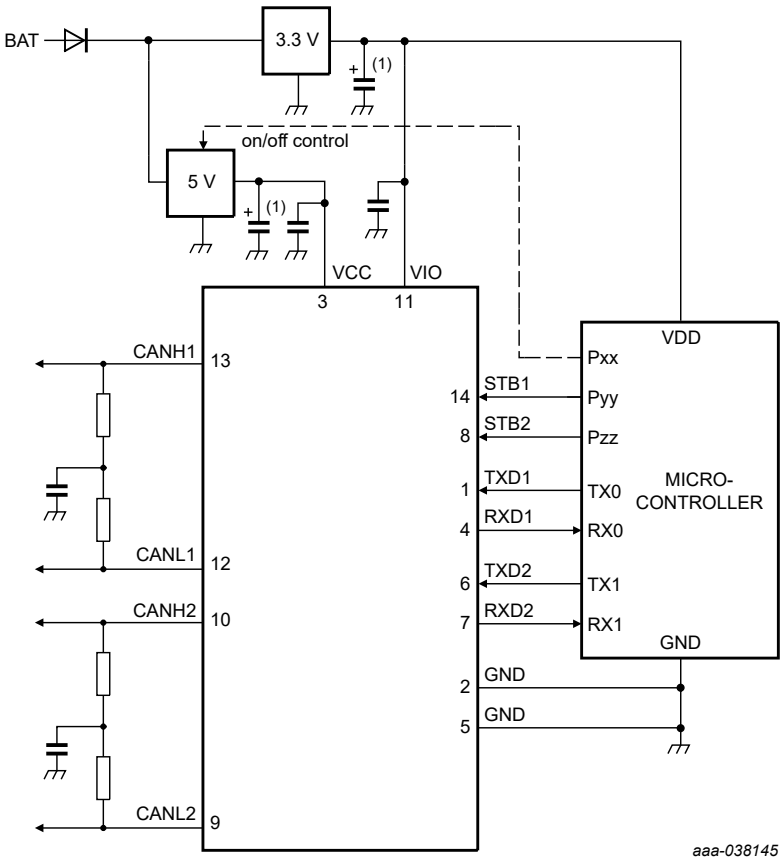


Figure 11. CAN bus common-mode voltage

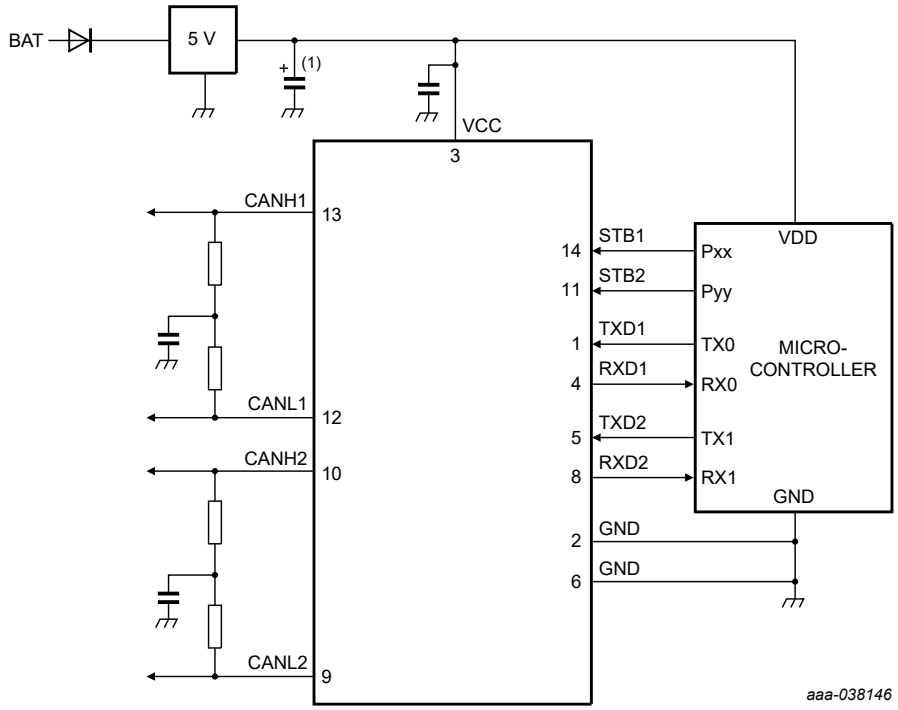
12 Application information

12.1 Application diagrams



(1) Optional, depends on regulator.

Figure 12. Typical TJA1448A/C application with a 3.3 V microcontroller



(1) Optional, depends on regulator.

Figure 13. Typical TJA1448B application with a 5 V microcontroller

12.2 Application hints

Further information on the application of the TJA1448 can be found in NXP application hints AH2002 *'TJx144x/TJx146x Application Hints'*, available on request from NXP Semiconductors.

13 Test information

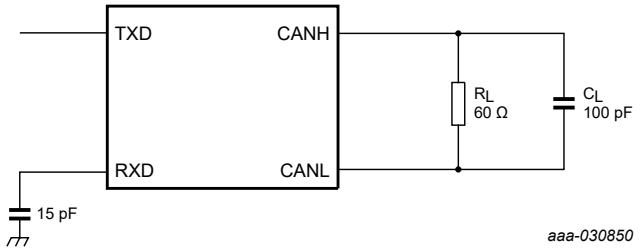


Figure 14. CAN transceiver timing test circuit

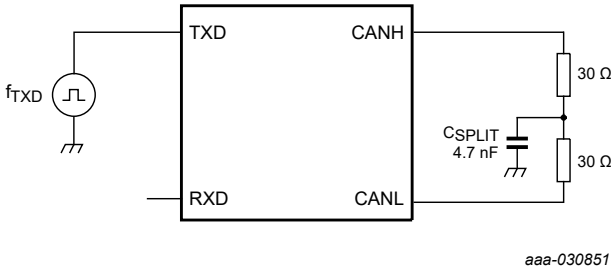


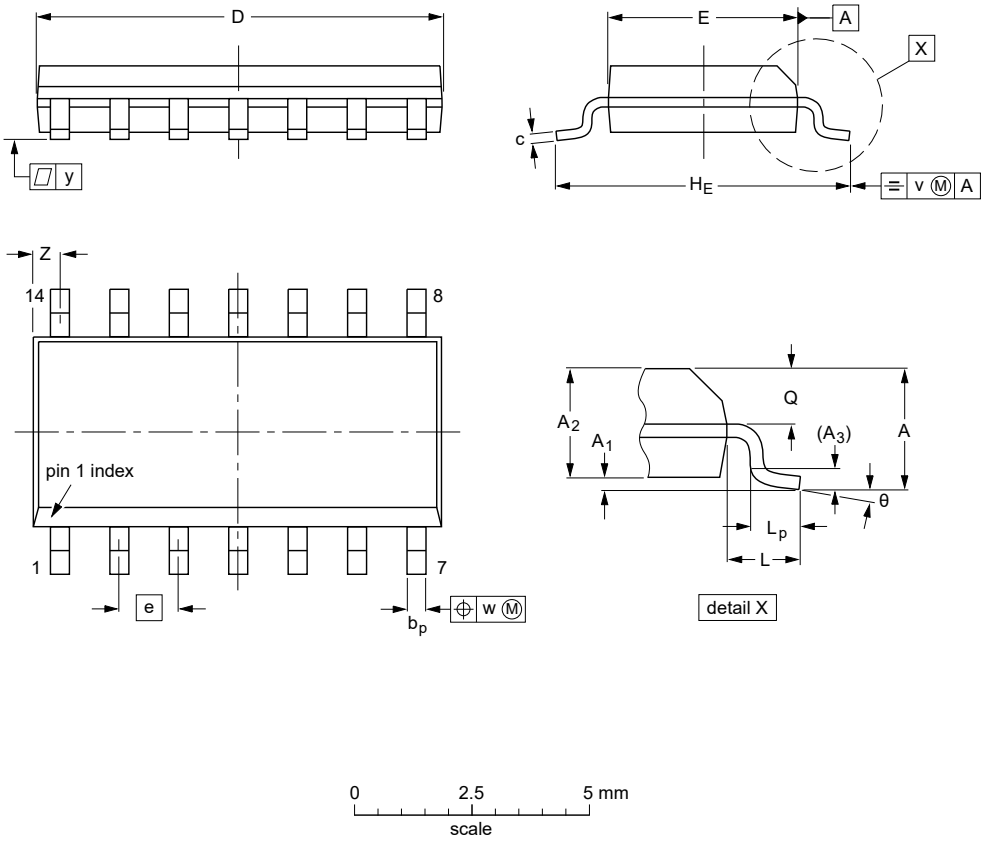
Figure 15. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

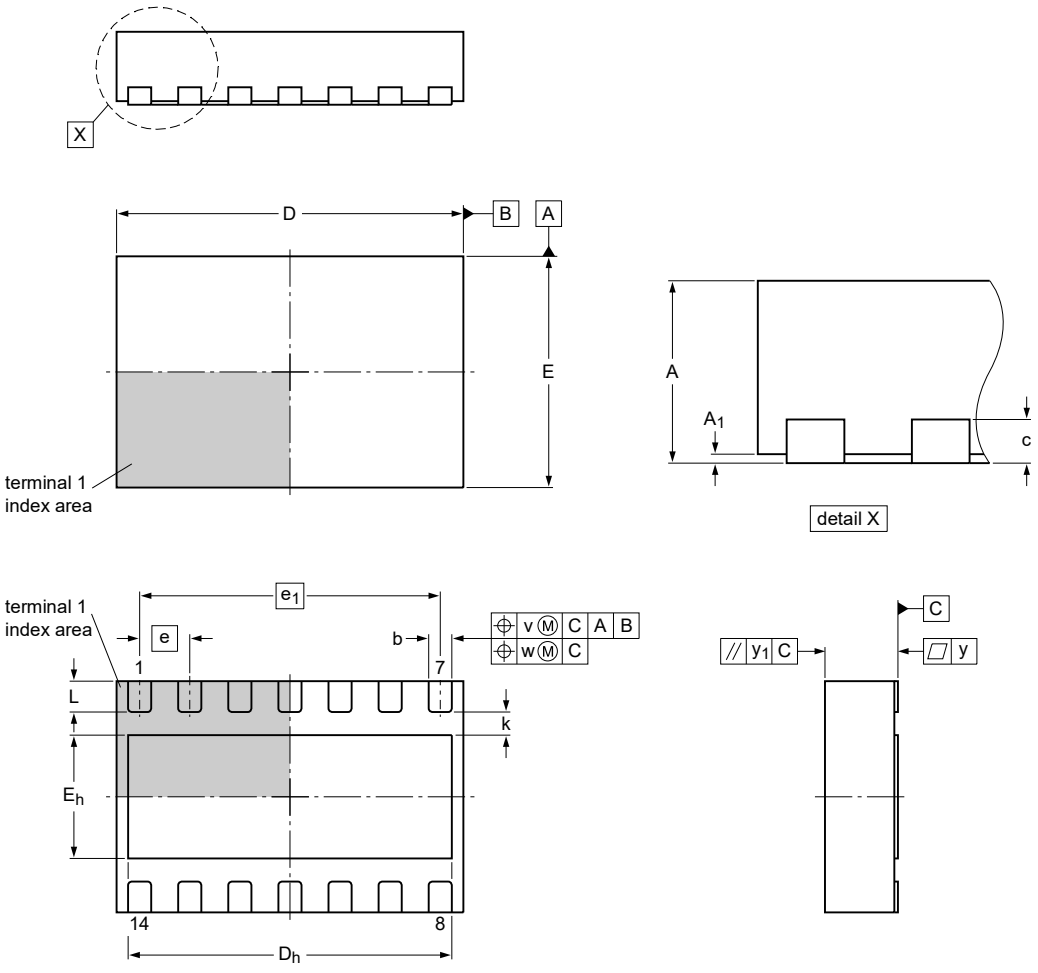
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Figure 16. Package outline SOT108-1 (SO14)

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit	A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Figure 17. Package outline SOT1086-2 (HVSON14)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and Table 12

Table 11. SnPb eutectic process (from J-STD-020D)

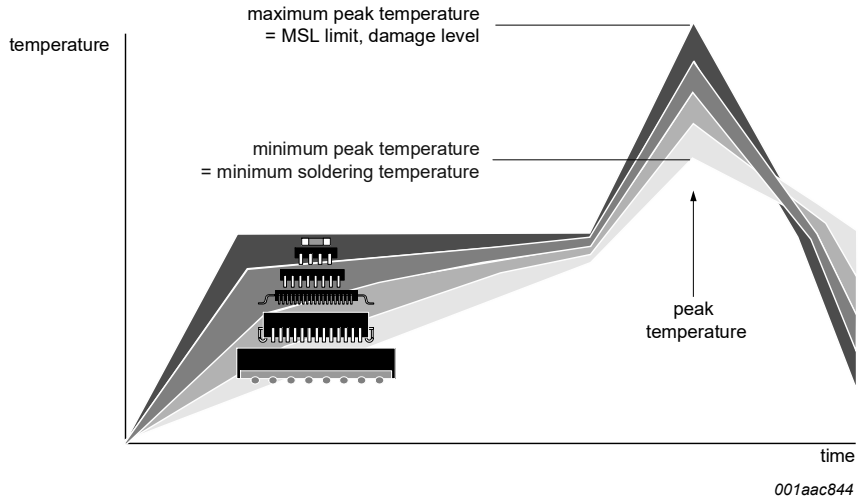
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Figure 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application note:

- AN10365 "Surface mount reflow soldering description"

18 Appendix: ISO 11898-2:2016 parameter cross-reference list

Table 13. ISO 11898-2:2016 to NXP data sheet parameter conversion

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
HS-PMA driver symmetry			
Driver symmetry	V_{SYM}	V_{TXsym}	transmitter voltage symmetry
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out, long	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time
Transmit dominant time-out, short			
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	R_{Diff}	$R_{i(dif)}$	differential input resistance
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	R_i	input resistance
Matching of internal resistance	MR	ΔR_i	input resistance deviation
HS-PMA implementation loop delay requirement			
Loop delay	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW

Table 13. ISO 11898-2:2016 to NXP data sheet parameter conversion*...continued*

ISO 11898-2:2016		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s			
Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended	$t_{Bit(Bus)}$	$t_{bit(bus)}$	transmitted recessive bit width
Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RXD)}$	bit time on pin RXD
Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s	Δt_{Rec}	Δt_{rec}	receiver timing symmetry
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating V_{Diff}	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating VCAN_H and VCAN_L			
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA bus biasing control timings			
CAN activity filter time, long	t_{Filter}	$t_{wake(busdom)}$[1] $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
CAN activity filter time, short			
Wake-up time-out, short	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up time-out, long			

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality

19 Appendix: TJx144x/TJx146x/TJF1441 family overview

Table 14. Feature overview of the complete TJx144x/TJx146x/TJF1441 family

	Modes					Supplies			Data rate		Additional features					
Device[1]	Normal	Standby	Sleep	Silent/Listen-only	Selectable Off	VCC pin	VIO pin	VBAT pin	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN FD[2]	Signal improvement[3]	Wake-up source recognition[4]	Short WUP support [0.5 - 1.8 µs][5]	Single supply pin wake-up[6]	TXD dominant timeout	Local diagnostics via ERR_N pin
TJx1441A	●			●		●	●		●						●	
TJx1441B	●			●		●			●						●	
TJx1441D	●			●	●	●			●						●	
TJF1441A	●			●		●	●		●						[7]	
TJx1442A	●	●				●	●		●				●	●	●	
TJx1442B	●	●				●			●				●		●	
TJx1443A	●	●	●	●		●	●	●	●			●	●	●	●	●
TJx1448A	●	●				●	●		●				●	●	●	
TJx1448B	●	●				●			●				●		●	
TJx1448C	●	●				●	●		●			●	●	●	●	
TJx1462A	●	●				●	●		●	●	●		●	●	●	
TJx1462B	●	●				●			●	●	●		●		●	
TJx1463A	●	●	●	●		●	●	●	●	●	●	●	●	●	●	●

[1] TJx: TJA14xxx is AEC-Q100 Grade 1; TJR14xxx is AEC-Q100 Grade 0; TJF1441A is non-automotive grade.
[2] Only guaranteed for TJA146x, AEC-Q100 Grade 1.
[3] CAN FD Signal Improvement Capability (SIC) according to CiA 601-4:2019.
[4] RXD is held LOW after wake-up request, enabling wake-up source recognition.
[5] WUP = wake-up pattern according ISO11898-2:2016.
[6] Only VIO supply needed for wake-up in TJA1442A, TJA1448A, TJA1448C, TJA1462A; only VBAT supply needed for wake-up in TJA1443A, TJA1463A.
[7] Not having TXD dominant timeout allows for very low data rates in non-automotive grade applications.

20 Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1448 v.2	20211015	Product data sheet	-	TJA1448 v.1
Modifications	• Added device (Table 3) and family (Section 19) feature overviews • Table 7: table note 10 added • Table 10: CAN delay timing characteristics revised; measurement conditions for parameter $t_{startup(RXD)}$ revised • Section 21: *Suitability for use in Automotive applications* and *Security* disclaimers revised			
TJA1448 v.1	20200812	Product data sheet	-	-

21 Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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