TJA1057

High-speed CAN transceiver

Rev. 8 — 10 September 2024

Product data sheet

1 General description

The TJA1057 is part of the Mantis family of high-speed CAN transceivers. It provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1057 offers a feature set optimized for 12 V automotive applications, with significant improvements over first- and second-generation CAN transceivers from NXP, such as the TJA1050, and excellent electromagnetic compatibility (EMC) performance. The TJA1057 also displays ideal passive behavior to the CAN bus when the supply voltage is off.

Variants with a V_{IO} pin can be interfaced directly with microcontrollers with supply voltages from 3.3 V to 5 V.

The TJA1057 implements the CAN physical layer as defined in ISO 11898-2:2024 third edition and SAE J2284-1 to SAE J2284-5. The TJA1057T is specified for data rates up to 1 Mbit/s. Additional timing parameters defining loop delay symmetry are specified for the other variants. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The TJA1057B and TJA1057C feature shorter propagation delay, supporting larger network topologies.

These features make the TJA1057 an excellent choice for HS-CAN networks that only require basic CAN functionality.

2 Features and benefits

2.1 General

- Fully ISO 11898-2:2024, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant[1]
- Optimized for use in 12 V automotive systems
- Low electromagnetic emission and high electromagnetic immunity, according to EMC standards IEC TS62228 and SAE J2962-2:2019[2]
- AEC-Q100 qualified
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Shorter propagation delay on the TJA1057B and TJA1057C variants supports larger network topologies (see Table 8)
- Variants with a V_{IO} pin allow for direct interfacing with 3.3 V to 5 V microcontrollers. Variants without a V_{IO} pin can interface with 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.

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[1] Compliant with the exception of parameters V_CM(STEP) and V_CM(PP); intended as an indication of emission performance. Note that the device fullfills the EMC requirements, as evidenced through IBEE reports available on request.

[2] Verified by an external test house for TJA1057B/C.

- Both V_{IO} and non-V_{IO} variants are available in SO8 and leadless HVSON8 (3.0 mm × 3.0 mm) packages; HVSON8 with improved Automated Optical Inspection (AOI) capability.

2.2 Predictable and fail-safe behavior

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus (high-ohmic) when the supply voltage drops below the undervoltage threshold
- Transmit Data (TXD) dominant time-out function
- Internal biasing of TXD and S input pins

2.3 Protection

- High ESD handling capability on the bus pins (8 kV IEC and HBM)
- Bus pins protected against transients in automotive environments
- Undervoltage detection on pins V_{CC} and V_{IO}
- Thermally protected

2.4 TJA1057 CAN FD (applicable to all product variants except TJA1057T)

- Timing guaranteed for data rates up to 5 Mbit/s

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IO}	supply voltage on pin V_{IO}		2.91	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	4	4.3	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		2.1	-	2.8	V
I_{CC}	supply current	Silent mode	0.1	-	1.2	mA
		Normal mode; bus recessive	2	5	10	mA
		Normal mode; bus dominant	20	45	70	mA
I_{IO}	supply current on pin V_{IO}	Silent mode	-	3	16	μA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$	-	7	30	μA
		dominant; $V_{TXD} = 0$ V	-	110	320	μA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	-8	-	+8	kV
V_{CANH}	voltage on pin CANH	limiting value according to IEC60134	-42	-	+42	V
V_{CANL}	voltage on pin CANL	limiting value according to IEC60134	-42	-	+42	V
T_{vj}	virtual junction temperature		-40	-	+150	°C

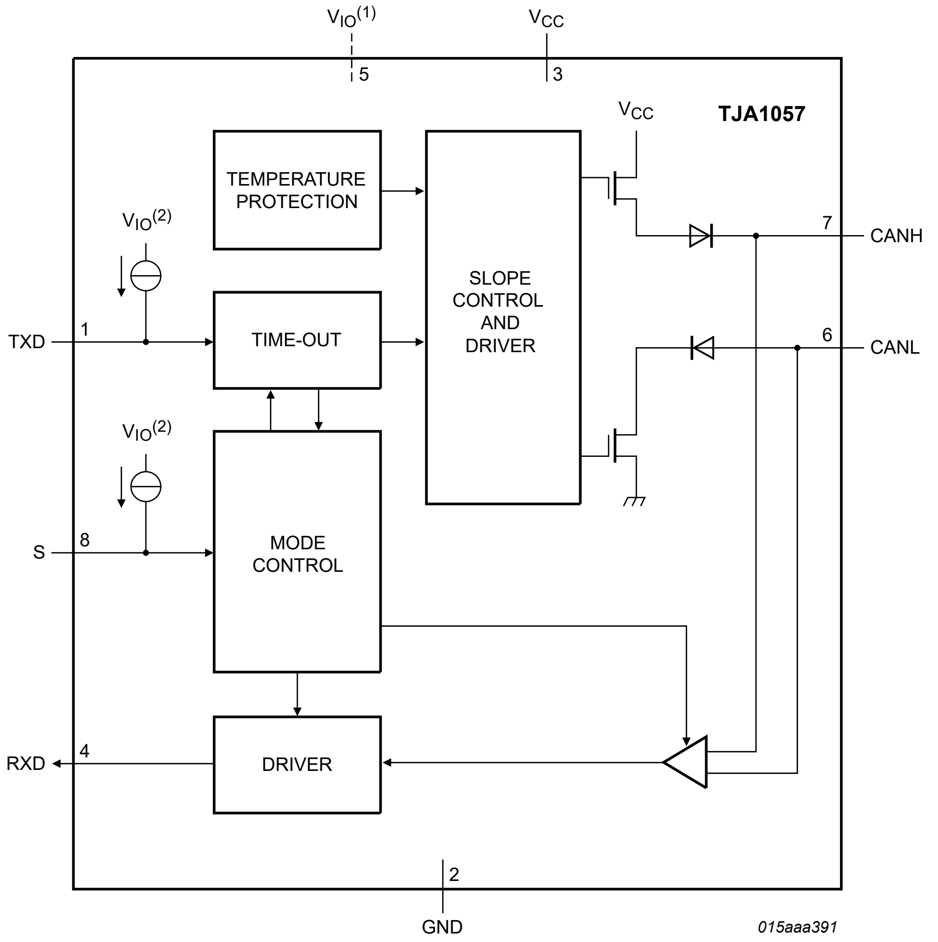
4 Ordering information

Table 2. Ordering information

Type number[1]	Package		
	Name	**Description**	**Version**
TJA1057T TJA1057BT TJA1057CT TJA1057GT TJA1057GT/3	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1057BTK TJA1057CTK TJA1057GTK TJA1057GTK/3	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT782-1

[1] TJA1057GT(K)/3 and TJA1057BT(K) with V_{IO} pin; all variants other than TJA1057T support CAN FD.

5 Block diagram

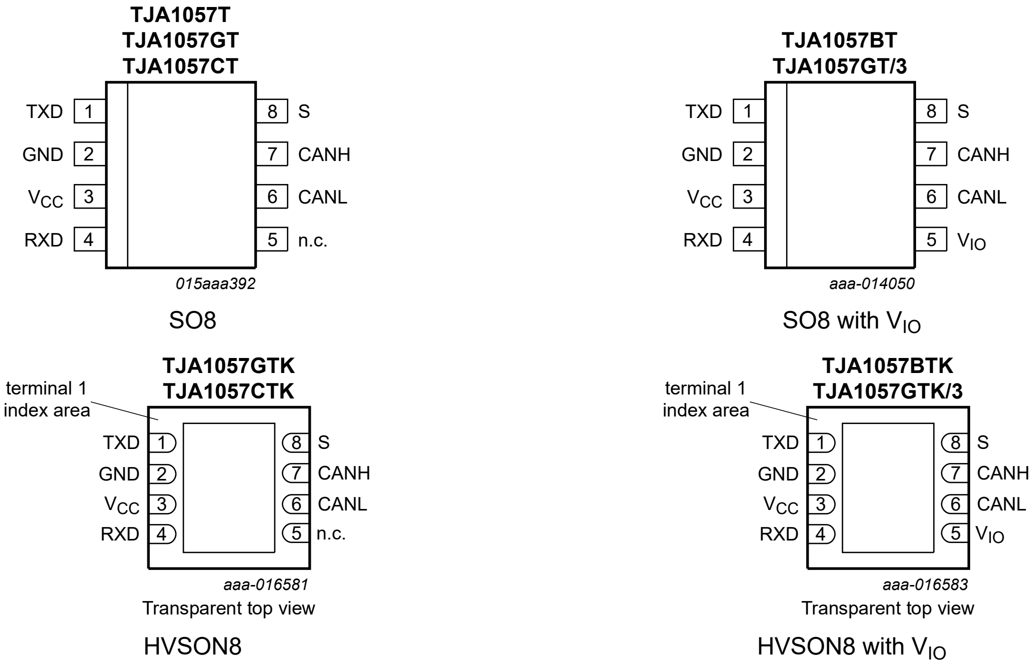


1. Pin 5 is not connected in non-V_{IO} product variants.
2. V_{IO} = V_{CC} in non-V_{IO} product variants.

Figure 1. Block diagram

6 Pinning information

6.1 Pinning



SO8

SO8 with V_{IO}

HVSON8

HVSON8 with V_{IO}

Figure 2. Pin configuration diagrams

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input
GND[2]	2	G	ground
V_{CC}	3	P	supply voltage
RXD	4	O	receive data output; reads out data from the bus lines
n.c.	5	-	not connected in TJA1057T, TJA1057GT, TJA1057CT, TJA1057GTK and TJA1057CTK
V_{IO}	5	P	supply voltage for I/O level adapter in TJA1057GT(K)/3 and TJA1057BT(K)
CANL	6	AIO	LOW-level CAN bus line
CANH	7	AIO	HIGH-level CAN bus line
S	8	I	Silent mode control input

[1] I: digital input; O: digital output; AIO: analog input/output; P: power supply; G: ground.

[2] HVSON8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

7 Functional description

7.1 Operating modes

The TJA1057 supports two operating modes, Normal and Silent. The operating mode is selected via pin S. See Table 4 for a description of the operating modes under normal supply conditions.

Table 4. Operating modes

Mode	Inputs		Outputs	
	Pin S	Pin TXD	CAN driver	Pin RXD
Normal	LOW	LOW	dominant	LOW
		HIGH	recessive	LOW when bus dominant
				HIGH when bus recessive
Silent	HIGH	x[1]	biased to recessive	LOW when bus dominant
				HIGH when bus recessive

[1] 'x' = don't care.

7.1.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines, CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

7.1.2 Silent mode

A HIGH level on pin S selects Silent mode. The transmitter is disabled in Silent mode, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller disrupting all network communications.

7.2 Fail-safe features

7.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

7.2.2 Internal biasing of TXD and S input pins

Pins TXD and S have internal pull-ups to V_{CC} (or V_{IO} in variants with a V_{IO} pin) to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Silent mode to minimize supply current.

7.2.3 Undervoltage detection on pins V_{CC} and V_{IO} (TJA1057GT(K)/3 and TJA1057BT(K) variants)

If V_{CC} or V_{IO} drops below the undervoltage detection level, $V_{uvd(VCC)}$/$V_{uvd(VIO)}$, the transceiver switches off and disengages from the bus (zero load; bus pins floating) until the supply voltage has recovered. The output drivers are enabled once both V_{CC} and V_{IO} are again within their operating ranges and TXD has been reset to HIGH.

7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{j(sd)}$ again, the output drivers recover once TXD has been reset to HIGH (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature).

7.2.5 V_{IO} supply pin (TJA1057GT(K)/3 and TJA1057BT(K) variants)

Pin V_{IO} should be connected to the microcontroller supply voltage (see Figure 5). This will adjust the signal levels on pins TXD, RXD and S to the I/O levels of the microcontroller.

For versions of the TJA1057 without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}. The signal levels on pins TXD, RXD and S are set to levels compatible with 5 V microcontrollers. This allows the device to interface with both 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to ground.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x[1]	on pins CANH, CANL	-42	+42	V
		on pins V_{CC}, V_{IO}	-0.3	+7	V
		on any other pin [2]	-0.3	V_{IO}[3] + 0.3	V
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-27	+27	V
V_{trt}	transient voltage	on pins CANH, CANL [4]			
		pulse 1	-100	-	V
		pulse 2a	-	75	V
		pulse 3a	-150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [5]			
		on pins CANH and CANL	-8	+8	kV
		SAE J2962-2:2019 (330 pF, 2kΩ) on pins CANH, CANL [6]			
		powered air discharge	-15	+15	kV
		powered contact discharge	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [7]	-4	+4	kV
		on pins CANH and CANL [8]	-8	+8	kV
		Machine Model (MM); 200 pF, 0.75 μH, 10 Ω [9]			
		on any pin	-200	+200	V
		Charged Device Model (CDM) [10]			
		on corner pins	-750	+750	V
		on any other pin	-500	+500	V
T_{vj}	virtual junction temperature	[11]	-40	+150	°C
T_{stg}	storage temperature	[12]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] Maximum voltage should never exceed 7 V.

[3] V_{IO} + 0.3 = V_{CC} + 0.3 in the non-V_{IO} product variants.

[4] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.

[5] Verified by an external test house according to IEC TS 62228, Section 4.3.

[6] Verified by an external test house according to ISO 10605 for TJA1057B/C.

[7] According to AEC-Q100-002.

[8] Pins stressed to reference group containing all ground and supply pins, emulating the application circuits (Figure 4 and Figure 5). HBM pulse as specified in AEC-Q100-002 used.

[9] According to AEC-Q100-003.

[10] According to AEC-Q100-011.

[11] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

[12] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 6. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8 package; in free air	94	K/W
		HVSON8 package; in free air	54	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	HVSON8 package; in free air	16	K/W
$\Psi_{j\text{-}top}$	thermal characterization parameter from junction to top of package	SO8 package; in free air	13	K/W
		HVSON8 package; in free air	6	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).

10 Static characteristics

Table 7. Static characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.91 V to 5.5 V[1]; R_L = 60 Ω; C_L = 100 pF unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}	[3]	3.5	4	4.3	V
I_{CC}	supply current	Silent mode; $V_{TXD} = V_{IO}$[4]	0.1	-	1.2	mA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$[4]	2	5	10	mA
		dominant; V_{TXD} = 0 V	20	45	70	mA
		dominant; short circuit on bus lines; V_{TXD} = 0 V; -3 V < ($V_{CANH} = V_{CANL}$) < +18 V	2	80	110	mA
I/O level adapter supply; pin V_{IO}[1]						
V_{IO}	supply voltage on pin V_{IO}		2.91	-	5.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}	[3]	2.1	-	2.8	V
I_{IO}	supply current on pin V_{IO}	Silent mode	-	3	16	µA
		Normal mode				
		recessive; $V_{TXD} = V_{IO}$[4]	-	7	30	µA
		dominant; V_{TXD} = 0 V	-	110	320	µA

Table 7. Static characteristics*...continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.91 V to 5.5 V[1]; R_L = 60 Ω; C_L = 100 pF unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Silent mode control input; pin S						
V_{IH}	HIGH-level input voltage		2	-	V_{IO}[4] + 0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.8	V
I_{IH}	HIGH-level input current	$V_S = V_{IO}$[4]	-1	-	+1	μA
I_{IL}	LOW-level input current	V_S = 0 V	-15	-	-1	μA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		2	-	V_{IO}[4] + 0.3	V
V_{IL}	LOW-level input voltage		-0.3	-	0.8	V
I_{IH}	HIGH-level input current	$V_{TXD} = V_{IO}$[4]	-5	-	+5	μA
I_{IL}	LOW-level input current	V_{TXD} = 0 V	-260	-	-30	μA
C_i	input capacitance	[5]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO}$[4] - 0.4 V	-9	-3	-1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	1	-	12	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; $t < t_{to(dom)TXD}$				
		pin CANH; R_L = 50 Ω to 65 Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50 Ω to 65 Ω	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH} - V_{CANL}$	-400	-	+400	mV
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; f_{TXD} = 250 kHz, 1 MHz and 2.5 MHz; C_{SPLIT} = 4.7 nF [5] [6]	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{O(dif)}$	differential output voltage	dominant; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$				
		R_L = 50 Ω to 65 Ω	1.5	-	3	V
		R_L = 45 Ω to 70 Ω	1.4	-	3.3	V
		R_L = 2240 Ω	1.5	-	5	V
		recessive; $V_{TXD} = V_{IO}$[4]; no load	-50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	$V_{TXD} = V_{IO}$[4]; no load	2	$0.5V_{CC}$	3	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal/Silent mode; $-12\ V \leq V_{CANL} \leq +12\ V$; $-12\ V \leq V_{CANH} \leq +12\ V$	0.5	-	0.9	V
$V_{rec(RX)}$	receiver recessive voltage	Normal/Silent mode; $-12\ V \leq V_{CANL} \leq +12\ V$; $-12\ V \leq V_{CANH} \leq +12\ V$ [5]	-4	-	0.5	V
$V_{dom(RX)}$	receiver dominant voltage	Normal/Silent mode; $-12\ V \leq V_{CANL} \leq +12\ V$; [5]	0.9	-	9.0	V

Table 7. Static characteristics*...continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.91 V to 5.5 V[1]; R_L = 60 Ω; C_L = 100 pF unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the IC.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$-12\ V \leq V_{CANH} \leq +12\ V$				
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal mode; $-12\ V \leq V_{CANL} \leq +12\ V$; $-12\ V\ v\ V_{CANH} \leq +12\ V$	50	-	300	mV
$I_{O(sc)dom}$	dominant short-circuit output current	V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = -15 V to +40 V	-100	-70	-	mA
		pin CANL; V_{CANL} = -15 V to +40 V	-	70	100	mA
$I_{O(sc)rec}$	recessive short-circuit output current	Normal mode; $V_{TXD} = V_{CC}$; $V_{CANH} = V_{CANL}$ = -27 V to +32 V	-5	-	+5	mA
I_L	leakage current	V_{CC} = 0 V or $V_{CC} = V_{IO}$ = shorted to ground via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V	-5	-	+5	µA
R_i	input resistance	$-2\ V \leq V_{CANL} \leq +7\ V$; $-2\ V \leq V_{CANH} \leq +7\ V$ [5]	9	15	28	kΩ
ΔR_i	input resistance deviation	$0\ V \leq V_{CANL} \leq +5\ V$; $0\ V \leq V_{CANH} \leq +5\ V$ [5]	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	$-2\ V \leq V_{CANL} \leq +7\ V$; $-2\ V \leq V_{CANH} \leq +7\ V$ [5]	19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	[5]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[5]	-	-	10	pF
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[5]	-	185	-	°C

[1] Only the TJA1057GT(K)/3 and TJA1057BT(K) variants have a V_{IO} pin; all circuitry is connected to V_{CC} in the other variants..
[2] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.
[3] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
[4] $V_{IO} = V_{CC}$ in non-V_{IO} product variants.
[5] Not tested in production; guaranteed by design.
[6] The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 7.

11 Dynamic characteristics

Table 8. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.91 V to 5.5 V[1]; R_L = 60 Ω; C_L = 100 pF unless specified otherwise; all voltages are defined with respect to ground.[2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 3 and Figure 6						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	TJA1057B/C; Normal mode [3]	-	62	90	ns
		other variants; Normal mode [3]	-	65	105	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	TJA1057B/C; Normal mode [3]	-	75	90	ns
		other variants; Normal mode [3]	-	90	105	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	TJA1057B/C; Normal mode [3]	-	60	100	ns
		other variants; Normal mode [3]	-	60	115	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	TJA1057B/C; Normal mode [3]	-	90	110	ns
		other variants; Normal mode [3]	-	65	135	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	TJA1057B/C; Normal mode	50	-	195	ns
		other variants; Normal mode	50	-	230	ns
		other variants; Normal mode; V_{CC} = 4.75 V to 5.25 V	50	-	210	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	TJA1057B/C; Normal mode	50	-	195	ns
		other variants; Normal mode	50	-	230	ns
		other variants; Normal mode; V_{CC} = 4.75 V to 5.25 V	50	-	210	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set B ($t_{bit(TXD)} \geq 200$ ns, up to 5 Mbit/s); see Figure 3 and Figure 6						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-45	-	+10	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-80	-	+20	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-45	-	+15	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set A ($t_{bit(TXD)} \geq 500$ ns, up to 2 Mbit/s); see Figure 3 and Figure 6						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-65	-	+30	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-100	-	+50	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-65	-	+40	ns
Dominant time-out time						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [4]	0.8	3	6.5	ms

[1] Only the TJA1057GT(K)/3 and TJA1057BT(K) variants have a V_{IO} pin; the V_{IO} input is internally connected to V_{CC} in the other variants.

[2] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range..

[3] Not tested in production; guaranteed by design.

[4] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

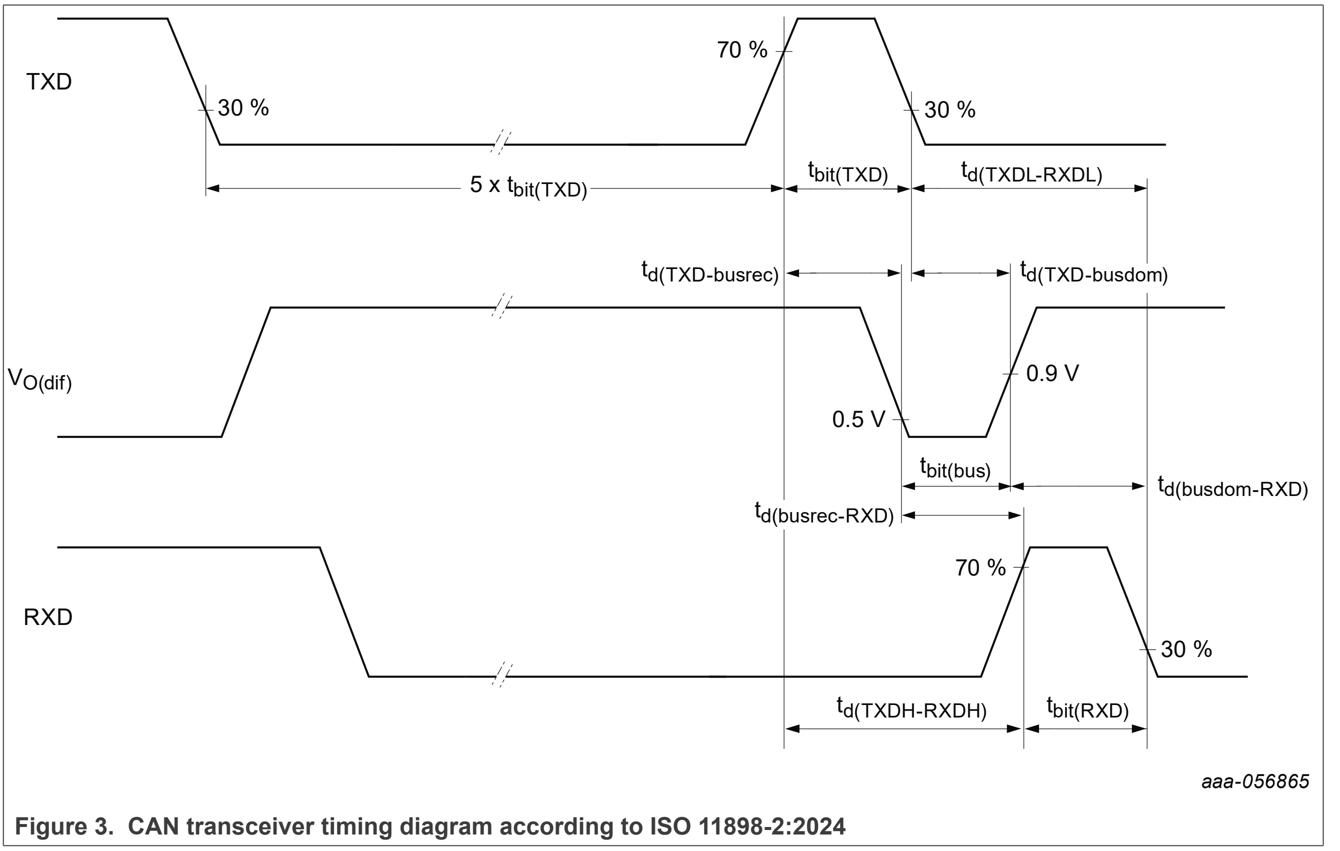
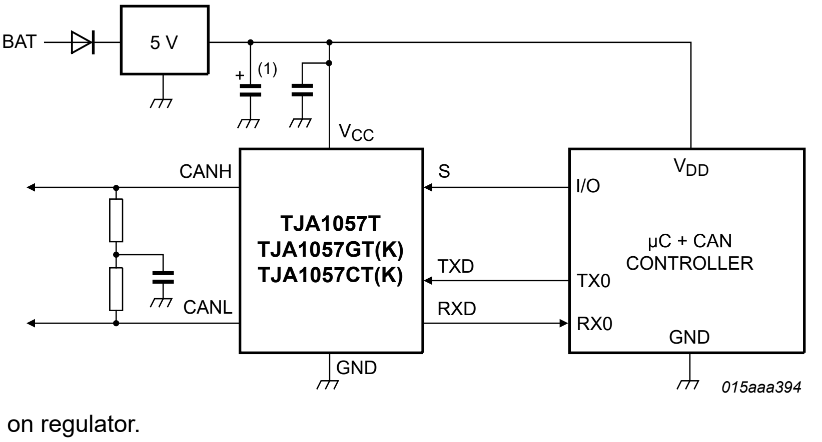


Figure 3. CAN transceiver timing diagram according to ISO 11898-2:2024

12 Application information

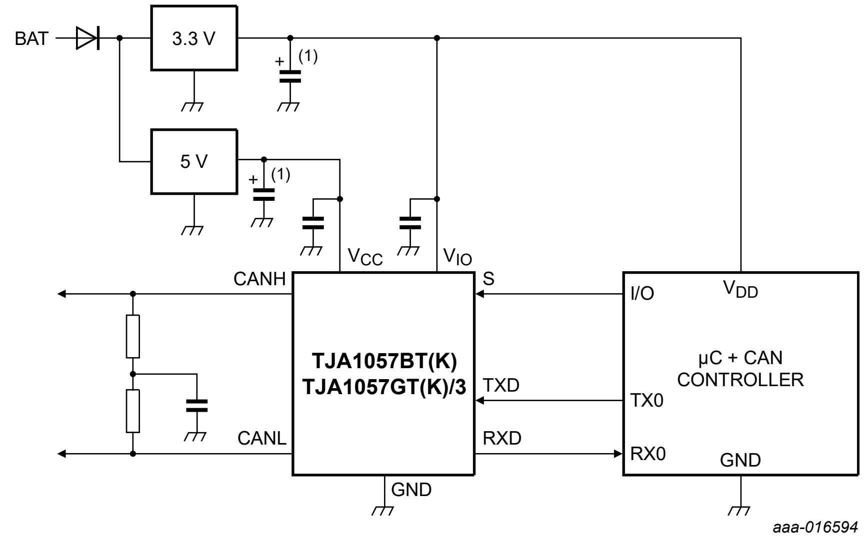
The minimum external circuitry needed with the TJA1057 is shown in Figure 4 and Figure 5. See the Application Hints (Section 12.2) for further information about external components and PCB layout requirements.

12.1 Application diagrams



1. Optional, depends on regulator.

Figure 4. Typical TJA1057 application with a 5 V microcontroller (non-V_{IO} variants)



1. Optional, depends on regulator.

Figure 5. Typical TJA1057 application with a 3.3 V microcontroller (V_{IO} variants)

12.2 Application hints

Further information on the application of the TJA1057 can be found in NXP application hints *AH1308 Application Hints - Standalone high-speed CAN transceivers Mantis TJA1044/TJA1057 and Dual-Mantis TJA1046*.

13 Test information

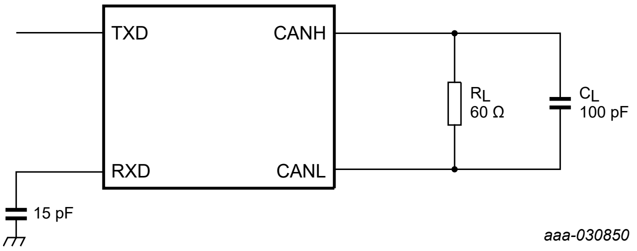


Figure 6. CAN transceiver timing test circuit

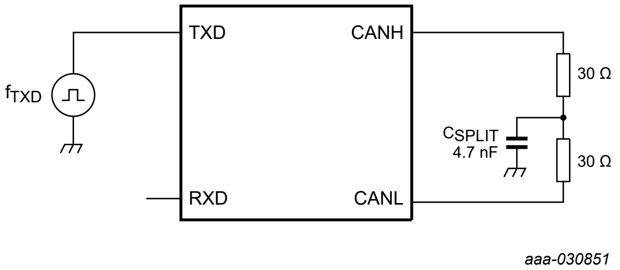


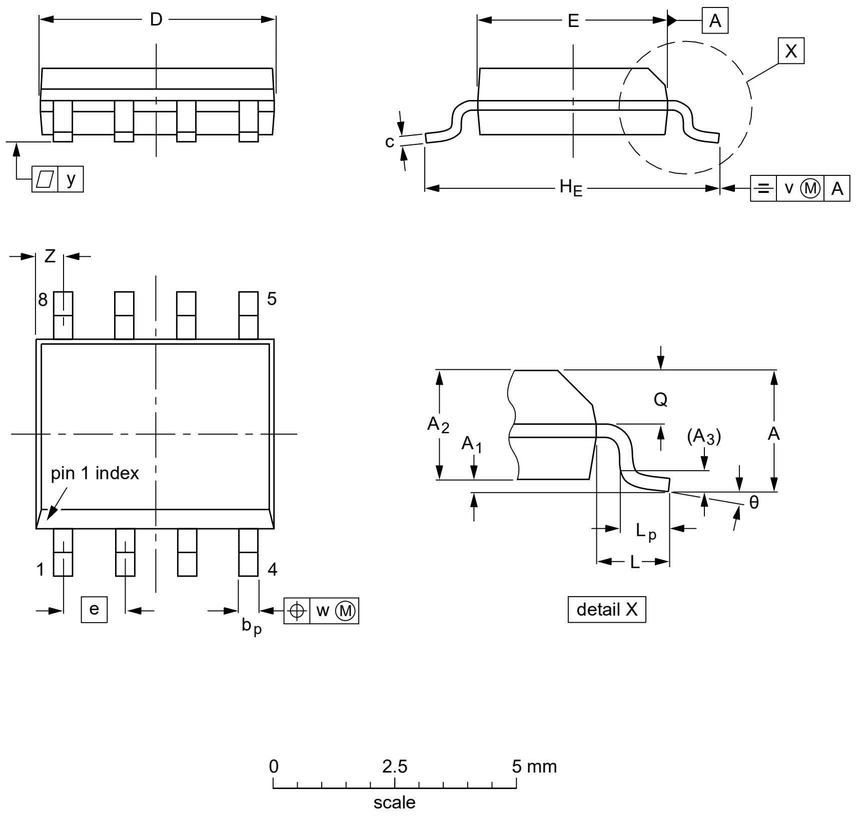
Figure 7. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

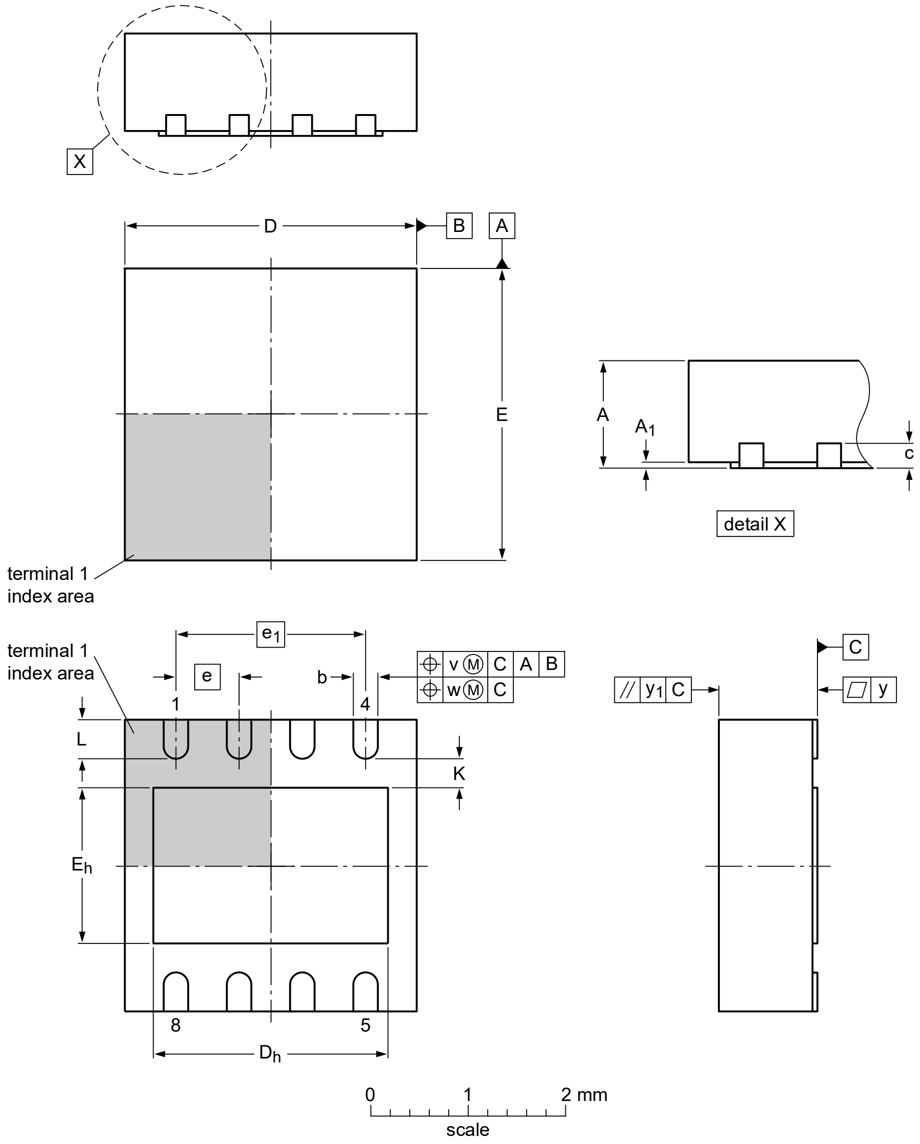
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Figure 8. Package outline SOT96-1 (SO8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads;
8 terminals; body 3 x 3 x 0.85 mm **SOT782-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	K	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
	nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note
1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	- - -	MO-229	- - -			~~09-08-25~~ 09-08-28

Figure 9. Package outline SOT782-1 (HVSON8)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 10) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and Table 10

Table 9. SnPb eutectic process (from J-STD-020D)

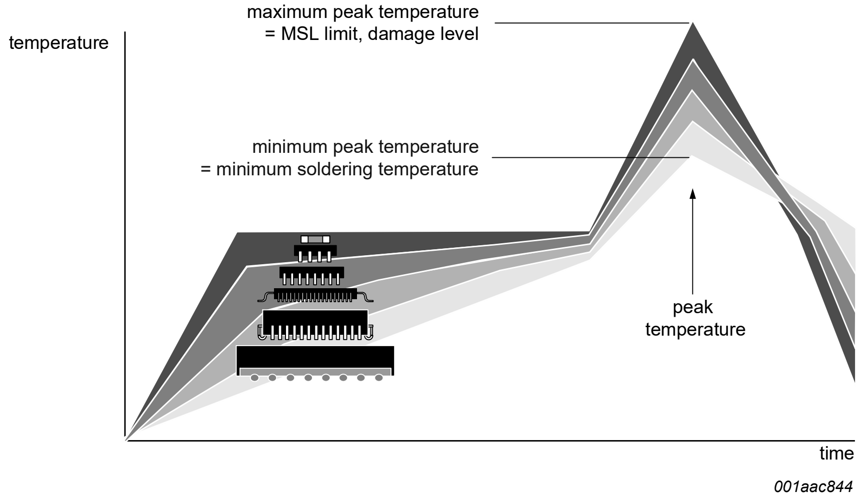
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 10.



MSL: Moisture Sensitivity Level

Figure 10. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17 Appendix: ISO 11898-2:2024 parameter cross-reference lists

Table 11. ISO 11898-2:2024 to NXP data sheet parameter conversion[1]

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating			
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	$R_{DIFF\_pas\_rec}$	$R_{i(dif)}$	differential input resistance
Single-ended internal resistance	$R_{SE\_pas\_rec\_H}$ $R_{SE\_pas\_rec\_L}$	R_i	input resistance
Matching of internal resistance	m_R	ΔR_i	input resistance deviation
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA driver symmetry			
Driver symmetry	V_{sym_vcc}	V_{TXsym}	transmitter voltage symmetry
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time

Table 11. ISO 11898-2:2024 to NXP data sheet parameter conversion[1] *...continued*

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA implementation loop delay requirements for parameter sets A, B and C			
Loop delay for parameter sets A and B	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
Loop delay for parameter set C		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD\_BUS)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
		$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive
Propagation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS\_RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominent to RXD
		$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD
HS-PMA implementation data signal timing requirements for parameter sets A, B and C			
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$	$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$	$\Delta t_{bit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry	$t_{\Delta REC}$	Δt_{rec}	receiver timing symmetry
HS-PMA implementation SIC timing and impedance for parameter set C			
Differential internal resistance (CAN_H to CAN_L)	$R_{DIFF\_act\_rec}$	$R_{i(actrec)}$	active recessive phase input resistance
Optional internal single-ended resistance	$R_{SE\_act\_rec}$	$R_{i(dif)actrec}$	active recessive phase differential input resistance
Start time of active signal improvement phase	$t_{act\_rec\_start}$	$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start
End time of active signal improvement phase	$t_{act\_rec\_end}$	$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end
Start time of passive recessive phase	$t_{pas\_rec\_start}$	$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus recessive end
PMA voltage wake-up control timing			
CAN activity filter time, long/short	t_{Filter}	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
Wake-up time-out	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up pattern signaling	t_{Flag}	$t_{startup(RXD)}$	RXD start-up time
		$t_{startup(INH)}$	INH start-up time
		$t_{startup(ERR\_N)}$	ERR_N start-up time
		$t_{startup}$	start-up time
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	$N_{bit(idle)}$	number of idle bits before a SOF is accepted
BitFilter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	$\rho_{Bitfilter\_option1}$	$t_{fltr(bit)dom}$	dominant bit filter time
CAN FD data phase bitfilter (option 2)	$\rho_{Bitfilter\_option2}$		
HS-PMA bus biasing control timing			
Time-out for bus activity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time

Table 11. ISO 11898-2:2024 to NXP data sheet parameter conversion[1] *...continued*

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
Bus bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	bus bias reaction time

[1] A number of proprietary NXP parameters are equivalent to parameters defined in ISO 11898-2:2024, but use different symbols. This conversion table allows ISO parameters to be cross-referenced with their NXP counterparts. The NXP parameters are defined in the Static and Dynamic characteristics tables. The conversion table provides a comprehensive listing - individual devices may not include all parameters.

18 Revision history

Table 12. Revision history

Document ID	Release date	Description
TJA1057 v.8.0	10 September 2024	Product data sheet Modifications: • ISO 11898-2:2016 upgraded to ISO 11898-2:2024 throughout • Section 2.1: EMC compliance updated • Table 5: SAE J2962-2:2019 V_{ESD} entries added • Table 8: Formatting of CAN (FD) timing characteristics revised • Original Figs. 3 and 4 combined in new single Figure 3 • Section 17: cross-reference table updated
TJA1057 v.7.0	16 January 2023	Product data sheet
TJA1057 v.6.0	24 August 2017	Product data sheet
TJA1057 v.5.1	23 May 2016	Product data sheet
TJA1057 v.5.0	28 January 2016	Product data sheet
TJA1057 v.4.0	10 July 2015	Product data sheet
TJA1057 v.3.0	19 November 2014	Product data sheet
TJA1057 v.2.0	30 October 2013	Product data sheet
TJA1057 v.1.0	30 May 2013	Preliminaly data sheet; initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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