DATA SHEET

TDA1517; TDA1517P
2 x 6 W stereo power amplifier

Product specification
Supersedes data of 2002 Jan 17

2004 Feb 18

2 x 6 W stereo power amplifier TDA1517; TDA1517P

FEATURES

- Requires very few external components
- High output power
- Fixed gain
- Good ripple rejection
- Mute/standby switch
- AC and DC short-circuit safe to ground and V_P
- Thermally protected
- Reverse polarity safe
- Capability to handle high energy on outputs (V_P = 0 V)
- No switch-on/switch-off plop
- Electrostatic discharge protection.

GENERAL DESCRIPTION

The TDA1517 is an integrated class-B dual output amplifier in a plastic single in-line medium power package with fin (SIL9MPF), a plastic rectangular-bent single in-line medium power package with fin (RBS9MPF) or a plastic heat-dissipating dual in-line package (HDIP18). The device is primarily developed for multi-media applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		6.0	14.4	18.0	V
I_{ORM}	repetitive peak output current		–	–	2.5	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{sb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
$\|Z_I\|$	input impedance		50	–	–	kΩ
P_o	output power	R_L = 4 Ω; THD = 0.5%	–	5	–	W
		R_L = 4 Ω; THD = 10%	–	6	–	W
SVRR	supply voltage ripple rejection	f_i = 100 Hz to 10 kHz	48	–	–	dB
α_{cs}	channel separation		40	–	–	dB
G_v	closed loop voltage gain		19	20	21	dB
$V_{no(rms)}$	noise output voltage (RMS value)		–	50	–	μV
T_c	crystal temperature		–	–	150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1517/N3	SIL9MPF	plastic single in-line medium power package with fin; 9 leads	SOT110-1
TDA1517/N3/S5	RBS9MPF	plastic rectangular-bent single in-line medium power package with fin; 9 leads	SOT352-1
TDA1517P	HDIP18	plastic heat-dissipating dual in-line package; 18 leads	SOT398-1

BLOCK DIAGRAM

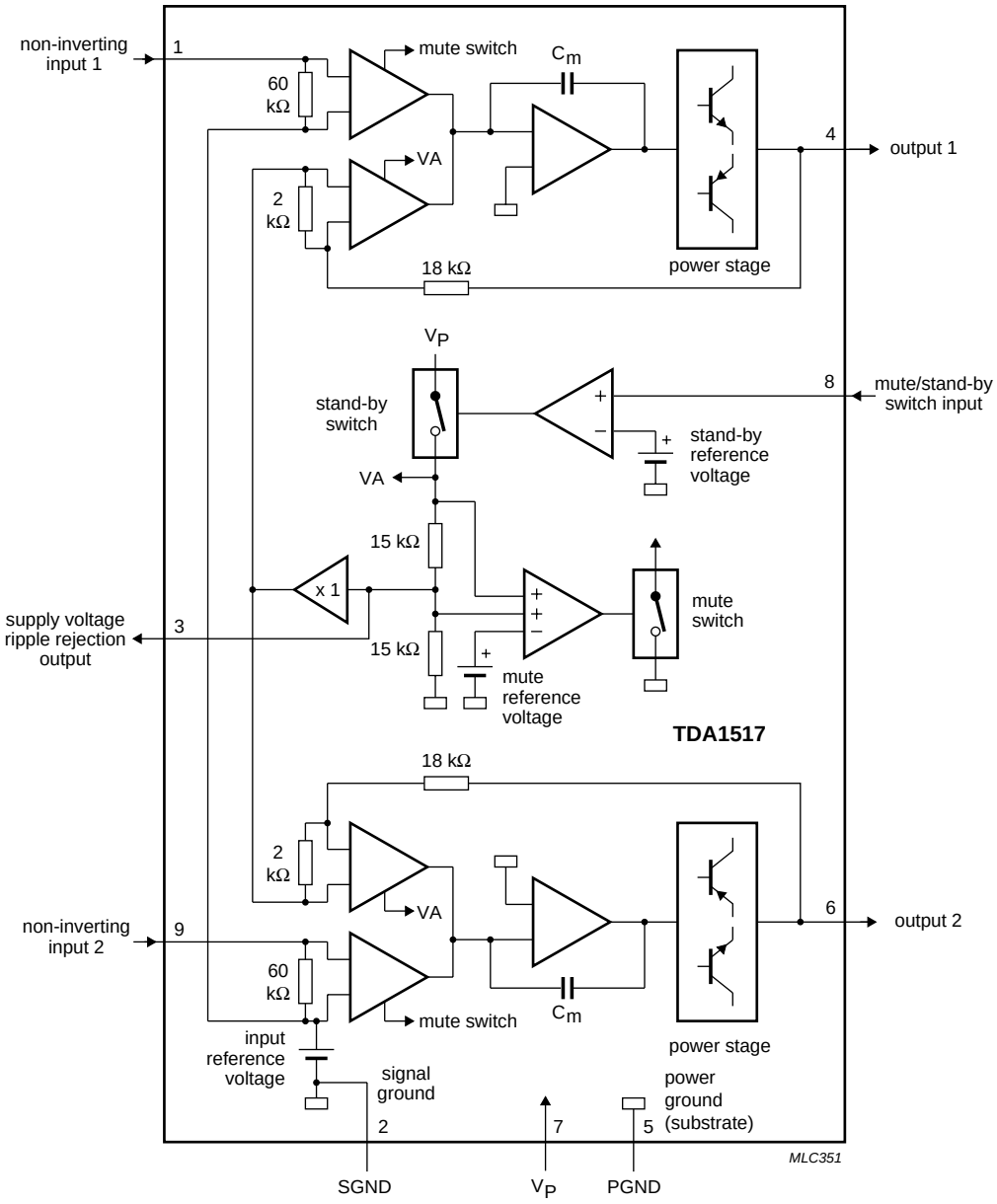


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
–INV1	1	non-inverting input 1
SGND	2	signal ground
SVRR	3	supply voltage ripple rejection output
OUT1	4	output 1
PGND	5	power ground
OUT2	6	output 2
V_P	7	supply voltage
M/SS	8	mute/standby switch input
–INV2	9	non-inverting input 2

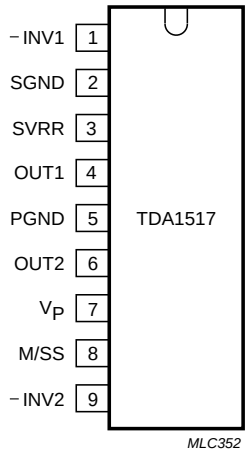
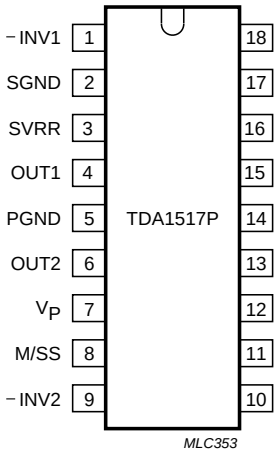


Fig.2 Pin configuration for SOT110-1 and SOT352-1.



Pins 10 to 18 should be connected to GND or floating.

Fig.3 Pin configuration for SOT398-1.

FUNCTIONAL DESCRIPTION

The TDA1517 contains two identical amplifiers with differential input stages. The gain of each amplifier is fixed at 20 dB. A special feature of the device is the mute/standby switch which has the following features:

- Low standby current (<100 μA)
- Low mute/standby switching current (low cost supply switch)
- Mute condition.

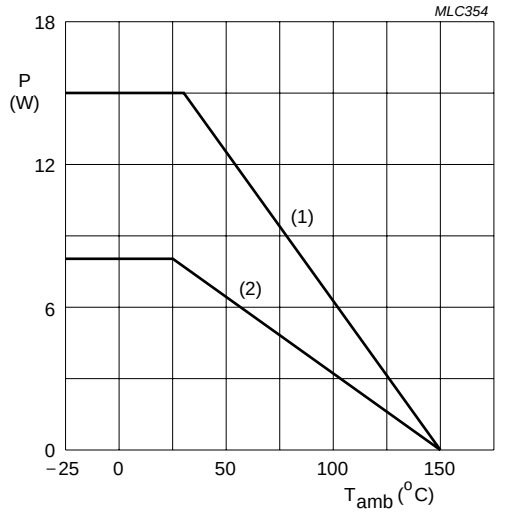
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage	operating	–	18	V
		no signal	–	20	V
$V_{P(sc)}$	AC and DC short-circuit safe voltage		–	18	V
$V_{P(r)}$	reverse polarity		–	6	V
ERG_O	energy handling capability at outputs	V_P = 0 V	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	4	A
I_{ORM}	repetitive peak output current		–	2.5	A
P_{tot}	total power dissipation	see Fig.4	–	15	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_c	crystal temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	TYPE NUMBER	PARAMETER	VALUE	UNIT
$R_{th(j-c)}$	TDA1517/N3; TDA1517/N3/S5	thermal resistance from junction to case	8	K/W
$R_{th(j-p)}$	TDA1517P	thermal resistance from junction to pins	15	K/W
$R_{th(j-a)}$	TDA1517/N3; TDA1517/N3/S5; TDA1517P	thermal resistance from junction to ambient	50	K/W



(1) $R_{th\ j-c}$ = 8 K/W.
(2) $R_{th\ j-p}$ = 15 K/W.

Fig.4 Power derating curve.

DC CHARACTERISTICS

V_P = 14.4 V; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	14.4	18.0	V
$I_{q(tot)}$	total quiescent current		–	40	80	mA
V_O	DC output voltage		–	6.95	–	V
Mute/standby switch						
V_8	switch-on voltage level	see Fig.5	8.5	–	–	V
Mute condition						
V_O	output signal in mute position	$V_{I(max)}$ = 1 V; f_i = 20 Hz to 15 kHz	–	–	2	mV
Standby condition						
I_{sb}	DC current in standby condition		–	–	100	μA
V_{sw}	switch-on current		–	12	40	μA

Note

1. The circuit is DC adjusted at V_P = 6 to 18 V and AC operating at V_P = 8.5 to 18 V.

AC CHARACTERISTICS

V_P = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 0.5%; note 1	4	5	–	W
		THD = 10%; note 1	5.5	6.0	–	W
THD	total harmonic distortion	P_o = 1 W	–	0.1	–	%
f_{lr}	low frequency roll-off	at −3 dB; note 2	–	45	–	Hz
f_{hr}	high frequency roll-off	at −1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB
SVRR	supply voltage ripple rejection	note 3				
	on		48	–	–	dB
	mute		48	–	–	dB
	standby		80	–	–	dB
$\|Z_i\|$	input impedance		50	60	75	kΩ
V_{no}	noise output voltage					
	on	R_S = 0 Ω; note 4	–	50	–	μV
	on	R_S = 10 Ω; note 4	–	70	100	μV
	mute	note 5	–	50	–	μV
α_{cs}	channel separation	R_S = 10 Ω	40	–	–	dB
$\|\Delta G_v\|$	channel unbalance		–	0.1	1	dB

Notes

1. Output power is measured directly at the output pins of the IC.
2. Frequency response externally fixed.
3. Ripple rejection measured at the output with a source impedance of 0 Ω, maximum ripple amplitude of 2 V (p-p) and a frequency between 100 Hz and 10 kHz.
4. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
5. Noise output voltage independent of R_S (V_I = 0 V).

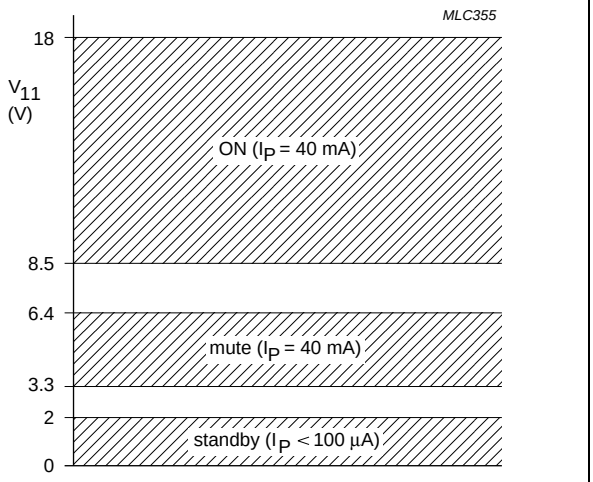


Fig.5 Standby, mute and on conditions.

APPLICATION INFORMATION

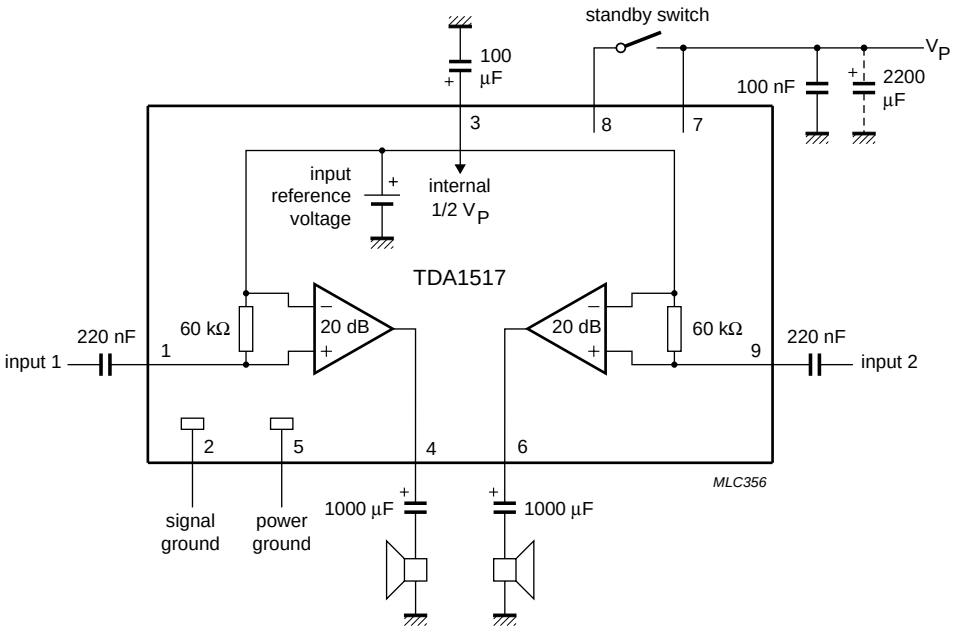
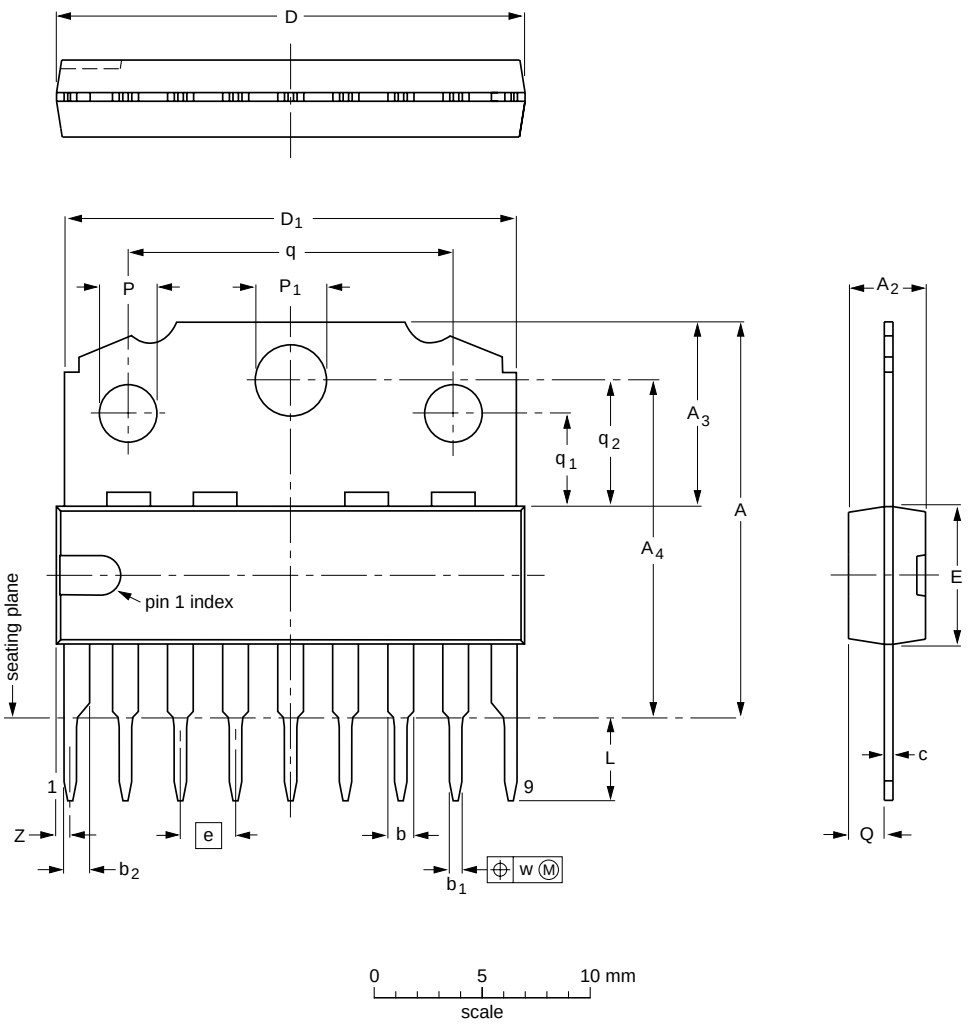


Fig.6 Application circuit diagram.

PACKAGE OUTLINES

SIL9MPF: plastic single in-line medium power package with fin; 9 leads **SOT110-1**



DIMENSIONS (mm are the original dimensions)

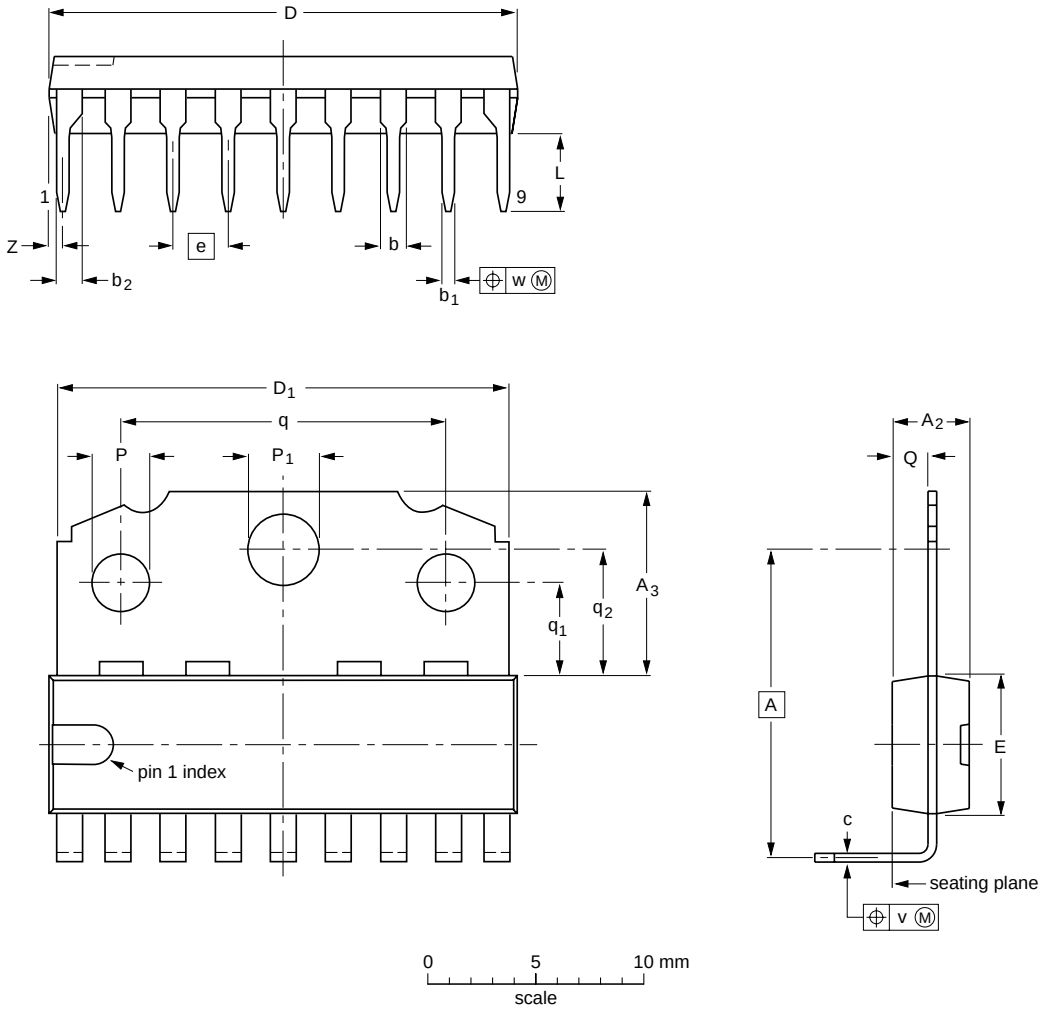
UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	L	P	P_1	Q	q	q_1	q_2	w	$Z^{(1)}$ max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT110-1						~~95-02-25~~ 03-03-12

RBS9MPF: plastic rectangular-bent single in-line medium power package with fin; 9 leads **SOT352-1**



DIMENSIONS (mm are the original dimensions)

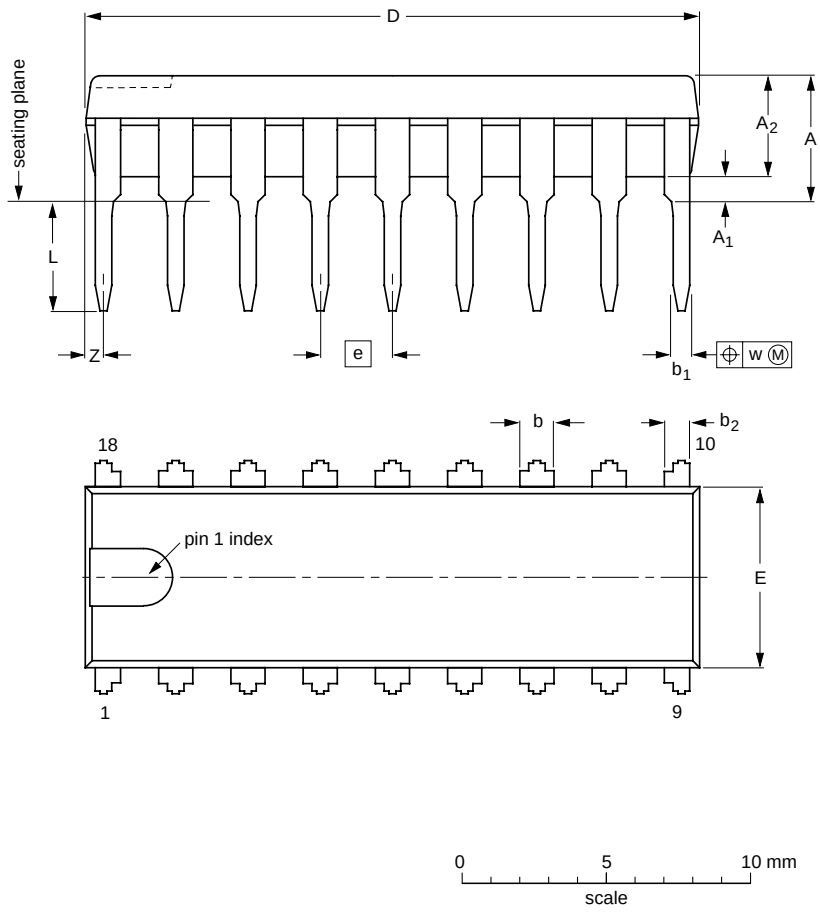
UNIT	A(1)	A2 max.	A3	b	b1	b2	c	D(2)	D1	E(2)	e	L	P	P1	Q	q	q1	q2	v	w	Z(2) max.
mm	14.45 13.95	3.7	8.7 8.0	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.8 3.3	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.6	0.25	1

Notes

1. Dimension is specified at seating plane.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT352-1						~~97-12-16~~ 03-03-12

HDIP18: plastic heat-dissipating dual in-line package; 18 leads **SOT398-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.67 0.50	1.05 0.75	0.47 0.38	21.85 21.35	6.5 6.2	2.54	7.62	3.9 3.1	8.32 8.02	8.7 7.7	0.25	1
inches	0.19	0.02	0.15	0.06 0.04	0.03 0.02	0.04 0.03	0.02 0.01	0.87 0.84	0.26 0.24	0.1	0.3	0.15 0.12	0.33 0.32	0.34 0.30	0.01	0.04

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT398-1						~~95-01-25~~ 03-02-13

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
CPGA, HCPGA	–	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	–	not suitable

Notes

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
2. For PMFP packages hot bar soldering or manual soldering is suitable.

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
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