SC18IS602B

I²C-bus to SPI bridge

Rev. 7 — 21 October 2019 Product data sheet

1. General description

The SC18IS602B is designed to serve as an interface between a standard I²C-bus of a microcontroller and an SPI bus. This allows the microcontroller to communicate directly with SPI devices through its I²C-bus. The SC18IS602B operates as an I²C-bus slave-transmitter or slave-receiver and an SPI master. The SC18IS602B controls all the SPI bus-specific sequences, protocol, and timing. The SC18IS602B has its own internal oscillator, and it supports four SPI chip select outputs that may be configured as GPIO when not used.

2. Features and benefits

- I²C-bus slave interface operating up to 400 kHz
- SPI master operating up to 1.8 Mbit/s
- 200-byte data buffer
- Up to four slave select outputs
- Up to four programmable I/O pins
- Operating supply voltage: 2.4 V to 3.6 V
- Low power mode
- Internal oscillator option
- Active LOW interrupt output
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 that exceeds 100 mA
- Very small 16-pin TSSOP

3. Applications

- Converting I²C-bus to SPI
- Adding additional SPI bus controllers to an existing system

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SC18IS602BIPW/S8	IS602B	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

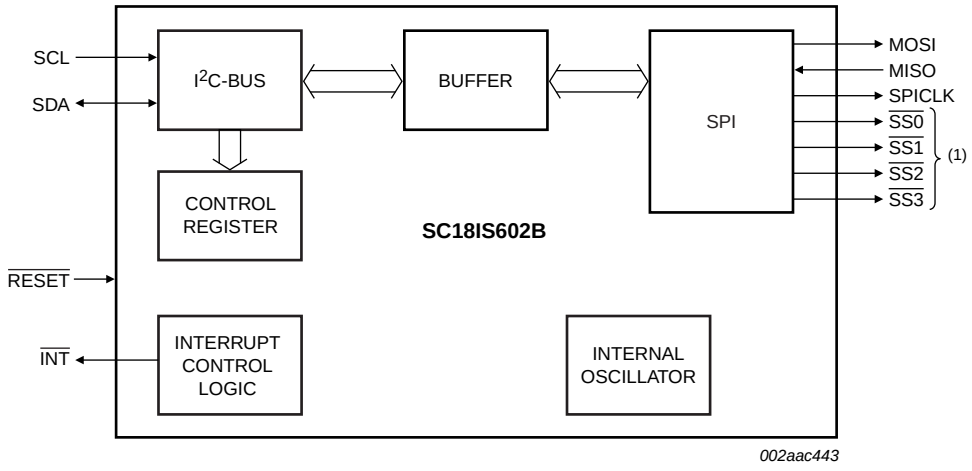
4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SC18IS602BIPW/S8	SC18IS602BIPW/S8HP[1]	TSSOP16	REEL 13" Q4/T2 *STANDARD MARK SMD	2500	T_{amb} = –40 °C to +85 °C

[1] NXP plans to supply the /S8 device with an expected discontinuation in the 2024-2025 timeframe, but in the meantime, Failure Analysis for /S8 devices will consist of Automated Test Equipment (ATE) and electrical overstress verification along with package and wire bond validation only. Detailed device failure analysis will not be available; refer to CIN 201708035I.

5. Block diagram



(1) Unused slave select outputs may be used for GPIO.

Fig 1. Block diagram of SC18IS602B

6. Pinning information

6.1 Pinning

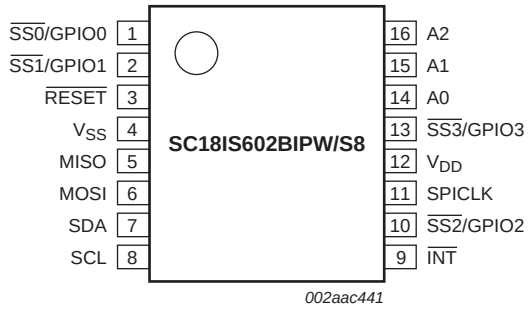


Fig 2. Pin configuration for TSSOP16

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
$\overline{SS0}$/GPIO0	1	I/O	SPI slave select output 0 (active LOW) or GPIO 0
$\overline{SS1}$/GPIO1	2	I/O	SPI slave select output 1 (active LOW) or GPIO 1
$\overline{RESET}$	3	I	reset input (active LOW)
V_{SS}	4	-	ground supply
MISO	5	I	Master In, Slave Out
MOSI	6	O	Master Out, Slave In
SDA	7	I/O	I²C-bus data
SCL	8	I	I²C-bus clock
$\overline{INT}$	9	O	Interrupt output (active LOW). This pin is an open-drain pin.
$\overline{SS2}$/GPIO2	10	I/O	SPI slave select output 2 (active LOW) or GPIO 2
SPICLK	11	O	SPI clock
V_{DD}	12	-	supply voltage
$\overline{SS3}$/GPIO3	13	I/O	SPI slave select output 3 (active LOW) or GPIO 3
A0	14	I	address input 0
A1	15	I	address input 1
A2	16	I	address input 2

7. Functional description

The SC18IS602B acts as a bridge between an I²C-bus and an SPI interface. It allows an I²C-bus master device to communicate with any SPI-enabled device.

7.1 I²C-bus interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes

A typical I²C-bus configuration is shown in Figure 3. (Refer to NXP Semiconductors *UM10204, "I²C-bus specification and user manual"*, at www.nxp.com/documents/user_manual/UM10204.pdf.)

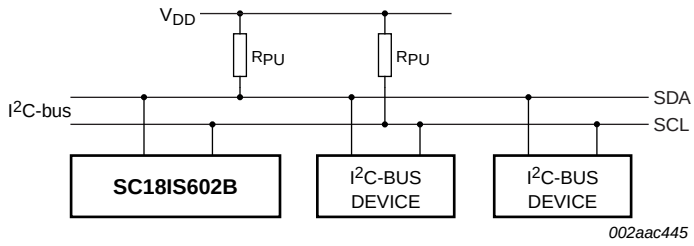


Fig 3. I²C-bus configuration

The SC18IS602B device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz. When the I²C-bus master is reading data from SC18IS602B, the device will be a slave-transmitter. The SC18IS602B will be a slave-receiver when the I²C-bus master is sending data. At no time does the SC18IS602B act as an I²C-bus master, however, it does have the ability to hold the SCL line LOW between bytes to complete its internal processes.

7.1.1 Addressing

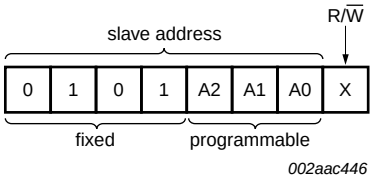


Fig 4. Slave address

The first seven bits of the first byte sent after a START condition defines the slave address of the device being accessed on the bus. The eighth bit determines the direction of the message. A '0' in the least significant position of the first byte means that the master will write information to a selected slave. A '1' in this position means that the master will read information from the slave. When an address is sent, each device in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the master as a slave-receiver or slave-transmitter, depending on the R/$\overline{W}$ bit.

A slave address of the SC18IS602B is comprised of a fixed and a programmable part. The programmable part of the slave address enables the maximum possible number of such devices to be connected to the I²C-bus. Since the SC18IS602B has three programmable address bits (defined by the A2, A1, and A0 pins), it is possible to have eight of these devices on the same bus.

The state of the A2, A1, and A0 pins are latched at reset. Changes made after reset will not alter the address.

When SC18IS602B is busy after the address byte is transmitted, it will not acknowledge its address.

7.1.2 Write to data buffer

All communications to or from the SC18IS602B occur through the data buffer. The data buffer is 200 bytes deep. A message begins with the SC18IS602B address, followed by the Function ID. Depending upon the Function ID, zero to 200 data bytes can follow.

The SC18IS602B will place the data received into a buffer and continue loading the buffer until a STOP condition is received. After the STOP condition is detected, further communications will not be acknowledged until the function designated by the Function ID has been completed.

Fig 5. Write to data buffer

7.1.3 SPI read and write - Function ID 01h to 0Fh

Data in the buffer will be sent to the SPI port if the Function ID is 01h to 0Fh. The Function ID contains the Slave Select (SS) to be used for the transmission on the SPI port. There are four Slave Selects that can be used, with each SS being selected by one of the bits in

the Function ID. There is no restriction on the number or combination of Slave Selects that can be enabled for an SPI message. If more than one $\overline{SSn}$ pin is enabled at one time, the user should be aware of possible contention on the data outputs of the SPI slave devices.

Table 4. Function ID 01h to 0Fh

7	6	5	4	3	2	1	0
0	0	0	0	SS3	SS2	SS1	SS0

The data on the SPI port will contain the same information as the I²C-bus data, but without the slave address and Function ID. For example, if the message shown in Figure 6 is transmitted on the I²C-bus, the SPI bus will send the message shown in Figure 7.

Fig 6. I²C-bus message

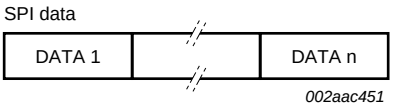


Fig 7. SPI message

The SC18IS602B counts the number of data bytes sent to the I²C-bus port and will automatically send this same number of bytes to the SPI bus. As the data is transmitted from the MOSI pin, it is also read from the MISO pin and saved in the data buffer. Therefore, the old data in the buffer is overwritten. The data in the buffer can then be read back.

If the data from the SPI bus needs to be returned to the I²C-bus master, the process must be completed by reading the data buffer. Section 8 gives an example of an SPI read.

7.1.4 Read from buffer

A read from the data buffer requires no Function ID. The slave address with the R/$\overline{W}$ bit set to a '1' will cause the SC18IS602B to send the buffer contents to the I²C-bus master. The buffer contents are not modified during the read process.

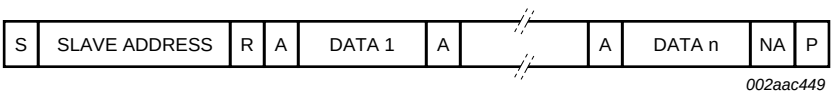


Fig 8. Read from buffer

A typical write and read from an SPI EEPROM is shown in Section 8.

7.1.5 Configure SPI Interface - Function ID F0h

The SPI hardware operating mode, data direction, and frequency can be changed by sending a 'Configure SPI Interface' command to the I²C-bus.

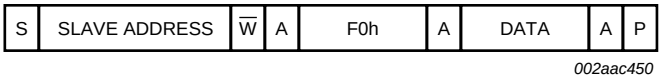


Fig 9. Configure SPI Interface

After the SC18IS602B address is transmitted on the bus, the Configure SPI Interface Function ID (F0h) is sent followed by a byte which will define the SPI communications.

The Clock Phase bit (CPHA) allows the user to set the edges for sampling and changing data. The Clock Polarity bit (CPOL) allows the user to set the clock polarity. Figure 19 and Figure 20 show the different settings of Clock Phase bit CPHA.

Table 5. Configure SPI Interface (F0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	ORDER	X	MODE1	MODE0	F1	F0
Reset	X	X	0	X	0	0	0	0

Table 6. Configure SPI Interface (F0h) bit description

Bit	Symbol	Description
7:6	-	reserved
5	ORDER	When logic 0, the MSB of the data word is transmitted first. If logic 1, the LSB of the data word is transmitted first.
4	-	reserved
3:2	MODE1:MODE0	Mode selection 00 - SPICLK LOW when idle; data clocked in on leading edge (CPOL = 0, CPHA = 0) 01 - SPICLK LOW when idle; data clocked in on trailing edge (CPOL = 0, CPHA = 1) 10 - SPICLK HIGH when idle; data clocked in on trailing edge (CPOL = 1, CPHA = 0) 11 - SPICLK HIGH when idle; data clocked in on leading edge (CPOL = 1, CPHA = 1)
1:0	F1:F0	SPI clock rate 00 - 1843 kHz 01 - 461 kHz 10 - 115 kHz 11 - 58 kHz

7.1.6 Clear Interrupt - Function ID F1h

An interrupt is generated by the SC18IS602B after any SPI transmission has been completed. This interrupt can be cleared ($\overline{INT}$ pin HIGH) by sending a 'Clear Interrupt' command. It is not necessary to clear the interrupt; when polling the device, this function may be ignored.

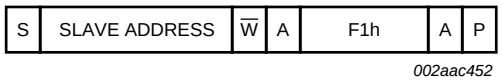


Fig 10. Clear Interrupt

7.1.7 Idle mode - Function ID F2h

A low-power mode may be entered by sending the 'Idle Mode' command.

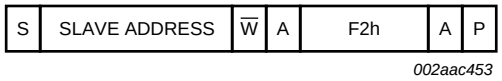


Fig 11. Idle mode

The Idle mode will be exited when its I²C-bus address is detected.

7.1.8 GPIO Write - Function ID F4h

The state of the pins defined as GPIO may be changed using the Port Write function.

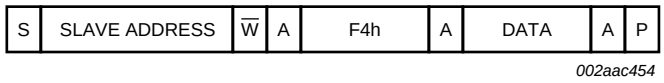


Fig 12. GPIO Write

The data byte following the F4h command will determine the state of SS3, SS2, SS1, and SS0, if they are configured as GPIO. The Port Enable function will define if these pins are used as SPI Slave Selects or if they are GPIO.

Table 7. GPIO Write (F0h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	X	SS3	SS2	SS1	SS0
Reset	X	X	X	X	0	0	0	0

7.1.9 GPIO Read - Function ID F5h

The state of the pins defined as GPIO may be read into the SC18IS602B data buffer using the GPIO Read function.

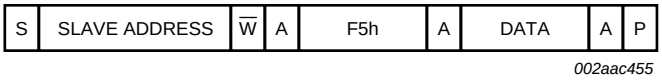


Fig 13. GPIO Read

Note that this function does not return the value of the GPIO. To receive the GPIO contents, a one-byte Read Buffer command would be required. The value of the Read Buffer command will return the following byte.

Table 8. GPIO Read (F5h) bit allocation

7	6	5	4	3	2	1	0
X	X	X	X	SS3	SS2	SS1	SS0

Data for pins not defined as GPIO are undefined.

A GPIO Read is always performed to update the GPIO data in the buffer. The buffer is undefined after the GPIO data is read back from the buffer. Therefore, reading data from the GPIO always requires a two-message sequence (GPIO Read, followed by Read Buffer).

7.1.10 GPIO Enable - Function ID F6h

At reset, the Slave Select pins ($\overline{SS0}$, $\overline{SS1}$, $\overline{SS2}$ and $\overline{SS3}$) are configured to be used as slave select outputs. If these pins are not required for the SPI functions, they can be used as GPIO after they are enabled as GPIO. Any combination of pins may be configured to function as GPIO or Slave Selects.

After the GPIO Enable function is sent, the ports defined as GPIO will be configured as quasi-bidirectional.

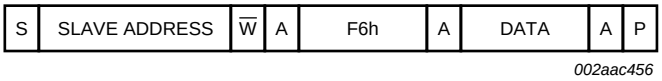


Fig 14. GPIO Enable

The data byte following the F6h command byte will determine which pins can be used as GPIO. A logic 1 will enable the pin as a GPIO, while a logic 0 will disable GPIO control.

Table 9. GPIO Enable (F6h) bit allocation

7	6	5	4	3	2	1	0
X	X	X	X	SS3	SS2	SS1	SS0

7.1.11 GPIO Configuration - Function ID F7h

The pins defined as GPIO may be configured by software to one of four types on a pin-by-pin basis. These are: quasi-bidirectional, push-pull, open-drain, and input-only.

Two bits select the output type for each port pin.

Table 10. GPIO Configuration (F7h) bit allocation

7	6	5	4	3	2	1	0
SS3.1	SS3.0	SS2.1	SS2.0	SS1.1	SS1.0	SS0.1	SS0.0

Table 11. GPIO Configuration (F7h) bit description

Bit	Symbol	Description
7	SS3.1	SS3[1:0] = 00: quasi-bidirectional
6	SS3.0	SS3[1:0] = 01: push-pull
		SS3[1:0] = 10: input-only (high-impedance)
		SS3[1:0] = 11: open-drain
5	SS2.1	SS2[1:0] = 00: quasi-bidirectional
4	SS2.0	SS2[1:0] = 01: push-pull
		SS2[1:0] = 10: input-only (high-impedance)
		SS2[1:0] = 11: open-drain
3	SS1.1	SS1[1:0] = 00: quasi-bidirectional
2	SS1.0	SS1[1:0] = 01: push-pull
		SS1[1:0] = 10: input-only (high-impedance)
		SS1[1:0] = 11: open-drain
1	SS0.1	SS0[1:0] = 00: quasi-bidirectional
0	SS0.0	SS0[1:0] = 01: push-pull
		SS0[1:0] = 10: input-only (high-impedance)
		SS0[1:0] = 11: open-drain

The $\overline{SS}$n pins defined as GPIO, for example SS0.0 and SS0.1, may be configured by software to one of four types. These are: quasi-bidirectional, push-pull, open-drain, and input-only. Two configuration bits in GPIO Configuration register for each pin select the type for each pin. A pin has Schmitt-triggered input that also has a glitch suppression circuit.

7.1.11.1 Quasi-bidirectional output configuration

Quasi-bidirectional outputs can be used both as an input and output without the need to reconfigure the pin. This is possible because when the pin outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a large current. There are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

One of these pull-ups, called the ‘very weak’ pull-up, is turned on whenever the port latch for the pin contains a logic 1. This very weak pull-up sources a very small current that will pull the pin HIGH if it is left floating.

A second pull-up, called the ‘weak’ pull-up, is turned on when the port latch for the pin contains a logic 1 and the pin itself is also at a logic 1 level. This pull-up provides the primary source current for a quasi-bidirectional pin that is outputting a 1. If this pin is

pulled LOW by an external device, the weak pull-up turns off, and only the very weak pull-up remains on. In order to pull the pin LOW under these conditions, the external device has to sink enough current to overpower the weak pull-up and pull the pin below its input threshold voltage.

The third pull-up is referred to as the 'strong' pull-up. This pull-up is used to speed up LOW-to-HIGH transitions on a quasi-bidirectional pin when the port latch changes from a logic 0 to a logic 1. When this occurs, the strong pull-up turns on for two CPU clocks quickly pulling the pin HIGH.

The quasi-bidirectional pin configuration is shown in Figure 15.

Although the SC18IS602B is a 3 V device, most of the pins are 5 V tolerant. If 5 V is applied to a pin configured in quasi-bidirectional mode, there will be a current flowing from the pin to V_{DD} causing extra power consumption. Therefore, applying 5 V to pins configured in quasi-bidirectional mode is discouraged.

A quasi-bidirectional pin has a Schmitt-triggered input that also has a glitch suppression circuit.

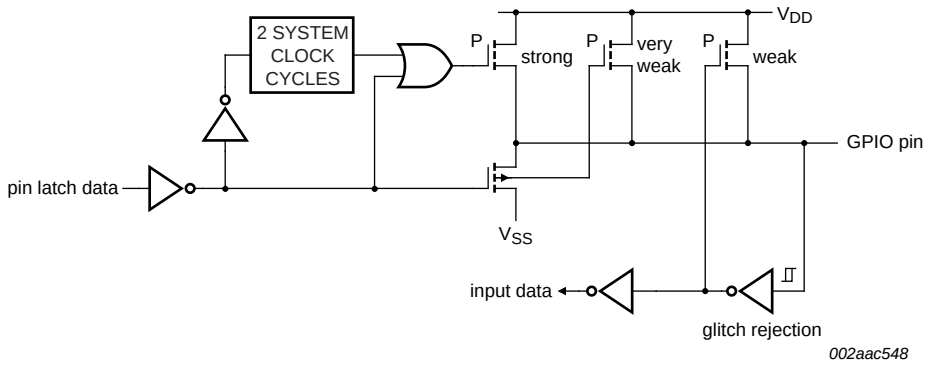


Fig 15. Quasi-bidirectional output configuration

7.1.11.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the pin when the port latch contains a logic 0. To be used as a logic output, a pin configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}. The pull-down for this mode is the same as for the quasi-bidirectional mode.

The open-drain pin configuration is shown in Figure 16.

An open-drain pin has a Schmitt-triggered input that also has a glitch suppression circuit.

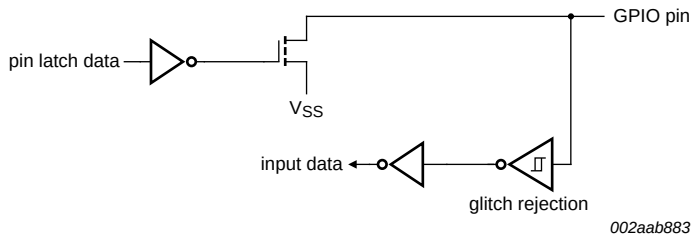


Fig 16. Open-drain output configuration

7.1.11.3 Input-only configuration

The input-only pin configuration is shown in Figure 17. It is a Schmitt-triggered input that also has a glitch suppression circuit.

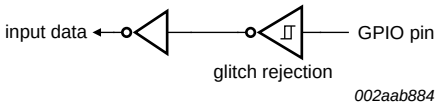


Fig 17. Input-only configuration

7.1.11.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a pin output.

The push-pull pin configuration is shown in Figure 18.

A push-pull pin has a Schmitt-triggered input that also has a glitch suppression circuit.

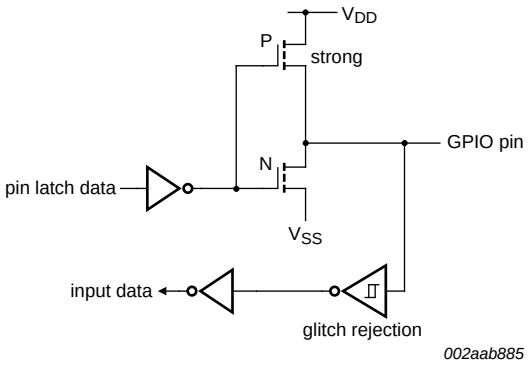


Fig 18. Push-pull output configuration

7.2 SPI interface

The SPI interface can support Mode 0 through Mode 3 of the SPI specification and can operate up to 1.8 Mbit/s. The SPI interface uses at least four pins: SPICLK, MOSI, MISO, and Slave Select ($\overline{SSn}$).

$\overline{SSn}$ are the slave select pins. In a typical configuration, an SPI master selects one SPI device as the current slave.

There are actually four $\overline{SSn}$ pins ($\overline{SS0}$, $\overline{SS1}$, $\overline{SS2}$ and $\overline{SS3}$) to allow the SC18IS602B to communicate with multiple SPI devices.

The SC18IS602B generates the SPICLK (SPI clock) signal in order to send and receive data. The SCLK, MOSI, and MISO are typically tied together between two or more SPI devices. Data flows from the SC18IS602B (master) to slave on the MOSI pin (Pin 6) and the data flows from slave to SC18IS602B (master) on the MISO pin (Pin 5).

8. I²C-bus to SPI communications example

The following example describes a typical sequence of events required to read the contents of an SPI-based EEPROM. This example assumes that the SC18IS602B is configured to respond to address 50h. A START condition is shown as ‘ST’, while a STOP condition is ‘SP’. The data is presented in hexadecimal format.

1. The first message is used to configure the SPI port for mode and frequency.

```
ST,50,F0,02,SP    SPI frequency 115 kHz using Mode 0
```

2. An SPI EEPROM first requires that a Write Enable command be sent before data can be written.

```
ST,50,04,06,SP    EEPROM write enable using SS2, assuming the Write Enable is
                  06h
```

3. Clear the interrupt. This is not required if using a polling method rather than interrupts.

```
ST,50,F1,SP       Clear interrupt
```

4. Write the 8 data bytes. The first byte (Function ID) tells the SC18IS602B which Slave Select output to use. This example uses SS2 (shown as 04h). The first byte sent to the EEPROM is normally 02h for the EEPROM write command. The next one or two bytes represent the subaddress in the EEPROM. In this example, a two-byte subaddress is used. Bytes 00 and 30 would cause the EEPROM to write to subaddress 0030h. The next eight bytes are the eight data bytes that will be written to subaddresses 0030h through 0037h.

```
ST,50,04,02,00,30,01,02,03,04,05,06,07,08,SP     Write 8 bytes using SS2
```

5. When an interrupt occurs, do a Clear Interrupt or wait until the SC18IS602B responds to its I²C-bus address.

```
ST,50,F1,SP       Clear interrupt
```

6. Read the 8 bytes from the EEPROM. Note that we are writing a command, even though we are going to perform a read from the SPI port. The Function ID is again 04h, indicating that we are going to use SS2. The EEPROM requires that you send a 03h for a read, followed by the subaddress you would like to read. We are going to read back the same data previously written, so this means that the subaddress should be 0030h. We would like to read back 8 bytes so we can send eight bytes of FFh to tell the SC18IS602B to send eight more bytes on MOSI. While it is sending these eight data bytes, it is also reading the MISO pin and saving the data in the buffer.

```
ST,50,04,03,00,30,FF,FF,FF,FF,FF,FF,FF,FF,SP     Read 8 bytes using SS2
```

7. The interrupt can be cleared, if needed.

```
ST,50,F1,SP       Clear interrupt
```

8. Read back the data buffer. Note that we will actually need to read back 11 data bytes since the first three bytes sent on the SPI port were the read code (03h) and the two subaddress bytes.

```
ST,50,00,00,00,01,02,03,04,05,06,07,08,SP        Read the data buffer
```

You can see that on the I²C-bus the first four bytes do not contain the data from the SPI bus. The first byte is the SC18IS602B address, followed by three dummy data bytes. These dummy data bytes correspond to the three bytes sent to the EEPROM before it actually places data on the bus (command 03h, subaddress 0030h).

9. Limiting values

Table 12. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1][2]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature	operating	–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
V_n	voltage on any other pin	referenced to V_{SS}	–0.5	+5.5	V
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/O(tot)(max)}$	maximum total I/O current		-	120	mA
P_{tot}/pack	total power dissipation per package	[3]	-	1.5	W

[1] This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

[2] Parameters are valid over the operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[3] Based on package heat transfer, not device power consumption.

10. Static characteristics

Table 13. Static characteristics

V_{DD} = 2.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C (industrial); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f = 7.3728 MHz		-	5.6	6.7	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f = 7.3728 MHz		-	3.3	3.9	mA
$V_{th(HL)}$	HIGH-LOW threshold voltage	Schmitt trigger input		$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	Schmitt trigger input		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	all pins					
		I_{OL} = 20 mA		-	0.6	1.0	V
		I_{OL} = 10 mA		-	0.3	0.5	V
		I_{OL} = 3.2 mA		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	all pins					
		I_{OH} = −8 mA; push-pull mode		$V_{DD} - 1$	-	-	V
		I_{OH} = −3.2 mA; push-pull mode		$V_{DD} - 0.7$	$V_{DD} - 0.4$	-	V
		I_{OH} = −20 µA; quasi-bidirectional mode		$V_{DD} - 0.3$	$V_{DD} - 0.2$	-	V
C_{ig}	input capacitance at gate		[2]	-	-	15	pF
I_{IL}	LOW-level input current	logical 0; V_I = 0.4 V	[3]	-	-	−80	µA
I_{LI}	input leakage current	all ports; $V_I = V_{IL}$ or V_{IH}	[4]	-	-	±10	µA
I_{THL}	HIGH-LOW transition current	all ports; logical 1-to-0; V_I = 2.0 V at V_{DD} = 3.6 V	[5][6]	−30	-	−450	µA
$R_{RESET\_N(int)}$	internal pull-up resistance on pin $\overline{\text{RESET}}$			10	-	30	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] Pin capacitance is characterized but not tested.

[3] Measured with pins in quasi-bidirectional mode.

[4] Measured with pins in high-impedance mode.

[5] Pins in quasi-bidirectional mode with weak pull-up (applies to all pins with pull-ups).

[6] Pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

11. Dynamic characteristics

Table 14. Dynamic characteristics

V_{DD} = 2.4 V to 3.6 V; T_{amb} = −40 °C to +85 °C (industrial); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C	7.189	-	7.557	MHz
Glitch filter						
t_{gr}	glitch rejection time	$\overline{\text{RESET}}$ pin	-	-	50	ns
		any pin except $\overline{\text{RESET}}$	125	-	-	ns
t_{sa}	signal acceptance time	$\overline{\text{RESET}}$ pin	-	-	15	ns
		any pin except $\overline{\text{RESET}}$	50	-	-	ns
SPI master interface						
f_{SPI}	SPI operating frequency	1.843 MHz	-	-	1.843	MHz
T_{SPICYC}	SPI cycle time	1.843 MHz	543	-	-	ns
$t_{SPICLKH}$	SPICLK HIGH time		271	-	-	ns
$t_{SPICLKL}$	SPICLK LOW time		271	-	-	ns
t_{SPIDSU}	SPI data set-up time		100	-	-	ns
t_{SPIDH}	SPI data hold time		100	-	-	ns
t_{SPIDV}	SPI enable to output data valid time		-	-	160	ns
t_{SPIOH}	SPI output data hold time		0	-	-	ns
t_{SPIR}	SPI rise time	SPI outputs (SPICLK, MOSI, MISO)	-	-	100	ns
		SPI inputs (SPICLK, MOSI, MISO, SSn)	-	-	2000	ns
t_{SPIF}	SPI fall time	SPI outputs (SPICLK, MOSI, MISO)	-	-	100	ns
		SPI inputs (SPICLK, MOSI, MISO, SSn)	-	-	2000	ns

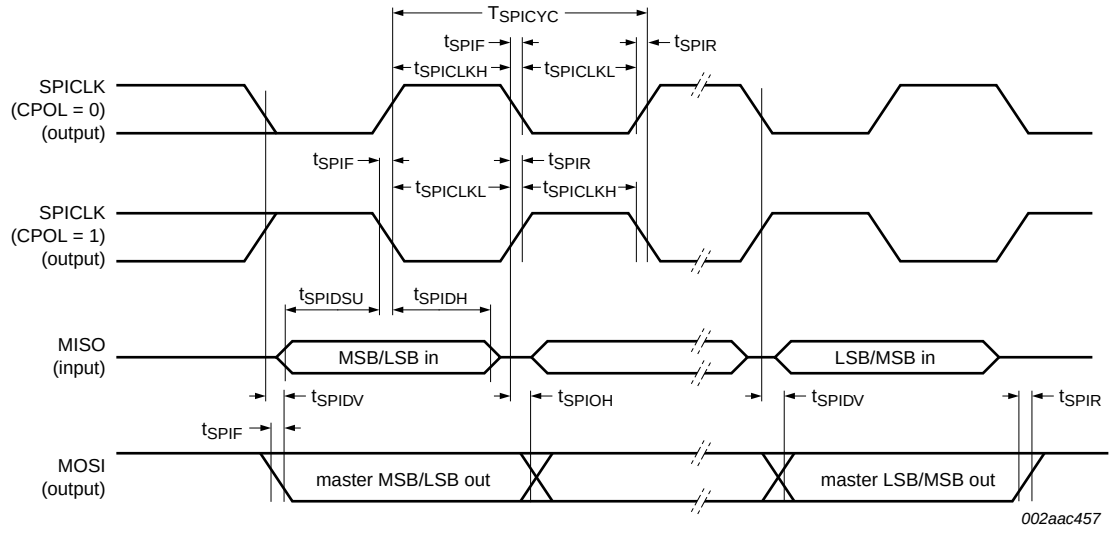


Fig 19. SPI master timing (CPHA = 0)

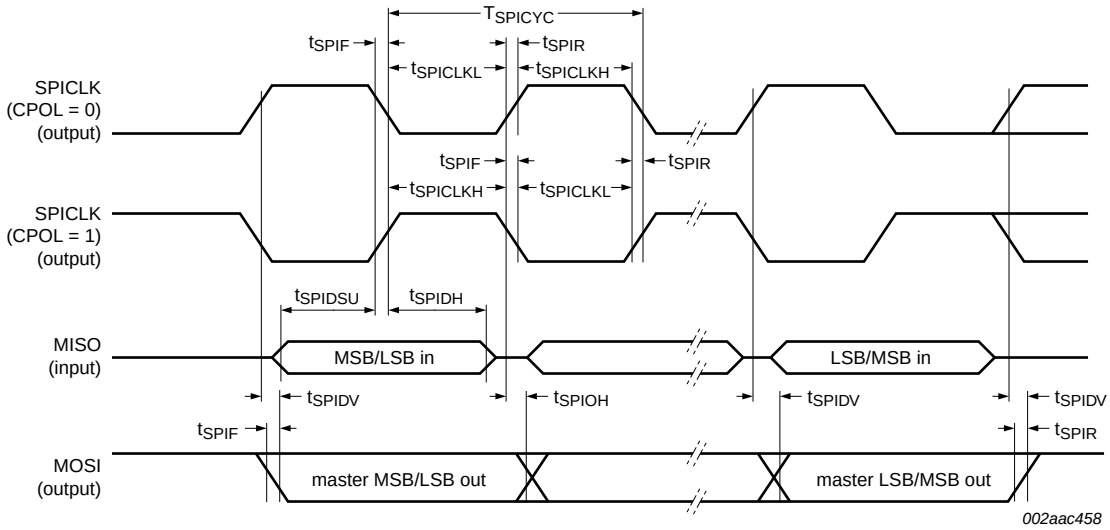
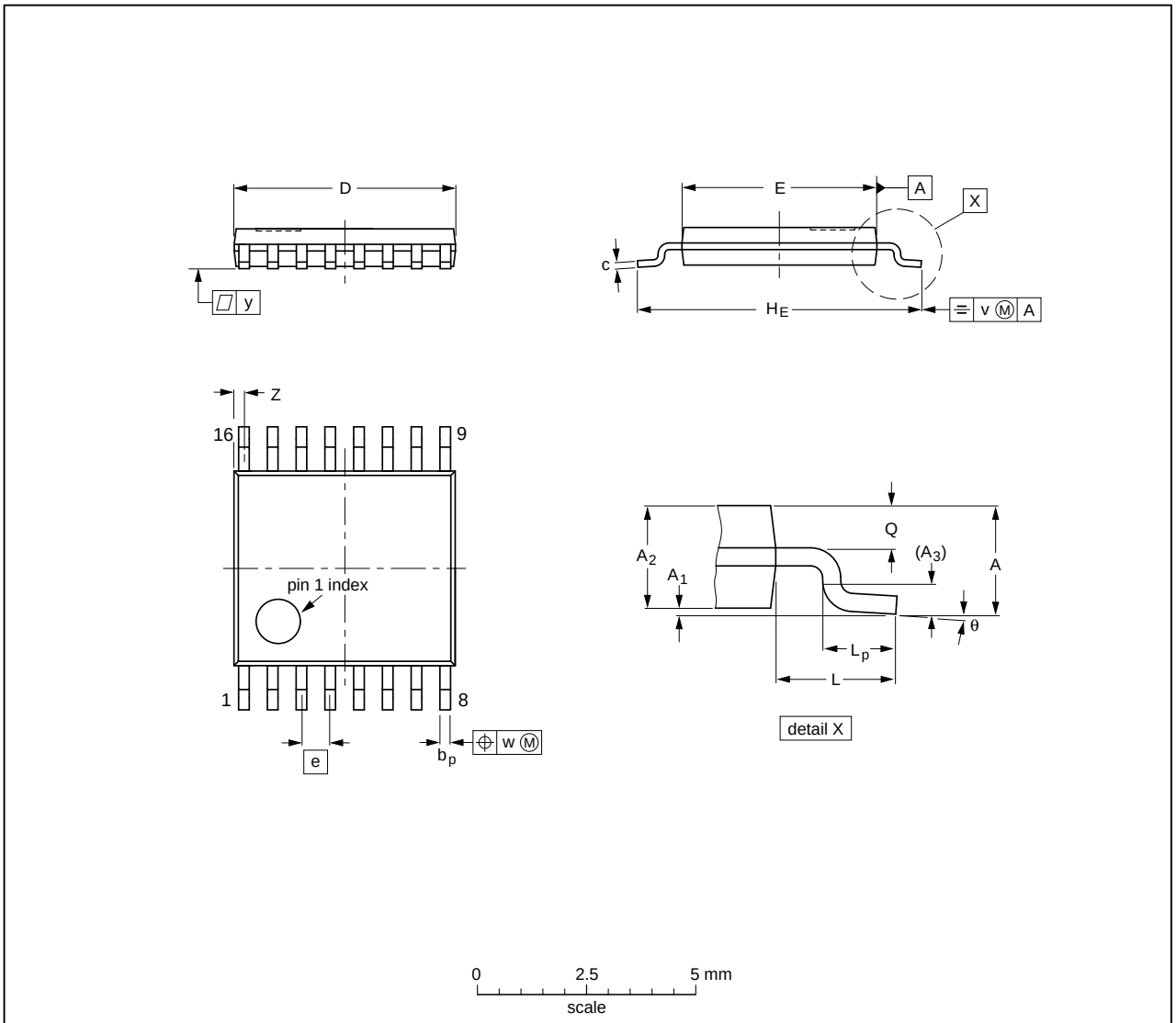


Fig 20. SPI master timing (CPHA = 1)

12. Package outline

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 21. Package outline SOT403-1 (TSSOP16)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 22) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 15 and 16

Table 15. SnPb eutectic process (from J-STD-020C)

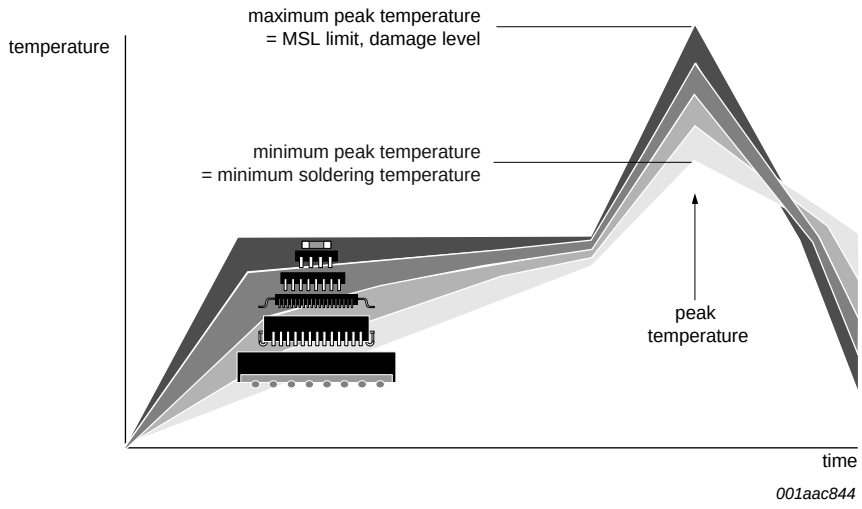
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 16. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 22.



MSL: Moisture Sensitivity Level

Fig 22. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
CPU	Central Processing Unit
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
SPI	Serial Peripheral Interface

15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SC18IS602B v.7	20191021	Product data sheet	-	SC18IS602_602B_603 v.6
Modifications:	• Removed discontinued versions			
SC18IS602B v.6	20171013	Product data sheet	201708035I	SC18IS602_602B_603 v.5.2
Modifications:	• Added SC18IS602B/S8 • Updated Section 4.1 “Ordering options”			
SC18IS602B v.5.2	20161026	Product data sheet	201610010I	SC18IS602_602B_603 v.5.1
Modifications:	• Table 2 “Ordering options”, packing method: Device orientation corrected from Q2/T3 to Q4/T2; no change to device functionality or product identification			
SC18IS602B v.5.1	20150211	Product data sheet	-	SC18IS602_602B_603 v.5
Modifications:	• Table 3 “Pin description”: Added “This pin is an open-drain pin” to $\overline{\text{INT}}$ pin description • Updated Section 4 “Ordering information”			
SC18IS602B v.5	20100803	Product data sheet		SC18IS602_602B_603 v.4
SC18IS602_602B_603 v.4	20080311	Product data sheet	-	SC18IS602_603 v.3
SC18IS602_603 v.3	20070813	Product data sheet	-	SC18IS602_603 v.2
SC18IS602_603 v.2	20061213	Product data sheet	-	SC18IS602_603 v.1
SC18IS602_603 v.1	20060926	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 21 October 2019
Document identifier: SC18IS602B

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