



# PSMN2R6-40YS

N-channel LFPAK 40 V 2.8 m $\Omega$  standard level MOSFET

Rev. 01 — 23 June 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in LFPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LFPAK provides maximum power density in a Power SO8 package

### 1.3 Applications

- DC-to-DC convertors
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference

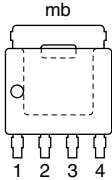
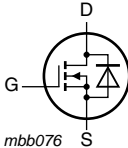
| Symbol                         | Parameter                                    | Conditions  | Min | Typ | Max | Unit |
|--------------------------------|--|---|-----|-----|-----|------|
| V <sub>DS</sub>                | drain-source voltage                         | T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C   | -   | -   | 40  | V    |
| I <sub>D</sub>                 | drain current                                | T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>   | -   | -   | 100 | A    |
| P <sub>tot</sub>               | total power dissipation                      | T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>   | -   | -   | 131 | W    |
| T <sub>j</sub>                 | junction temperature                         |   | -55 | -   | 175 | °C   |
| <b>Avalanche ruggedness</b>    |  |   |     |     |     |      |
| E <sub>DS(AL)S</sub>           | non-repetitive drain-source avalanche energy | V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 40 V; unclamped; R <sub>GS</sub> = 50 $\Omega$ | -   | -   | 179 | mJ   |
| <b>Dynamic characteristics</b> |  |   |     |     |     |      |
| Q <sub>GD</sub>                | gate-drain charge                            | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A;  | -   | 14  | -   | nC   |
| Q <sub>G(tot)</sub>            | total gate charge                            | V <sub>DS</sub> = 20 V; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>   | -   | 63  | -   | nC   |

Table 1. Quick reference

| Symbol                        | Parameter                           | Conditions  | Min | Typ | Max | Unit |
|-------------------------------|-------------------------------------|---|-----|-----|-----|------|
| <b>Static characteristics</b> |                                     |   |     |     |     |      |
| $R_{DS(on)}$                  | drain-source<br>on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$<br>$T_j = 100\text{ °C};$ see <a href="#">Figure 12</a> ;<br>see <a href="#">Figure 13</a> | -   | -   | 3.7 | mΩ   |
|                               |                                     | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$<br>$T_j = 25\text{ °C};$ see <a href="#">Figure 12</a> ;<br>see <a href="#">Figure 13</a>  | -   | 2   | 2.8 | mΩ   |

## 2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline   | Graphic symbol   |
|-----|--------|-------------|--|--|
| 1   | S      | source      |  <p><b>SOT669<br/>(LPAK)</b></p> |  <p><i>mbb076</i></p> |
| 2   | S      | source      |  |  |
| 3   | S      | source      |  |  |
| 4   | G      | gate        |  |  |
| mb  | D      | drain       |  |  |

## 3. Ordering information

Table 3. Ordering information

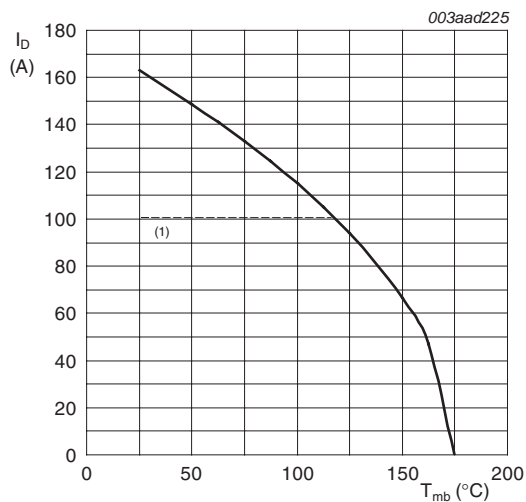
| Type number  | Package |  | Version |
|--------------|---------|--|---------|
|              | Name    | Description  |         |
| PSMN2R6-40YS | LPAK    | plastic single-ended surface-mounted package (LPAK); 4 leads | SOT669  |

## 4. Limiting values

**Table 4. Limiting values**

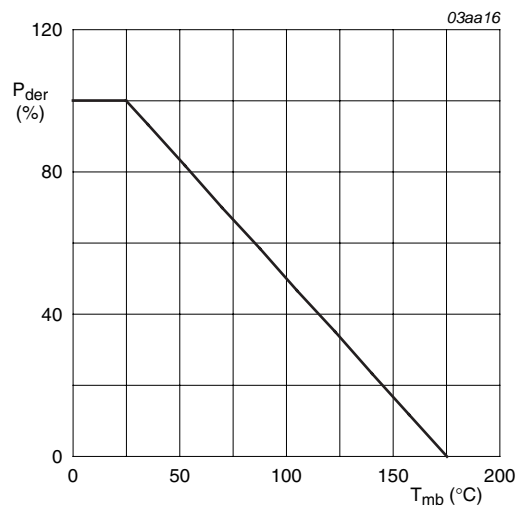
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions  | Min | Max | Unit |
|-----------------------------|--|---|-----|-----|------|
| $V_{DS}$                    | drain-source voltage                         | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$  | -   | 40  | V    |
| $V_{DGR}$                   | drain-gate voltage                           | $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$   | -   | 40  | V    |
| $V_{GS}$                    | gate-source voltage                          |   | -20 | 20  | V    |
| $I_D$                       | drain current                                | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>  | -   | 100 | A    |
|                             |  | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>   | -   | 100 | A    |
| $I_{DM}$                    | peak drain current                           | $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>   | -   | 651 | A    |
| $P_{tot}$                   | total power dissipation                      | $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>  | -   | 131 | W    |
| $T_{stg}$                   | storage temperature                          |   | -55 | 175 | °C   |
| $T_j$                       | junction temperature                         |   | -55 | 175 | °C   |
| $T_{sld(M)}$                | peak soldering temperature                   |   | -   | 260 | °C   |
| <b>Source-drain diode</b>   |  |   |     |     |      |
| $I_S$                       | source current                               | $T_{mb} = 25\text{ °C}$   | -   | 100 | A    |
| $I_{SM}$                    | peak source current                          | $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$  | -   | 651 | A    |
| <b>Avalanche ruggedness</b> |  |   |     |     |      |
| $E_{DS(AL)S}$               | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 100\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; unclamped; $R_{GS} = 50\text{ }\Omega$ | -   | 179 | mJ   |



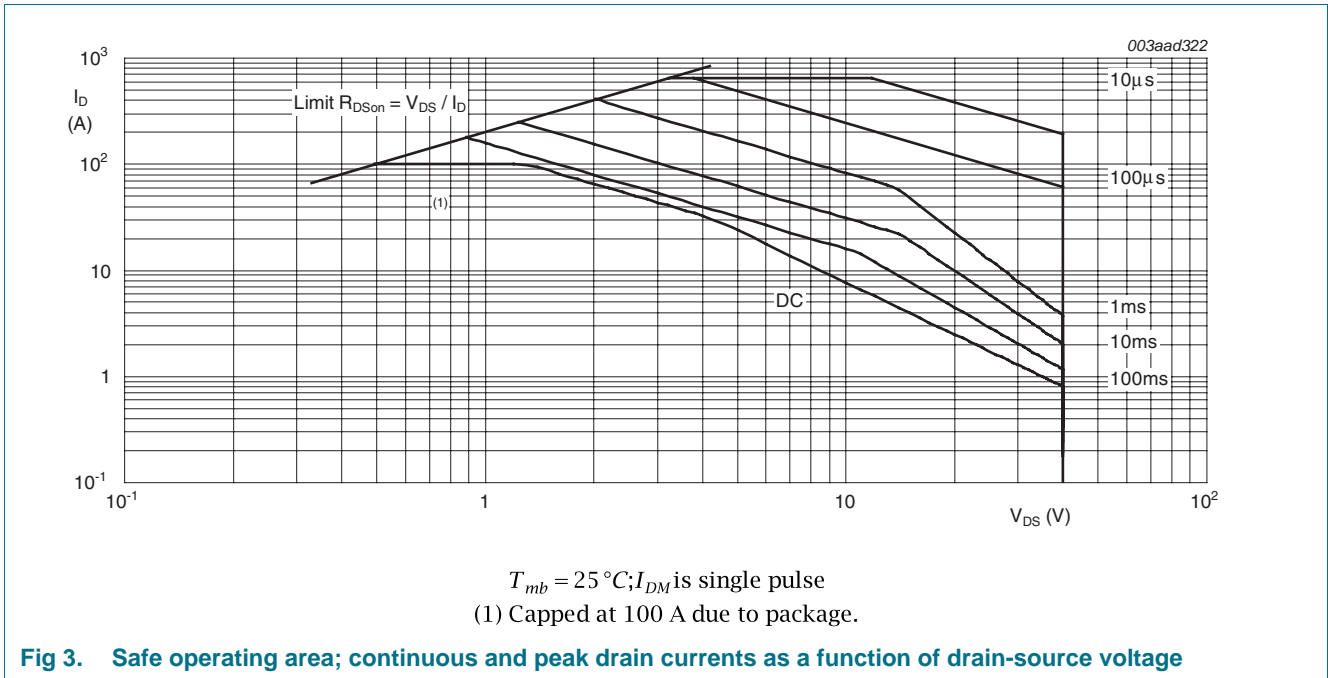
$V_{GS} \geq 5\text{ V}$ (1) Capped at 100A due to package

**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ °C})}} \times 100\%$$

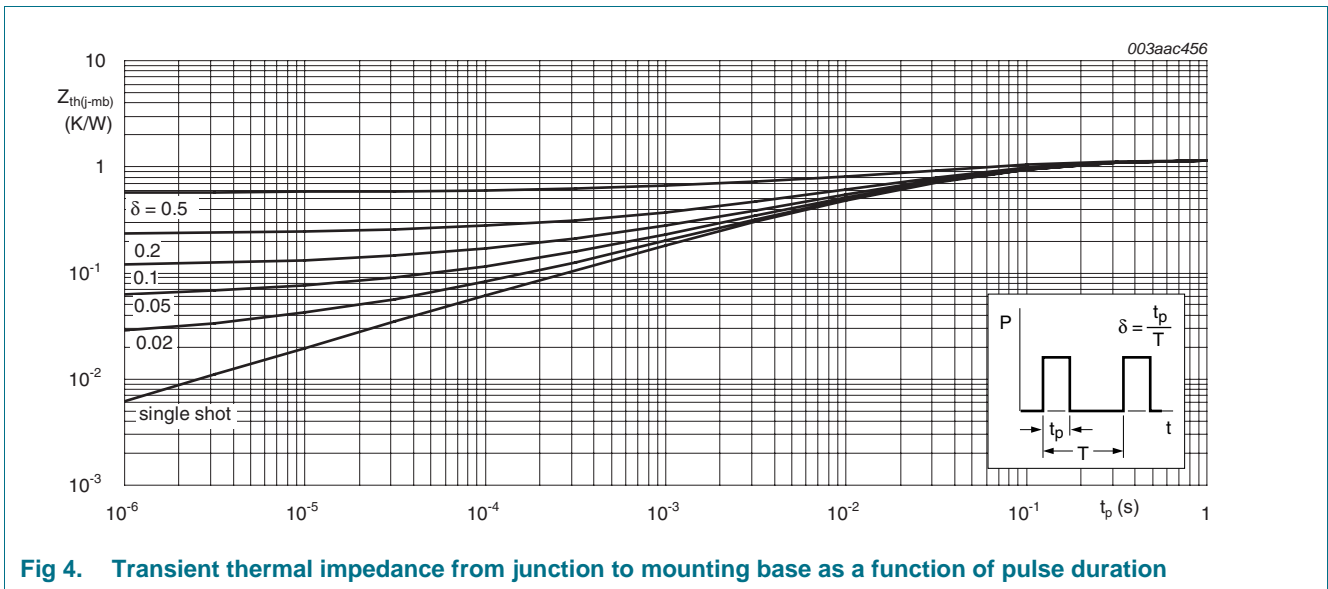
**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



## 5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol         | Parameter   | Conditions                   | Min | Typ | Max  | Unit |
|----------------|---|------------------------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 4</a> | -   | 0.5 | 1.15 | K/W  |



## 6. Characteristics

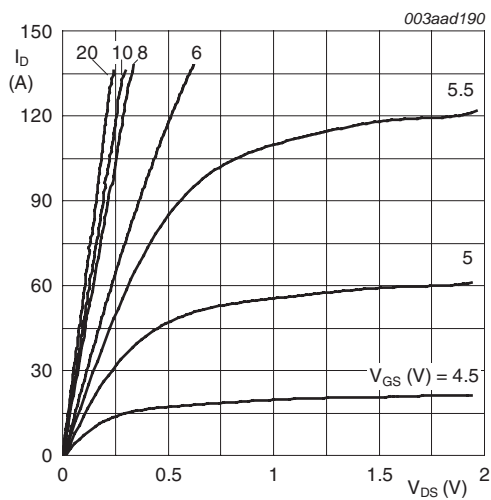
**Table 6. Characteristics**

| Symbol                         | Parameter                         | Conditions  | Min | Typ  | Max | Unit          |
|--------------------------------|-----------------------------------|---|-----|------|-----|---------------|
| <b>Static characteristics</b>  |                                   |   |     |      |     |               |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage    | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$   | 36  | -    | -   | V             |
|                                |                                   | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | 40  | -    | -   | V             |
| $V_{GS(th)}$                   | gate-source threshold voltage     | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>       | -   | -    | 4.6 | V             |
|                                |                                   | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>       | 1   | -    | -   | V             |
|                                |                                   | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>        | 2   | 3    | 4   | V             |
| $I_{DSS}$                      | drain leakage current             | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -   | -    | 4   | $\mu\text{A}$ |
|                                |                                   | $V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$   | -   | -    | 50  | $\mu\text{A}$ |
| $I_{GSS}$                      | gate leakage current              | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -   | -    | 100 | nA            |
|                                |                                   | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -   | -    | 100 | nA            |
| $R_{DS(on)}$                   | drain-source on-state resistance  | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 12</a>                                 | -   | -    | 5.3 | mΩ            |
|                                |                                   | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a> | -   | -    | 3.7 | mΩ            |
|                                |                                   | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$<br>see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>  | -   | 2    | 2.8 | mΩ            |
| $R_G$                          | internal gate resistance (AC)     | $f = 1 \text{ MHz}$   | -   | 0.7  | -   | Ω             |
| <b>Dynamic characteristics</b> |                                   |   |     |      |     |               |
| $Q_{G(tot)}$                   | total gate charge                 | $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$  | -   | 50   | -   | nC            |
|                                |                                   | $I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$<br>see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>            | -   | 63   | -   | nC            |
| $Q_{GS}$                       | gate-source charge                | $I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 10 \text{ V};$<br>see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>            | -   | 18   | -   | nC            |
| $Q_{GS(th)}$                   | pre-threshold gate-source charge  |   | -   | 12   | -   | nC            |
| $Q_{GS(th-pl)}$                | post-threshold gate-source charge |   | -   | 6    | -   | nC            |
| $Q_{GD}$                       | gate-drain charge                 |   | -   | 14   | -   | nC            |
| $V_{GS(pl)}$                   | gate-source plateau voltage       | $I_D = 25 \text{ A}; V_{DS} = 20 \text{ V};$ see <a href="#">Figure 14</a> ;<br>see <a href="#">Figure 15</a>                                   | -   | 4.4  | -   | V             |
| $C_{iss}$                      | input capacitance                 | $V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$<br>$T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>           | -   | 3776 | -   | pF            |
| $C_{oss}$                      | output capacitance                |   | -   | 948  | -   | pF            |
| $C_{rss}$                      | reverse transfer capacitance      |   | -   | 457  | -   | pF            |
| $t_{d(on)}$                    | turn-on delay time                | $V_{DS} = 12 \text{ V}; R_L = 0.5 \text{ } \Omega; V_{GS} = 10 \text{ V};$<br>$R_{G(ext)} = 4.7 \text{ } \Omega$                                | -   | 24   | -   | ns            |
| $t_r$                          | rise time                         |   | -   | 22   | -   | ns            |
| $t_{d(off)}$                   | turn-off delay time               |   | -   | 46   | -   | ns            |
| $t_f$                          | fall time                         |   | -   | 15   | -   | ns            |

Table 6. Characteristics ...continued

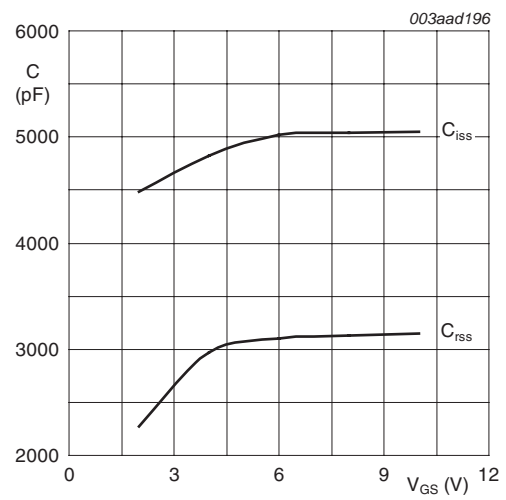
| Symbol                    | Parameter             | Conditions   | Min | Typ  | Max | Unit |
|---------------------------|-----------------------|--|-----|------|-----|------|
| <b>Source-drain diode</b> |                       |  |     |      |     |      |
| $V_{SD}$                  | source-drain voltage  | $I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ;<br>see <a href="#">Figure 17</a>                                  | -   | 0.78 | 1.2 | V    |
| $t_{rr}$                  | reverse recovery time | $I_S = 50\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;<br>$V_{DS} = 20\text{ V}$                        | -   | 45   | -   | ns   |
| $Q_r$                     | recovered charge      | $I_S = 50\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;<br>$V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$ | -   | 47   | -   | nC   |

[1] Tested to JEDEC standards where applicable.



$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

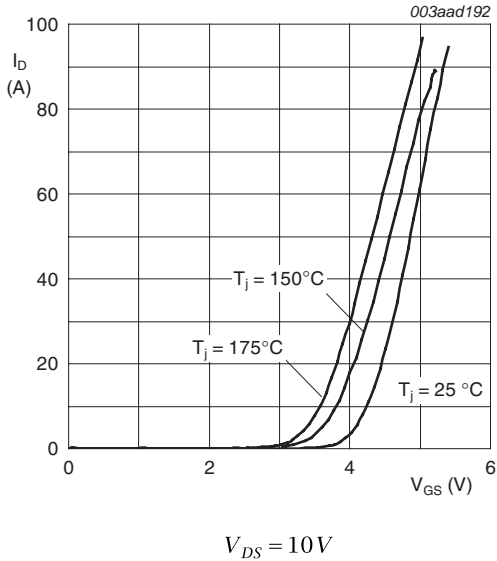


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

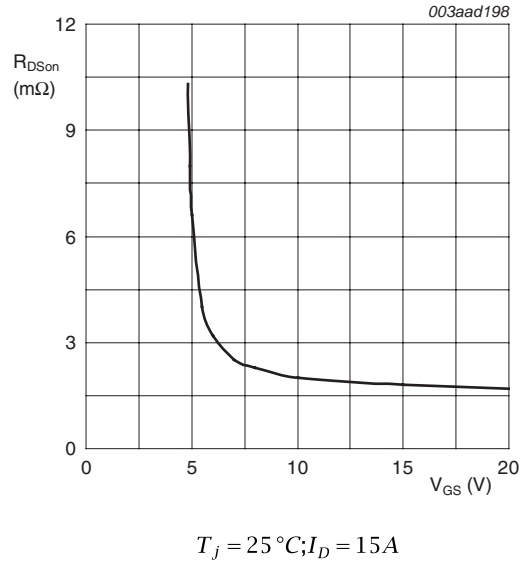


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

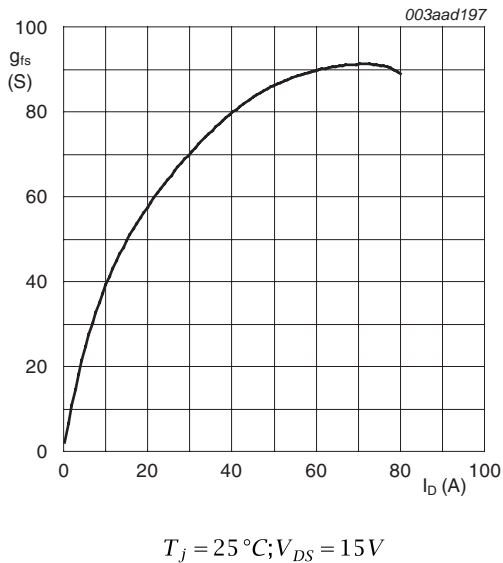


Fig 9. Forward transconductance as a function of drain current; typical values

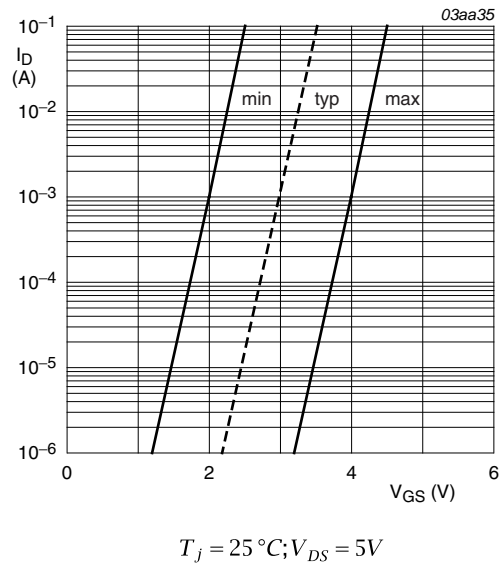
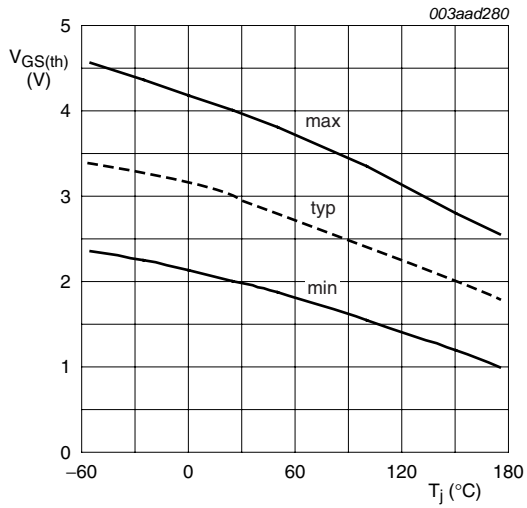
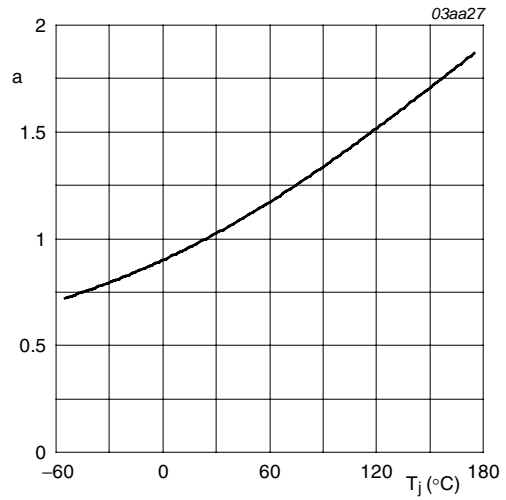


Fig 10. Sub-threshold drain current as a function of gate-source voltage



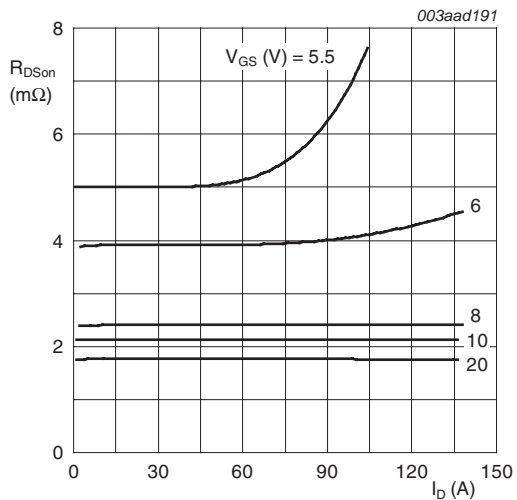
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

**Fig 11. Gate-source threshold voltage as a function of junction temperature**



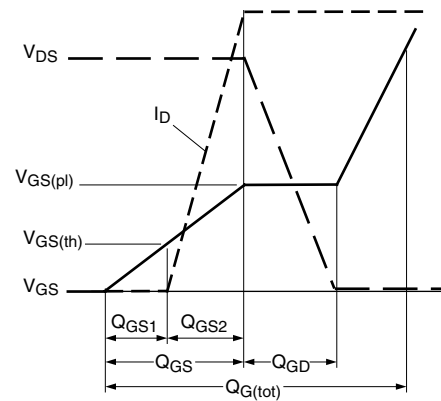
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature**



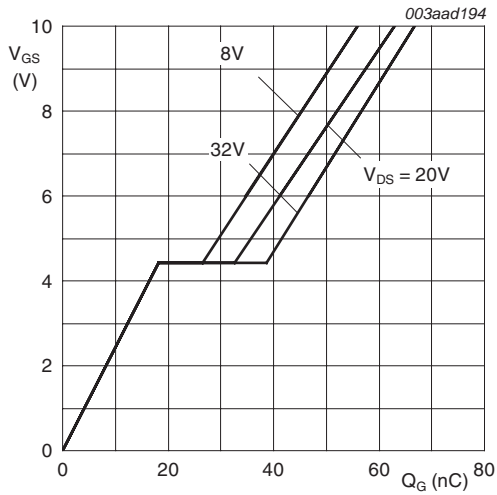
$$T_j = 25^\circ\text{C}$$

**Fig 13. Drain-source on-state resistance as a function of drain current; typical values**



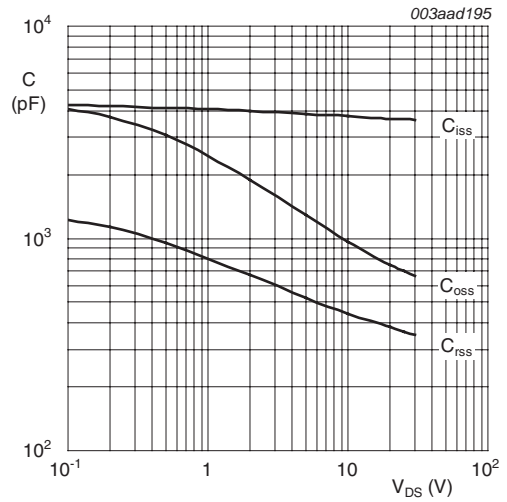
**Fig 14. Gate charge waveform definitions**





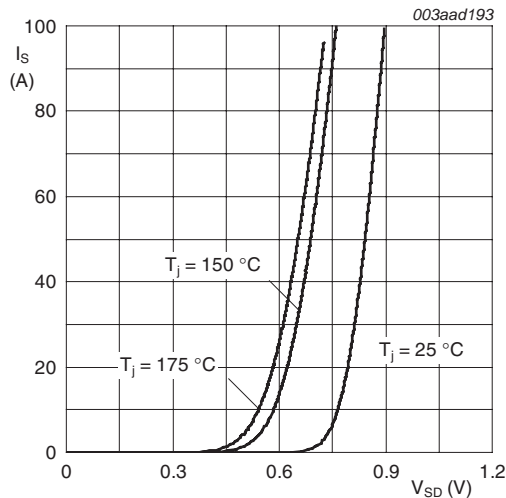
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{V}$

Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669

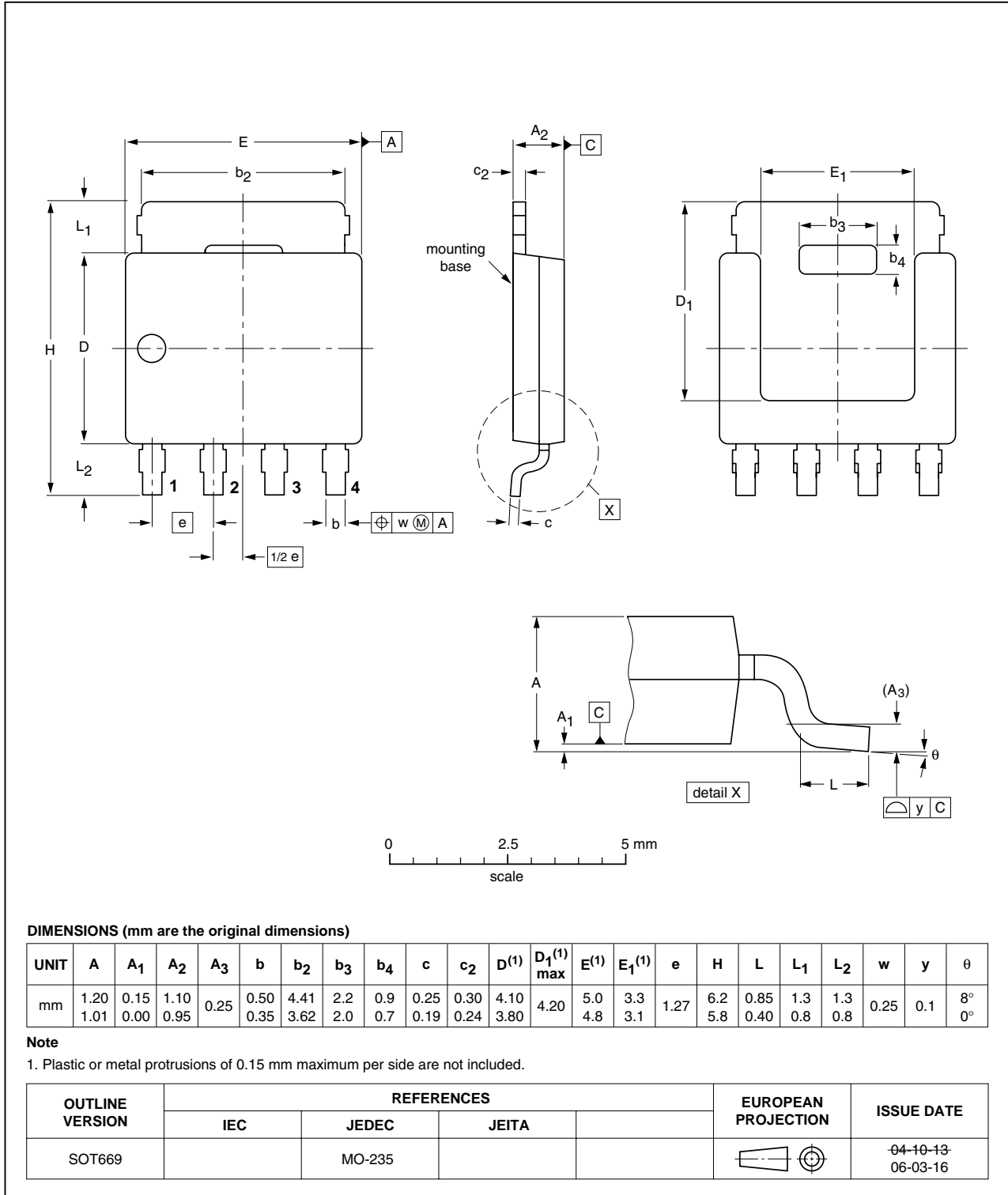


Fig 18. Package outline SOT669 (LPAK)

## 8. Revision history

Table 7. Revision history

| Document ID    | Release date | Data sheet status  | Change notice | Supersedes |
|----------------|--------------|--------------------|---------------|------------|
| PSMN2R6-40YS_1 | 20090623     | Product data sheet | -             | -          |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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| 1.3       | Applications . . . . .                   | 1         |
| 1.4       | Quick reference data . . . . .           | 1         |
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