TJA1043

High-speed CAN transceiver

Rev. 3 — 24 April 2013 **Product data sheet**

1. General description

The TJA1043 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed (up to 1 Mbit/s) CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1043 belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices such as the TJA1041A. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroMagnetic Discharge (ESD) performance, very low power consumption, and passive behavior when the supply voltage is turned off. Advanced features include:

- Low-power management controls the power supply throughout the node while supporting local and remote wake-up with wake-up source recognition
- Several protection and diagnostic functions including bus line short-circuit detection and battery connection detection
- Can be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V

These features make the TJA1043 the ideal choice for high speed CAN networks containing nodes that need to be available all times, even when the internal V_{IO} and V_{CC} supplies are switched off.

2. Features and benefits

2.1 General

- Fully ISO 11898-2 and ISO 11898-5 compliant
- Suitable for 12 V and 24 V systems
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- V_{IO} input allows for direct interfacing with 3 V and 5 V microcontrollers
- SPLIT voltage output for stabilizing the recessive bus level
- Listen-only mode for node diagnosis and failure containment
- Available in SO14 and HVSON14 packages
- Leadless HVSON14 package (3.0 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Low-power management

- Very low current Standby and Sleep modes, with local and remote wake-up
- Capability to power down the entire node while supporting local, remote and host wake-up
- Wake-up source recognition
- Transceiver disengages from the bus (zero load) when V_{BAT} absent
- Functional behavior predictable under all supply conditions

2.3 Protection and diagnosis (detection and signalling)

- High ESD handling capability on the bus pins
- Bus pins and V_{BAT} protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function with diagnosis
- TXD-to-RXD short-circuit handler with diagnosis
- Thermal protection with diagnosis
- Undervoltage detection and recovery on pins V_{CC}, V_{IO} and V_{BAT}
- Bus line short-circuit diagnosis
- Bus dominant clamping diagnosis
- Cold start diagnosis (first battery connection)

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3	3.5	4.3	V
I_{CC}	supply current	Normal mode; bus dominant	30	48	65	mA
		Normal or Listen-only mode; bus recessive	3	6	9	mA
		Standby or Sleep mode	0	0.75	2	μA
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANH and CANL	−8	-	+8	kV
V_{CANH}	voltage on pin CANH	no time limit; DC limiting value	−58	-	+58	V
V_{CANL}	voltage on pin CANL	no time limit; DC limiting value	−58	-	+58	V
T_{vj}	virtual junction temperature		−40	-	+150	°C

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1043T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1043TK	HVSON14	plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

5. Block diagram

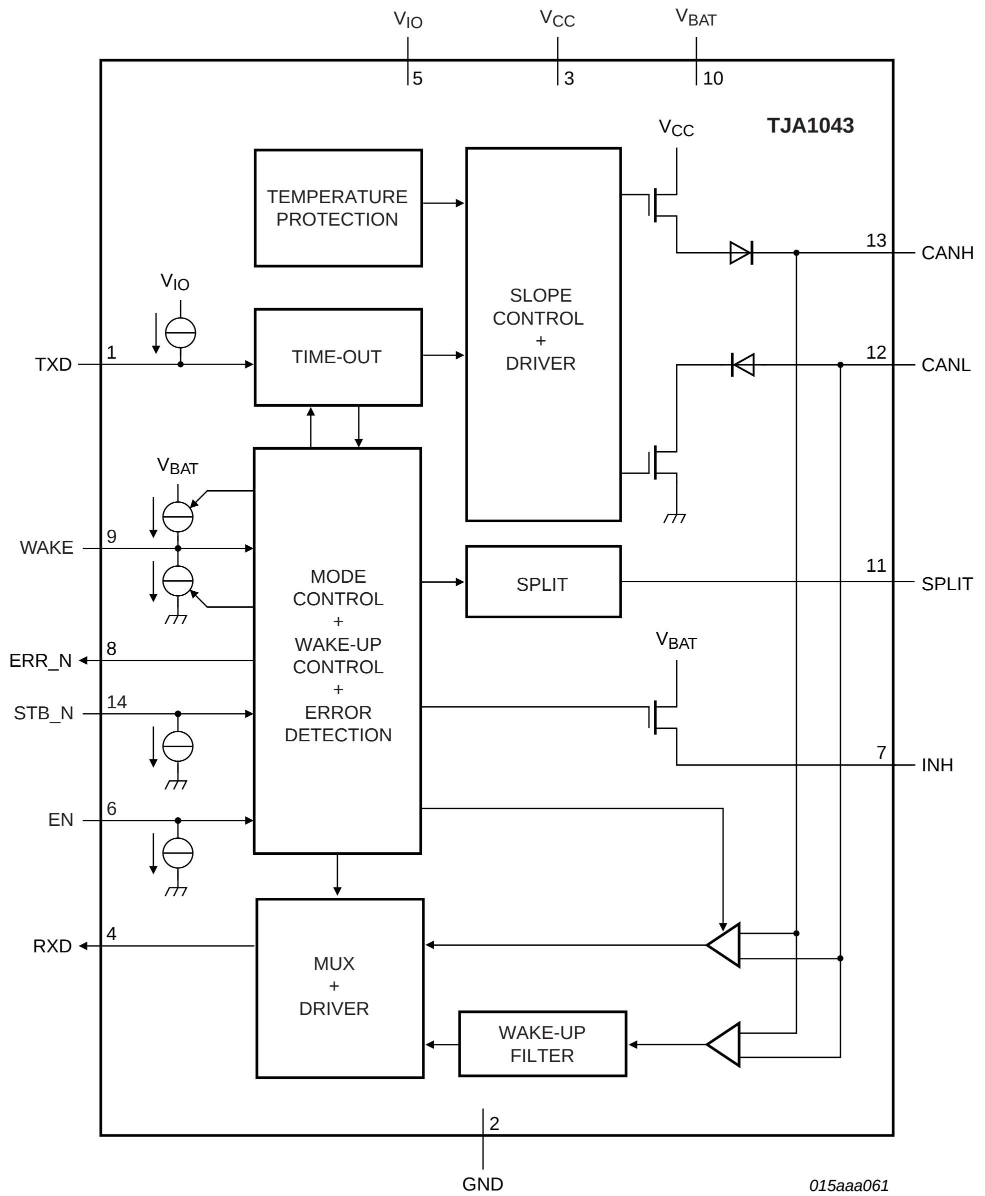


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

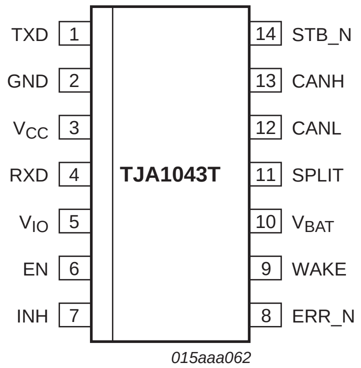


Fig 2. Pin configuration diagram: SO14

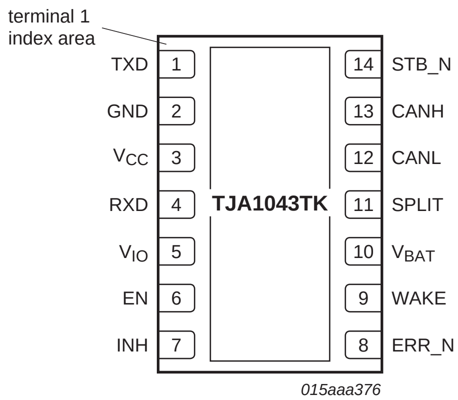


Fig 3. Pin configuration diagram: HVSON14

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND[1]	2	ground supply
V_{CC}	3	transceiver supply voltage
RXD	4	receive data output; reads out data from the bus lines
V_{IO}	5	supply voltage for I/O level adaptor
EN	6	enable control input
INH	7	inhibit output for switching external voltage regulators
ERR_N	8	error and power-on indication output (active LOW)
WAKE	9	local wake-up input
V_{BAT}	10	battery supply voltage
SPLIT	11	common-mode stabilization output
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
STB_N	14	standby control input (active LOW)

[1] For enhanced thermal and electrical performance, the exposed center pad of the HVSON14 package should be soldered to board ground (and not to any other voltage level).

7. Functional description

The TJA1043 is a stand-alone high-speed CAN transceiver with a number of operating modes, fail-safe features and diagnostic features that offer enhanced system reliability and advanced power management. The transceiver combines the functionality of the

TJA1041A with improved EMC and ESD capability and quiescent current performance. Improved slope control and high DC handling capability on the bus pins provide additional application flexibility.

7.1 Operating modes

The TJA1043 supports five operating modes. Control pins STB_N and EN are used to select the operating mode. Switching between modes allows access to a number of diagnostics flags via pin ERR_N. Table 4 describes how to switch between modes. Figure 4 illustrates the mode transitions when V_{CC}, V_{IO} and V_{BAT} are valid.

Table 4. Operating mode selection

Internal flags			Control pins		Operating mode	Pin INH
UV_{NOM}[1]	UV_{BAT}	Wake[2]	STB_N[3]	EN		
From Normal, Listen-only, Standby and Go-to-Sleep modes						
set	X	X	X	X	Sleep mode	floating
cleared	set	X	HIGH	X	Standby mode	HIGH
cleared	X	set	LOW	X	Standby mode	HIGH
cleared	X	cleared	LOW	LOW	Standby mode	HIGH
cleared	X	cleared	LOW	HIGH	Go-to-Sleep mode[4]	HIGH[4]
cleared	cleared	X	HIGH	LOW	Listen-only mode	HIGH
cleared	cleared	X	HIGH	HIGH	Normal mode	HIGH
From Sleep mode						
set	X	X	X	X	Sleep mode	floating
cleared	set	X	HIGH	X	Standby mode	HIGH
cleared	X	set	LOW	X	Standby mode	HIGH
cleared	X	cleared	LOW	X	Sleep mode	floating
cleared	cleared	X	HIGH	LOW	Listen-only mode	HIGH
cleared	cleared	X	HIGH	HIGH	Normal mode	HIGH

[1] Setting the UV_{NOM} flag will clear the WAKE flag.

[2] Setting the Wake flag will clear the UV_{NOM} flag.

[3] A LOW-to-HIGH transition on pin STB_N will clear the UV_{NOM} flag

[4] After the minimum hold time, in Go-to-Sleep mode, $t_{h(min)}$, the transceiver will enter Sleep mode and pin INH will be set floating.

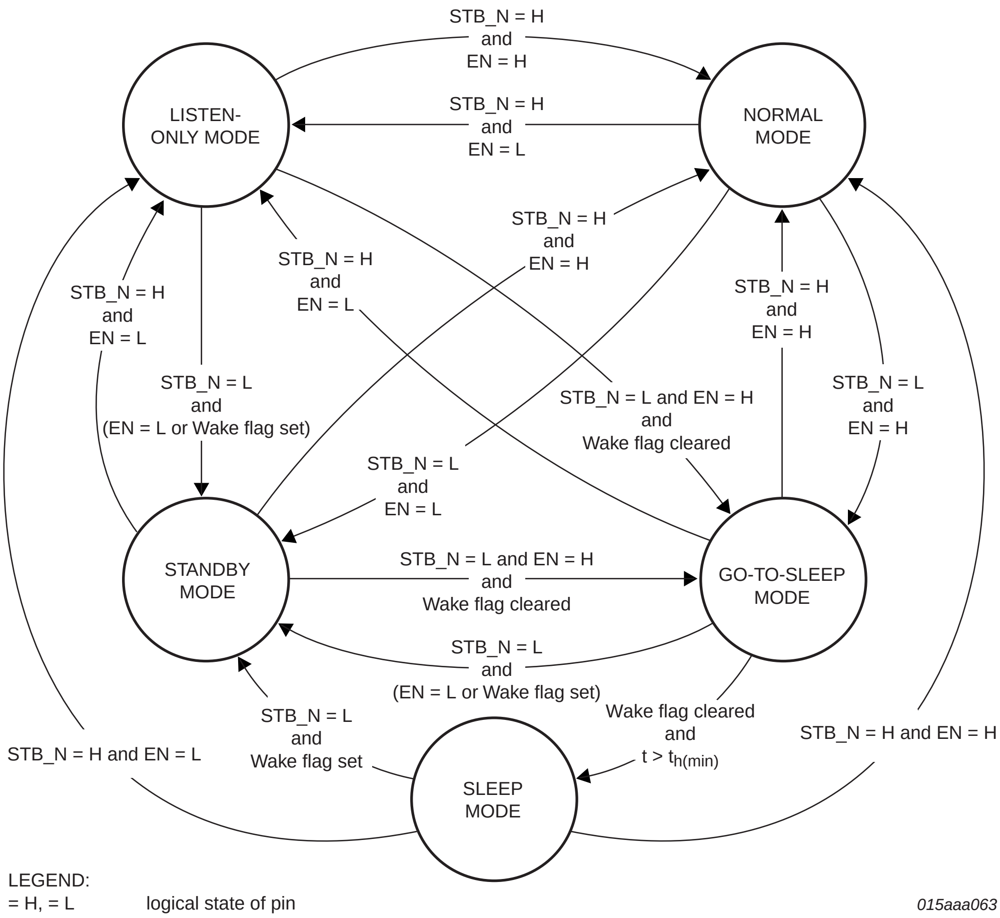


Fig 4. Mode transitions when valid V_{CC}, V_{IO} and V_{BAT} voltages are present

7.1.1 Normal mode

In Normal mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible EME. The bus pins are biased to $0.5V_{CC}$ (via R_i). Pin INH is active, so voltage regulators controlled by pin INH (see Figure 7) will be active too.

7.1.2 Listen-only mode

In Listen-only mode, the transceiver's transmitter is disabled, effectively providing a transceiver listen-only feature. The receiver will still convert the analog bus signal on pins CANH and CANL into digital data, available for output on pin RXD. As in Normal mode, the bus pins are biased at $0.5V_{CC}$ and pin INH remains active.

7.1.3 Standby mode

Standby mode is the TJA1043's first-level power saving mode, offering reduced current consumption. In Standby mode, the transceiver is unable to transmit or receive data and the low-power receiver is activated to monitor bus activity. The bus pins are biased at ground level (via R_i). Pin INH is still active, so voltage regulators controlled by this pin will also be active.

Pins RXD and ERR_N will reflect any active wake-up requests (provided that V_{IO} and V_{BAT} are present).

7.1.4 Go-to-Sleep mode

Go-to-Sleep mode is the controlled route for entering Sleep mode. In Go-to-Sleep mode, the transceiver behaves as in Standby mode, with the addition that a go-to-sleep command is issued to the transceiver. The transceiver will remain in Go-to-Sleep mode for the minimum hold time ($t_{h(min)}$) before entering Sleep mode. The transceiver will not enter Sleep mode if the state of pin STB_N or pin EN is changed or if the Wake flag is set before $t_{h(min)}$ has elapsed.

7.1.5 Sleep mode

Sleep mode is the TJA1043's second-level power saving mode. Sleep mode is entered via Go-to-Sleep mode, and also when the undervoltage detection time on either V_{CC} or V_{IO} elapses before the relevant voltage level has recovered. In Sleep mode, the transceiver behaves as described for Standby mode, with the exception that pin INH is set floating. Voltage regulators controlled by this pin will be switched off, and the current into pin V_{BAT} will be reduced to a minimum. Pins STB_N, EN and the Wake flag can be used to wake up a node from Sleep mode (see Table 4).

7.2 Internal flags

The TJA1043 makes use of seven internal flags for its fail-safe fallback mode control and system diagnosis support. Five of these flags can be polled by the controller via pin ERR_N. Which flag is available on pin ERR_N at any time depends on the active operating mode and on a number of other conditions. Table 5 describes how to access these flags.

Table 5. Accessing internal flags via pin ERR_N

Internal flag	Flag is available on pin ERR_N[1]	Flag is cleared
UV_{NOM}	no	by setting the Pwon or Wake flags, by a LOW-to-HIGH transition on STB_N or when both V_{IO} and V_{BAT} have recovered.
UV_{BAT}	no	when V_{BAT} has recovered
Pwon	in Listen-only mode (coming from Standby mode, Go-to-Sleep mode, or Sleep mode)	on entering Normal mode
Wake	in Standby mode, Go-to-Sleep mode, and Sleep mode (provided that V_{IO} and V_{BAT} are present)	on entering Normal mode or by setting the UV_{NOM} flag

Table 5. Accessing internal flags via pin ERR_N *...continued*

Internal flag	Flag is available on pin ERR_N[1]	Flag is cleared
Wake-up source	in Normal mode (before the fourth dominant-to-recessive edge on pin TXD[2])	on leaving Normal mode
Bus failure	in Normal mode (after the fourth dominant-to-recessive edge on pin TXD[2])	on re-entering Normal mode or by setting the Pwon flag
Local failure	in Listen-only mode (coming from Normal mode)	on entering Normal mode or when RXD is dominant while TXD is recessive (provided that all local failures are resolved) or by setting the Pwon flag

[1] Pin ERR_N is an active-LOW output, so a LOW-level indicates a set flag and a HIGH-level indicates a cleared flag. Allow pin ERR_N to stabilize for at least 8 μs after changing operating modes.

[2] Allow for a TXD dominant time of at least 4 μs per dominant-recessive cycle.

7.2.1 UV_{NOM} flag

UV_{NOM} is the V_{CC} and V_{IO} undervoltage detection flag. The flag is set when the voltage on pin V_{CC} drops below the V_{CC} undervoltage detection voltage, $V_{uvd(VCC)}$, for longer than the undervoltage detection time, $t_{det(uv)}$, or when the voltage on pin V_{IO} drops below $V_{uvd(VIO)}$ for longer than $t_{det(uv)}$. When the UV_{NOM} flag is set, the transceiver enters Sleep mode to save power and to ensure the bus is not disturbed. In Sleep mode the voltage regulators connected to pin INH are disabled, avoiding any extra power consumption that might be generated as a result of a short-circuit condition.

Any wake-up request, setting the Pwon flag or a LOW-to-HIGH transition on STB_N will clear UV_{NOM} and the timers, allowing the voltage regulators to be reactivated (at least until UV_{NOM} is set again). UV_{NOM} will also be cleared if both V_{CC} and V_{IO} recover for longer than the undervoltage recovery time, $t_{rec(uv)}$. The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN (see Table 4).

7.2.2 UV_{BAT} flag

UV_{BAT} is the V_{BAT} undervoltage detection flag. This flag is set when the voltage on pin V_{BAT} drops below $V_{uvd(VBAT)}$. When UV_{BAT} is set, the transceiver will try to enter Standby mode to save power and will disengage from the bus (zero load). UV_{BAT} is cleared when the voltage on pin V_{BAT} recovers. The transceiver will then switch to the operating mode indicated by the logic levels on pins STB_N and EN (see Table 4).

7.2.3 Pwon flag

Pwon is the V_{BAT} power-on flag. This flag is set when the voltage on pin V_{BAT} recovers after previously dropping below $V_{uvd(VBAT)}$ (usually because the battery was disconnected). Setting the Pwon flag clears the UV_{NOM} flag and timers. The Wake and Wake-up source flags are set to ensure consistent system power-up under all supply conditions. In Listen-only mode the Pwon flag can be polled via pin ERR_N (see Table 5). The flag is cleared when the transceiver enters Normal mode.

7.2.4 Wake flag

The Wake flag is set when the transceiver detects a local or remote wake-up request. A local wake-up request is detected when the logic level on pin WAKE changes, and the new level remains stable for at least t_{wake}. A remote wake-up request is triggered by two bus dominant states of at least $t_{wake(busdom)}$, with the first dominant state followed by a recessive state of at least $t_{wake(busrec)}$ (provided the complete dominant-recessive-dominant pattern is completed within $t_{to(wake)bus}$). The Wake flag can be set in Standby mode, Go-to-Sleep mode or Sleep mode. Setting the Wake flag clears the UV_{NOM} flag and timers. Once set, the Wake flag status is immediately available on pins ERR_N and RXD (provided V_{IO} and V_{BAT} are present). This flag is also set at power-on and cleared when the UV_{NOM} flag is set or the transceiver enters Normal mode.

7.2.5 Wake-up source flag

Wake-up source recognition is provided via the Wake-up source flag, which is set when the Wake flag is set by a local wake-up request via the WAKE pin. The Wake-up source flag can be polled via the ERR_N pin in Normal mode (see Table 5). This flag is also set at power-on and cleared when the transceiver leaves Normal mode.

7.2.6 Bus failure flag

The Bus failure flag is set if the transceiver detects a bus line short-circuit condition to V_{BAT}, V_{CC} or GND during four consecutive dominant-recessive cycles on pin TXD, while trying to drive the bus lines dominant. The Bus failure flag can be polled via the ERR_N pin in Normal mode (see Table 5). This flag is cleared at power-on or when the transceiver re-enters Normal mode.

7.2.7 Local failure flag

In Normal and Listen-only modes, the transceiver can distinguish four different local failure events, any of which will cause the Local failure flag to be set. The four local failure events are: TXD dominant clamping, TXD-to-RXD short circuit, bus dominant clamping and an overtemperature event. The nature and detection of these local failures is described in Section 7.3. The Local failure flag can be polled via the ERR_N pin in Listen-only mode (see Table 5). This flag is cleared at power-on, when entering Normal mode or when RXD is dominant while TXD is recessive, provided that all local failures have been resolved.

7.3 Local failures

The TJA1043 can detect four different local failure conditions. Any of these failures will set the Local failure flag, and in most cases the transmitter of the transceiver will be disabled.

7.3.1 TXD dominant clamping detection

A permanent LOW level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communications. The TXD dominant time-out function prevents such a network lock-up by disabling the transmitter if pin TXD remains LOW for longer than the TXD dominant time-out time $t_{to(dom)TXD}$. The $t_{to(dom)TXD}$ timer defines the minimum possible bit rate of 40 kbit/s. The transmitter remains disabled until the Local failure flag has been cleared.

7.3.2 TXD-to-RXD short-circuit detection

A short-circuit between pins RXD and TXD would lock the bus in a permanent dominant state once it had been driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. TXD-to-RXD short-circuit detection prevents such a network lock-up by disabling the transmitter. The transmitter remains disabled until the Local failure flag has been cleared.

7.3.3 Bus dominant clamping detection

A CAN bus short circuit (to V_{BAT}, V_{CC} or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The Local failure flag is set if the dominant state on the bus persists for longer than $t_{to(dom)bus}$. By checking this flag, the controller can determine if a clamped bus is blocking network communications. There is no need to disable the transmitter. Note that the Local failure flag does not retain a bus dominant clamping failure, and is released as soon as the bus returns to recessive state.

7.3.4 Overtemperature detection

If the junction temperature becomes excessive, the transmitter will shut down in time to protect the output drivers from overheating without compromising the maximum operating temperature. The transmitter will remain disabled until the Local failure flag has been cleared.

7.4 SPLIT pin

Using the SPLIT pin on the TJA1043 in conjunction with a split termination network (see Figure 5 and Figure 7) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal and Listen-only modes, pin SPLIT delivers a DC output voltage of $0.5V_{CC}$. In Standby, Go-to-Sleep and Sleep modes, pin SPLIT is floating.

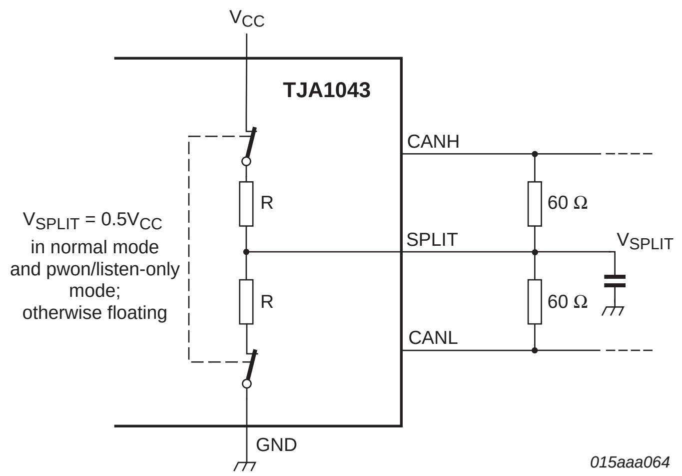


Fig 5. Stabilization circuit and application

7.5 V_{IO} supply pin

Pin V_{IO} should be connected to the microcontroller supply voltage (see Figure 7). This will cause the signal levels of pins TXD, RXD, STB_N, EN and ERR_N to be adjusted to the I/O levels of the microcontroller, facilitating direct interfacing without the need for glue logic.

7.6 WAKE pin

A local wake-up event is triggered by a LOW-to-HIGH or HIGH-to-LOW transition on the WAKE pin, allowing for maximum flexibility when designing a local wake-up circuit.To minimize current consumption, the internal bias voltage will follow the logic state on the pin after a delay of t_{wake}. A HIGH level on pin WAKE is followed by an internal pull-up to V_{BAT}. A LOW level on pin WAKE is followed by an internal pull-down towards GND. In applications that don't make use of the local wake-up facility, it is recommended that the WAKE pin be connected to V_{BAT} or GND to ensure optimal EMI performance.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	battery supply voltage	no time limit		–0.3	+58	V
		load dump		-	58	V
V_x	voltage on pin x	no time limit; DC value				
		on pins CANH, CANL and SPLIT		–58	+58	V
		on pins INH and WAKE		–0.3	+58	V
		on pins V_{CC}, V_{IO}, TXD, RXD, STB_N, EN, ERR_N		–0.3	+7	V
I_{WAKE}	current on pin WAKE	DC value		-	–15	mA
V_{trt}	transient voltage	on pins CANH, CANL, SPLIT and V_{BAT}	[1]	–200	+200	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2	[2]			
		at pins CANH and CANL	[3]	–8	+8	kV
		HBM	[4]			
		at pins CANH and CANL		–8	+8	kV
		at any other pin		–4	+4	kV
		MM	[5]			
		at any pin		–300	+300	V
		CDM	[6]			
		at corner pins		–750	+750	V
		at any pin		–500	+500	V
T_{vj}	virtual junction temperature		[7]	–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C

[1] Verified by an external test house to ensure pins CANH, CANL, SPLIT and V_{BAT} can withstand ISO 7637 part 3 automotive transient test pulses 1, 2a, 3a and 3b.

[2] IEC 61000-4-2 (150 pF, 330 Ω); direct coupling.

[3] ESD performance of pins CANH and CANL according to IEC 61000-4-2 (150 pF, 330 Ω) has been verified by an external test house. The result is equal to or better than ±8 kV (unaided).

[4] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[5] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μH, 10 Ω).

[6] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF); grade C3B.

[7] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 7. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(vj-a)}$	thermal resistance from virtual junction to ambient	SO14 package; in free air	68	K/W
		HVSON14 package; in free air	44	K/W

10. Static characteristics

Table 8. Static characteristics

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply pin V_{CC}						
V_{CC}	supply voltage		4.5	-	5.5	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}	V_{BAT} > 4.5 V	3	3.5	4.3	V
I_{CC}	supply current	Normal mode; V_{TXD} = 0 V (dominant)	30	48	65	mA
		Normal or Listen-only mode; V_{TXD} = V_{IO} (recessive)	3	6	9	mA
		Standby or Sleep mode; V_{BAT} > V_{CC}	0	0.75	2	μA
I/O level adapter supply; pin V_{IO}						
V_{IO}	supply voltage on pin V_{IO}		2.8	-	5.5	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}	V_{BAT} or V_{CC} > 4.5 V	0.8	1.8	2.5	V
I_{IO}	supply current on pin V_{IO}	Normal mode; V_{TXD} = 0 V (dominant)	-	150	500	μA
		Normal or Listen-only mode; V_{TXD} = V_{IO} (recessive)	0	1	4	μA
		Standby or Sleep mode	0	1	4	μA
Supply pin V_{BAT}						
V_{BAT}	battery supply voltage		4.5	-	40	V
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin V_{BAT}		3	3.5	4.3	V
I_{BAT}	battery supply current	Normal or Listen-only mode	15	40	70	μA
		Standby mode; V_{CC} > 4.5 V V_{INH} = V_{WAKE} = V_{BAT}	5	18	30	μA
		Sleep mode; V_{INH} = V_{CC} = V_{IO} = 0 V; V_{WAKE} = V_{BAT}	5	18	30	μA
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	+0.3V_{IO}	V
I_{IH}	HIGH-level input current	V_{TXD} = V_{IO}	−5	0	+5	μA
I_{IL}	LOW-level input current	Normal mode; V_{TXD} = 0 V	−300	−200	−30	μA
C_i	input capacitance	not tested	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	V_{RXD} = V_{IO} − 0.4 V; V_{IO} = V_{CC}	−12	−6	0	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; V_{TXD} = V_{IO}; bus dominant	0	6	14	mA
Standby and enable control inputs; pins STB_N and EN						
V_{IH}	HIGH-level input voltage		0.7V_{IO}	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.3V_{IO}	V
I_{IH}	HIGH-level input current	V_{STB_N} = V_{EN} = 0.7V_{IO}	1	4	10	μA

Table 8. Static characteristics *...continued*

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current	V_{STB_N} = V_{EN} = 0 V	−1	0	+1	μA
Error and power-on indication output; pin ERR_N						
I_{OH}	HIGH-level output current	V_{ERR_N} = V_{IO} − 0.4 V; V_{IO} = V_{CC}	−50	−20	−4	μA
I_{OL}	LOW-level output current	V_{ERR_N} = 0.4 V	0.1	0.5	2	mA
Local wake-up input; pin WAKE						
I_{IH}	HIGH-level input current	V_{WAKE} = V_{BAT} − 1.9 V	−10	−5	−1	μA
I_{IL}	LOW-level input current	V_{WAKE} = V_{BAT} − 3.1 V	1	5	10	μA
V_{th}	threshold voltage	V_{STB_N} = 0 V	V_{BAT} − 3	V_{BAT} − 2.5	V_{BAT} − 2	V
Inhibit output; pin INH						
ΔV_H	HIGH-level voltage drop	I_{INH} = −0.18 mA	0	0.25	0.8	V
I_L	leakage current	Sleep mode	−2	0	+2	μA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH	2.75	3.5	4.5	V
		pin CANL	0.5	1.5	2.25	V
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym}$ = V_{CC} − V_{CANH} − V_{CANL}	−400	-	+400	mV
$V_{O(dif)bus}$	bus differential output voltage	V_{TXD} = 0 V; V_{CC} = 4.75 V to 5.25 V; 45 Ω < R_L < 65 Ω; dominant	1.5	-	3.0	V
		V_{TXD} = V_{IO}; recessive; no load	−50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	Normal or Listen-only mode; V_{TXD} = V_{IO}; no load	2	$0.5V_{CC}$	3	V
		Standby or Sleep mode; no load	−0.1	0	+0.1	V
$I_{O(sc)}$	short-circuit output current	V_{TXD} = 0 V (dominant); V_{CC} = 5 V				
		pin CANH; V_{CANH} = 0 V	−100	−70	−40	mA
		pin CANL; V_{CANL} = 40 V	40	70	100	mA
$I_{O(rec)}$	recessive output current	−27 V < V_{CAN} < 32 V	−3	-	+3	mA
$V_{th(RX)dif}$	differential receiver threshold voltage	$V_{cm(CAN)}$ = −30 V to +30 V [2]				
		Normal or Listen-only mode	0.5	0.7	0.9	V
		Standby or Sleep mode	0.4	0.7	1.15	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal or Listen-only mode $V_{cm(CAN)}$ = −30 V to +30 V [2]	50	120	400	mV
I_{LI}	input leakage current	V_{CC} = 0 V; V_{CANH} = V_{CANL} = 5 V	100	170	250	μA
		V_{BAT} = 0 V; V_{CANH} = V_{CANL} = 5 V	−2	-	+2	μA
R_i	input resistance		9	15	28	kΩ
ΔR_i	input resistance deviation	between V_{CANH} and V_{CANL}	−3	0	+3	%
$R_{i(dif)}$	differential input resistance		19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance	V_{TXD} = V_{CC} [3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	V_{TXD} = V_{CC} [3]	-	-	10	pF

Table 8. Static characteristics *…continued*

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device [1].

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Common-mode stabilization output; pin SPLIT							
V_O	output voltage	Normal or Listen-only mode; −500 μA < I_{SPLIT} < 500 μA		$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
		Normal or Listen-only mode R_L = 1 MΩ		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
I_L	leakage current	Standby or Sleep mode; −58 V < V_{SPLIT} < +58 V		−3	0	+3	μA
Temperature detection							
$T_{j(sd)}$	shutdown junction temperature		[3]	-	190	-	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] $V_{cm(CAN)}$ is the common mode voltage of CANH and CANL.

[3] Not tested in production; guaranteed by design.

11. Dynamic characteristics

Table 9. Dynamic characteristics;

V_{CC} = 4.5 V to 5.5 V; V_{IO} = 2.8 V to V_{CC}; V_{BAT} = 4.5 V to 40 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Timing characteristics; Figure 6						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	70	-	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	90	-	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal or Listen-only mode	-	60	-	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal or Listen-only mode	-	70	-	ns
$t_{PD(TXD-RXD)}$	propagation delay from TXD to RXD	V_{STB_N} = 0 V	40	-	240	ns
$t_{det(uv)}$	undervoltage detection time		100	-	350	ms
$t_{rec(uv)}$	undervoltage recovery time		1	-	5	ms
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V	0.3	0.6	1.5	ms
$t_{to(dom)bus}$	bus dominant time-out time	$V_{O(dif)(bus)}$ > 0.9 V	0.3	0.6	1.5	ms
t_h	hold time	from issuing go-to-sleep command to entering Sleep mode	20	35	50	μs
$t_{wake(busdom)}$	bus dominant wake-up time	Standby or Sleep mode; V_{BAT} = 12 V	0.5	1.75	5	μs
$t_{wake(busrec)}$	bus recessive wake-up time	Standby or Sleep mode; V_{BAT} = 12 V	0.5	1.75	5	μs
$t_{to(wake)bus}$	bus wake-up time-out time		0.5	-	2	ms
t_{wake}	wake-up time	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode	5	25	50	μs

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

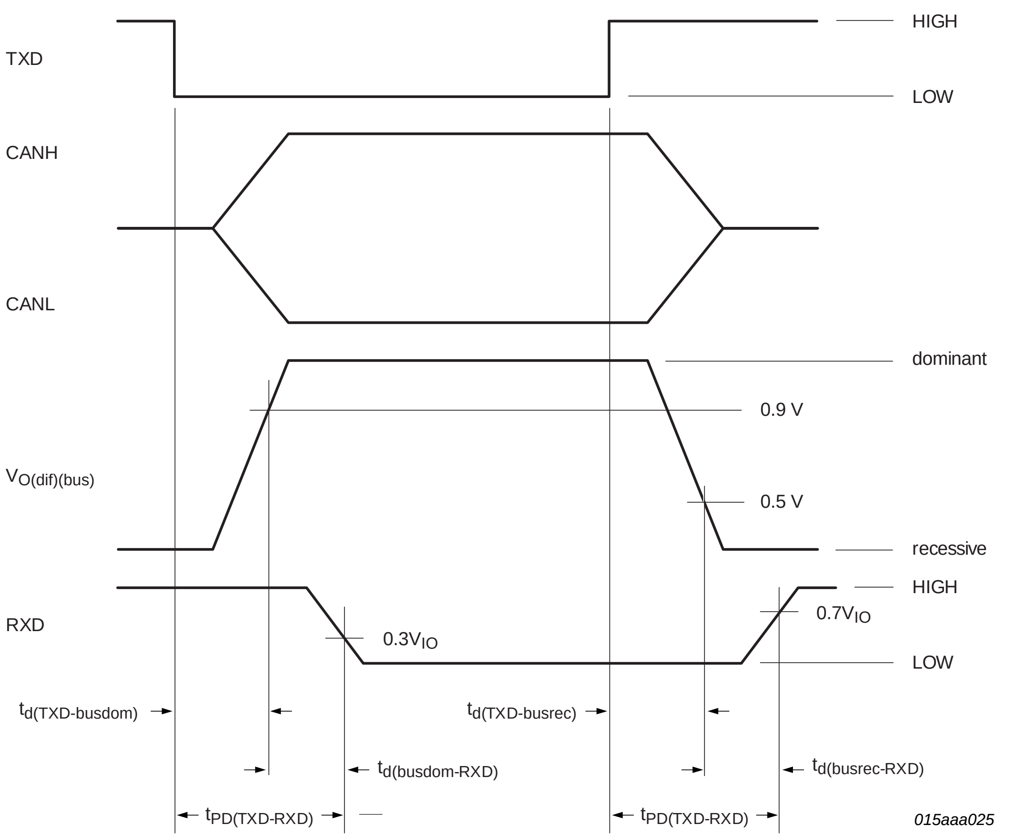


Fig 6. CAN transceiver timing diagram

12. Application information

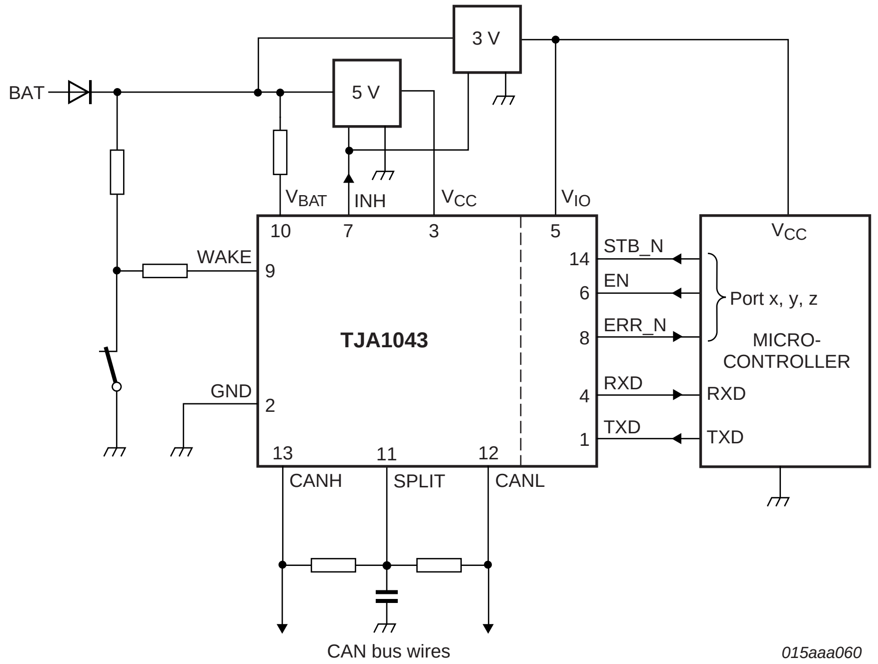


Fig 7. Typical application with 3 V microcontroller

13. Test information

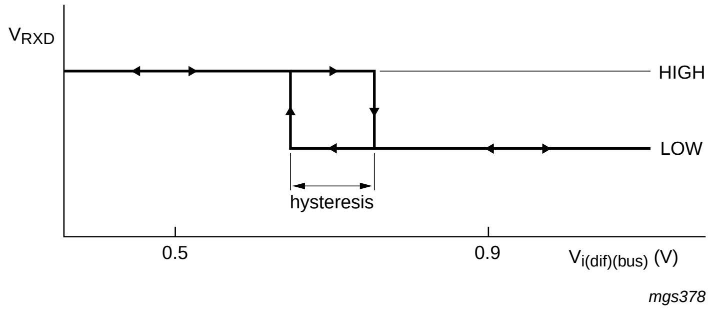


Fig 8. Hysteresis of the receiver

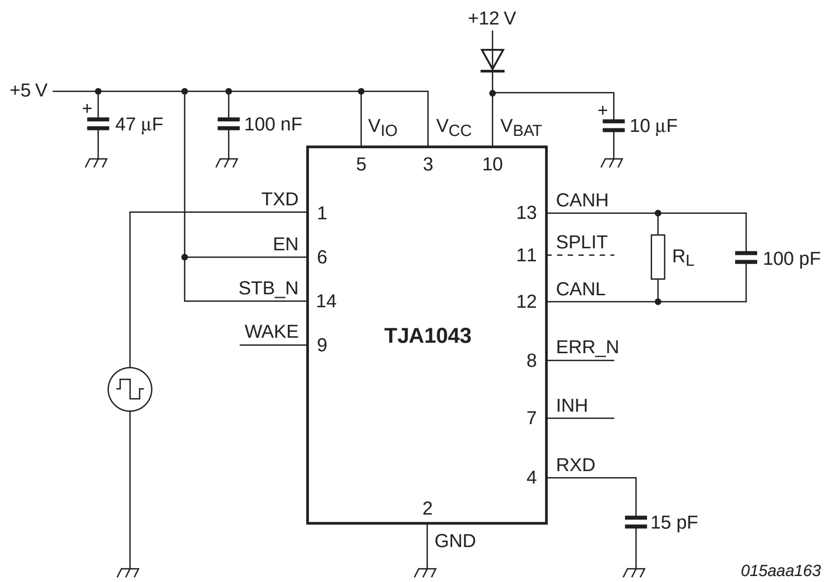


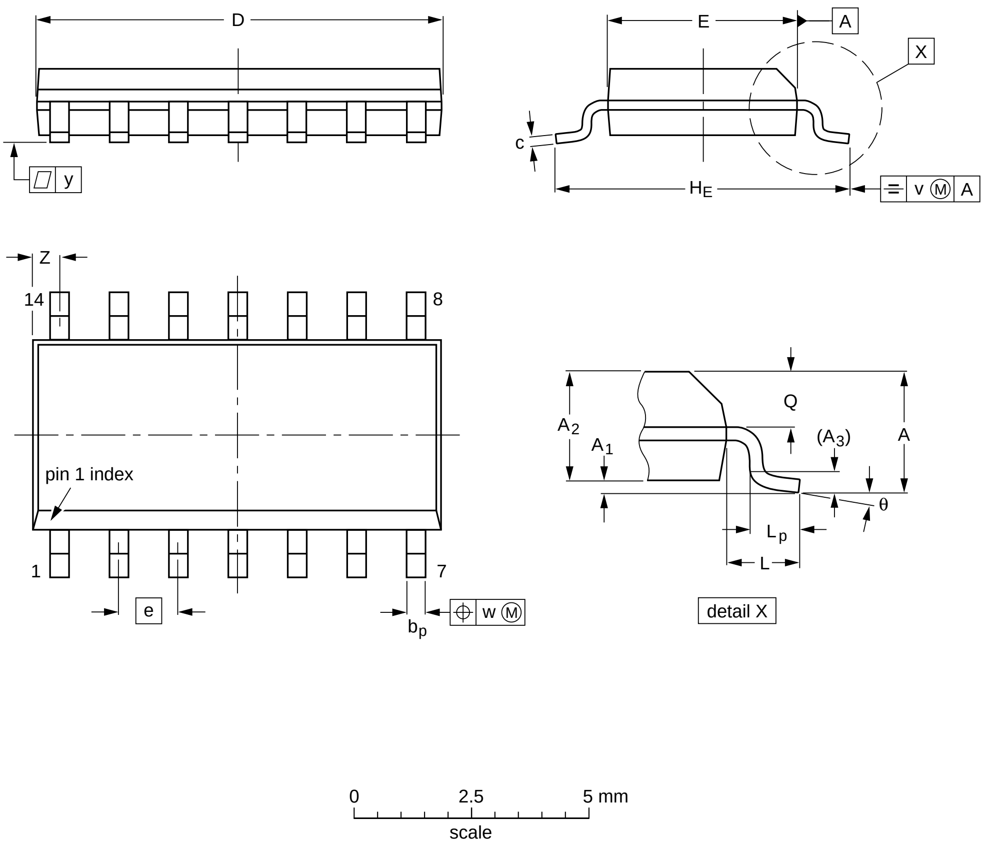
Fig 9. Test circuit for timing characteristics

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

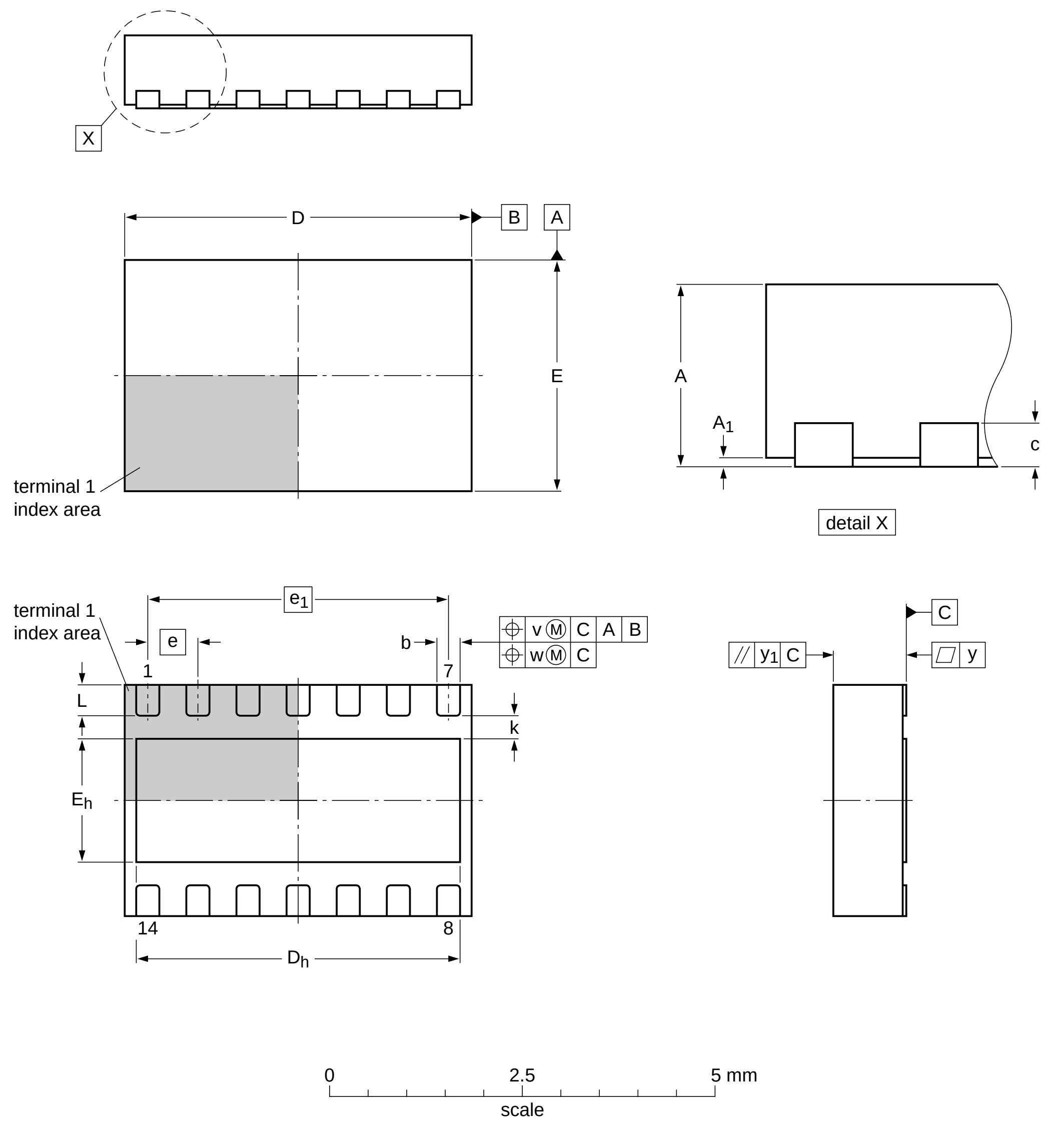
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
mm	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Fig 11. Package outline SOT1086 (HVSON14)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020D)

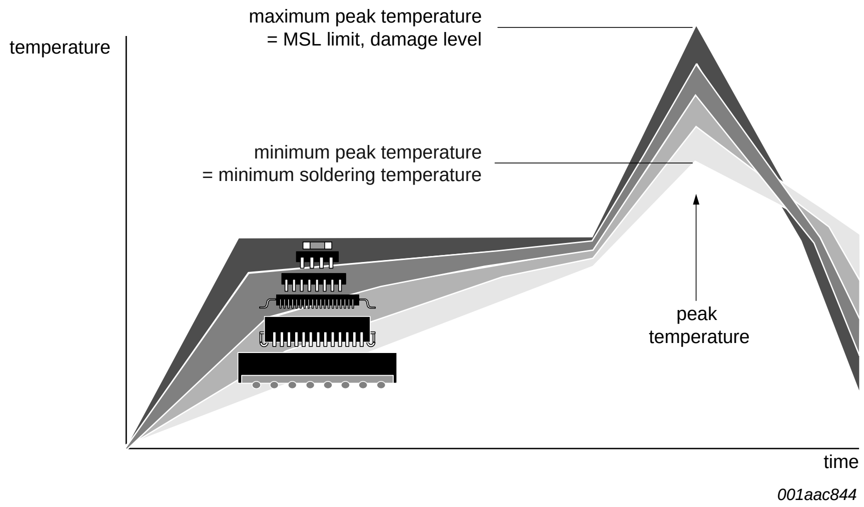
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.



MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17. Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can found in the following application notes:

- *AN10365 ‘Surface mount reflow soldering description”*
- *AN10366 “HVQFN application information”*

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1043 v.3	20130424	Product data sheet	-	TJA1043 v.2
Modifications:	• Section 2.1: revised • Added HVSON14 package (Table 2, Figure 3, Table 7, Figure 11) • Table 3: table note section added • Section 13.1 text revised • Section 17: added			
TJA1043 v.2	20110620	Product data sheet	-	TJA1043 v.1
TJA1043 v.1	20100330	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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