# 1. General description

The PCF2119x is a low power CMOS<sup>1</sup> LCD controller and driver, designed to drive a dot matrix LCD display of 2-lines by 16 characters or 1-line by 32 characters with  $5 \times 8$  dot format. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD bias voltages, resulting in a minimum of external components and lower system current consumption. The PCF2119x interfaces to most microcontrollers via a 4-bit or 8-bit bus or via the 2-wire l<sup>2</sup>C-bus. The chip contains a character generator and displays alphanumeric and kana (Japanese) characters.

The letter 'x' in PCF2119x characterizes the built-in character set. Various character sets can be manufactured on request. In addition 16 user defined symbols ( $5 \times 8$  dot format) are available.

For a selection of NXP LCD character drivers, see <u>Table 51 on page 78</u>.

# 2. Features and benefits

- Single-chip LCD controller and driver
- 2-line display of up to 16 characters plus 160 icons or 1-line display of up to 32 characters plus 160 icons
- 5 × 7 character format plus cursor; 5 × 8 for kana (Japanese) and user defined symbols
- Reduced current consumption while displaying icons only
- Icon blink function
- On-chip:
  - Configurable 4, 3, or 2 times voltage multiplier generating LCD supply voltage, independent of V<sub>DD</sub>, programmable by instruction (external supply also possible)
  - Temperature compensation of on-chip generated V<sub>LCDOUT</sub>: -0.16 %/K to -0.24 %/K (programmable by instruction)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Display Data RAM (DDRAM): 80 characters
- Character Generator ROM (CGROM): 240 characters (5 × 8)
- Character Generator RAM (CGRAM): 16 characters (5 × 8); 4 characters used to drive 160 icons, 8 characters used if icon blink feature is used in application
- 4-bit or 8-bit parallel bus and 2-wire l<sup>2</sup>C-bus interface
- Manufactured in silicon gate CMOS process
- 18 row and 80 column outputs

<sup>1.</sup> The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21.



**PCF2119x** 

- Multiplex rates 1:18 (2-line display or 1-line display), 1:9 (for 1-line display of up to 16 characters and 80 icons) and 1:2 (for icon only mode)
- Uses common 11 code instruction set (extended)
- Logic supply voltage: V<sub>DD1</sub> V<sub>SS1</sub> = 1.5 V to 5.5 V (chip may be driven with two battery cells)
- LCD supply voltage: V<sub>LCDOUT</sub> V<sub>SS2</sub> = 2.2 V to 6.5 V
- V<sub>LCD</sub> generator supply voltage: V<sub>DD2</sub> V<sub>SS2</sub> = 2.2 V to 4 V and V<sub>DD3</sub> V<sub>SS2</sub> = 2.2 V to 4 V
- Direct mode to save current consumption for icon mode and multiplex drive mode 1:9 (depending on V<sub>DD2</sub> value and LCD liquid properties)
- Very low current consumption (20 μA to 200 μA):
  - Icon mode: < 25 μA</p>
  - Power-down mode: < 2 μA</p>
- Icon mode is used to save current. When only icons are displayed, a much lower LCD operating voltage can be used and the switching frequency of the LCD outputs is reduced; in most applications it is possible to use V<sub>DD</sub> as LCD supply voltage

# 3. Applications

- Telecom equipment
- Portable instruments
- Point-of-sale terminals

# 4. Ordering information

### Table 1. Ordering information

Type number	Package				
	Name	Description	Version		
PCF2119AU	bare die	168 bumps	PCF2119x		
PCF2119DU	bare die	168 bumps	PCF2119x		
PCF2119FU	bare die	168 bumps	PCF2119x		
PCF2119IU	bare die	168 bumps	PCF2119x		
PCF2119RU	bare die	168 bumps	PCF2119x		
PCF2119SU	bare die	168 bumps	PCF2119x		

# 4.1 Ordering options

### Table 2.Ordering options

Product type number	IC revision	Sales item (12NC)	Delivery form
PCF2119AU/2DA/2	2	935273369033	chips in tray
PCF2119DU/2/2	2	935272743033	chips in tray
PCF2119FU/2/F2	2	935267829033	chips in tray
PCF2119IU/2DA/2	2	935294878033	chips in tray
PCF2119RU/2/F2	2	935263699033	chips in tray
PCF2119RU/2DB/2	2	935293133033	chips in tray
PCF2119SU/2/F2	2	935263700033	chips in tray

# 5. Marking

#### Table 3.Marking codes

Product type number	Marking code
PCF2119AU	PC2119-2
PCF2119DU	PC2119-2
PCF2119FU	PC2119-2
PCF2119IU	PC2119-2
PCF2119RU	PC2119-2
PCF2119SU	PC2119-2

# 6. Block diagram



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#### **Pinning information** 7.

### 7.1 Pinning



PCF2119X **Product data sheet** 

# 7.2 Pin description

#### Table 4.Pin description

Input or input/output pins must always be at a defined level (V<sub>SS</sub> or V<sub>DD</sub>) unless otherwise specified.

V <sub>DD1</sub> 1 to 6 supply voltage 1 (logic)	
V <sub>DD2</sub> 7 to 14         11         supply voltage 2 (for high voltage generator)	
V <sub>DD3</sub> 15 to 18 11 supply voltage 3 (for high voltage generator)	
E 19 2 data bus clock input	
<ul> <li>set HIGH to signal the start of a read or write ope</li> </ul>	ration
<ul> <li>data is clocked in or out of the chip on the negative of the clock</li> </ul>	/e edge
T1 and T2 20 and 21 test pins	
<ul> <li>must be connected to V<sub>SS1</sub></li> </ul>	
V <sub>SS1</sub> 22 to 29 3 ground supply voltage 1	
<ul> <li>for all circuits, except of high voltage generator</li> </ul>	
V <sub>SS2</sub> 30 to 35 3 ground supply voltage 2	
<ul> <li>for high voltage generator</li> </ul>	
V <sub>LCDSENSE</sub> 36 input for voltage multiplier regulation circuitry and for t level generation	he bias
<ul> <li>if V<sub>LCD</sub> is generated internally then this pin must be connected to V<sub>LCDUT</sub> and V<sub>LCDIN</sub></li> </ul>	be
<ul> <li>if V<sub>LCD</sub> is generated externally then this pin must connected to V<sub>LCDIN</sub> only</li> </ul>	be
V <sub>LCDOUT</sub> 37 to 43 V <sub>LCD</sub> output	
<ul> <li>if V<sub>LCD</sub> is generated internally then this pin must be connected to V<sub>LCDIN</sub> and to V<sub>LCDSENSE</sub></li> </ul>	be
<ul> <li>if V<sub>LCD</sub> is generated externally then this pin must open-circuit</li> </ul>	be left
V <sub>LCDIN</sub> 44 to 49 input for LCD bias level generator	
<ul> <li>if V<sub>LCD</sub> is generated internally then this pin must be connected to V<sub>LCDOUT</sub> and to V<sub>LCDSENSE</sub></li> </ul>	be
<ul> <li>if V<sub>LCD</sub> is generated externally then this pin must connected to V<sub>LCDSENSE</sub> and to the external V<sub>LCD</sub> supply</li> </ul>	be power
dummy 50 -	
R8 to R1, 51 to 58, LCD row driver output	
R17, 59, • R17 has two pins: R17 and R17DUP	
R17DUP, 100 P19 • R17 and R18 drive the icons	
R16, 141, R9 to R16 142 to 149	
C80 to C41. 60 to 99. LCD column driver output	
C40 to C1 101 to 140	
dummy 150 -	
SCL 151 and 152 4 I <sup>2</sup> C-bus serial clock input	
T3 153 test pin	
• open-circuit	
<ul> <li>not user accessible</li> </ul>	

Symbol					
Symbol	PIN	Description			
POR	154	external Power-On Reset (POR) input			
PD	155	power-down mode select			
		<ul> <li>for normal operation, pin PD must be LOW</li> </ul>			
SDA	156 and 157 [4]	I <sup>2</sup> C-bus serial data input/output			
R/W	158	read/write input			
		<ul> <li>pin R/W = HIGH selects the read operation</li> </ul>			
		• pin $R/\overline{W}$ = LOW selects the write operation			
		<ul> <li>this pin has an internal pull-up resistor</li> </ul>			
RS	159	register select pin			
		<ul> <li>this pin has an internal pull-up resistor</li> </ul>			
DB0 to DB2,	160 to 162, [5]6]	8 bit bidirectional data bus (bit 0 to bit 7)			
DB3/SA0, DB4 to DB7	163, 164 to 167	<ul> <li>the 8-bit bidirectional data bus (3-state) transfers data between the microcontroller and the PCF2119x</li> </ul>			
		<ul> <li>pin DB7 may be used as the busy flag, signalling that internal operations are not yet completed</li> </ul>			
		<ul> <li>4-bit operations the 4 higher order lines DB7 to DB4 are used, DB3 to DB0 must be left open-circuit</li> </ul>			
		<ul> <li>data bus line DB3 has an alternative function (SA0) as the I<sup>2</sup>C-bus address pin</li> </ul>			
		<ul> <li>each data line has its own internal pull-up resistor</li> </ul>			
OSC	168	oscillator or external clock input			
		<ul> <li>when the on-chip oscillator is used this pin must be connected to V<sub>DD1</sub></li> </ul>			

#### Table 4. Pin description ... continued

[1] Always put  $V_{DD2} = V_{DD3}$ .

- [2] When the I<sup>2</sup>C-bus is used, the parallel interface pin E must be LOW.
- [3] The substrate (rear side of the die) is wired to V<sub>SS</sub> but should not be electrically connected.
- [4] When the parallel bus is used, the pins SCL and SDA must be connected to V<sub>SS1</sub> or V<sub>DD1</sub>; they must not be left open-circuit.
- [5] In the I<sup>2</sup>C-bus read mode, ports DB7 to DB4 and DB2 to DB0 should be connected to  $V_{DD1}$  or left open-circuit.
- When the 4-bit interface is used without reading out from the PCF2119x (bit R/W is set permanently to [6] logic 0), the unused ports DB4 to DB0 can either be set to  $V_{\text{SS1}}$  or  $V_{\text{DD1}}$  instead of leaving them open-circuit.

# 8. Functional description

### 8.1 Oscillator and timing generator

The internal logic and the LCD drive signals of the PCF2119x are timed by the frequency  $f_{clk}$  which equals either the built in oscillator frequency  $f_{osc}$  or an external clock frequency  $f_{osc(ext)}$ .

### 8.1.1 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not disturbed by operations on the data buses.

### 8.1.2 Internal clock

To use the on-chip oscillator, pin OSC must be connected to V<sub>DD1</sub>. The on-chip oscillator provides the clock signal for the display system. No external components are required.

### 8.1.3 External clock

If an external clock will be used, the input is at pin OSC. The resulting display frame frequency is given by:

$$f_{fr} = \frac{f_{clk}}{3072}$$

**Remark:** Only in the power-down mode the clock is allowed to be stopped (pin OSC connected to  $V_{SS}$ ), otherwise the LCD is frozen in a DC state, which is not suitable for the liquid crystals.

### 8.2 Reset function and Power-On Reset (POR)

The PCF2119x must be reset externally when power is turned on. If no external reset is performed, the chip might start-up in an unwanted state.

For the external reset, pin POR has to be active HIGH. The reset has to be active for at least 3 oscillator periods in order for the reset to be executed. If the internal oscillator is used, the minimum reset activity time follows from the lowest possible oscillator frequency ( $f_{osc} = 140 \text{ kHz}$ ,  $t_{osc} \sim 7.1 \text{ } \mu\text{s}$ ,  $3 \times t_{osc} \sim 2.15 \text{ } \mu\text{s}$ ). The internal oscillator start-up time is 200  $\mu$ s (typ) up to 300  $\mu$ s (max) after power-on. In case that an external oscillator is used,  $t_{osc}$  is dependent from  $f_{osc(ext)}$ .

Afterwards the chip executes the Clear\_display instruction, which requires 165 oscillator cycles. After the reset the chip has the state shown in <u>Table 5</u> and is then ready for use.

(1)

Step	Function	Control bit and register state	Description	Reference
1	Clear_display	-	-	Table 17
2	Entry_mode_set	bit I_D = 1	incremental cursor move direction	Table 19
		bit $S = 0$	no display shift	
3	Display_ctl	bit $D = 0$	display off	Table 20
		bit $C = 0$	cursor off	
		bit $B = 0$	cursor character blink off	
4	Function_set	bit DL = 1	8-bit interface	Table 13
		bit $M = 0$	1-line display	
		bit $SL = 0$	1:18 multiplex drive mode	
		bit H = 0	normal instruction set	
5	default address pointer to DDRAM[1]	-	-	Table 23
6	Icon_ctl	bit IM = 0	character mode, full display	Table 26
		bit IB = 0	icon blink disabled	
7	Screen_conf	bit $L = 0$	default configuration	Table 24
	Disp_conf	bit $P = 0$ ; bit $Q = 0$	default configurations	Table 25
8	Temp_ctl	bit TC1 = 0; bit TC2 = 0	default temperature coefficient	Table 29
9	VLCD_set	register $V_A = 0$ ; register $V_B = 0$	V <sub>LCD</sub> generator off	Table 33
10	I <sup>2</sup> C-bus interface reset	-	-	-
11	HV_gen	bit S1 = 1; bit S0 = 0	V <sub>LCD</sub> generator set to 3 internal stages (4 voltage multipliers)	Table 31

#### Table 5. State after reset

[1] The Busy Flag (BF) indicates the busy state (bit BF = 1) until initialization ends. The busy state lasts 2 ms. The chip may also be initialized by software (see Table 45 and Table 46).

### 8.3 Power-down mode

The chip can be put into power-down mode by applying a HIGH-level to pin PD. In power-down mode all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V<sub>SS</sub>).

During power-down, information in the RAM and the chip state are preserved. Instruction execution during power-down is possible when pin OSC is externally clocked.

### 8.4 LCD supply voltage generator

The LCD supply voltage may be generated on-chip. The  $V_{LCD}$  generator is controlled by two internal 6-bit registers:  $V_A$  and  $V_B$ . Register  $V_A$  is programmed with the voltage for character mode and register  $V_B$  with the voltage for icon mode.

The nominal LCD operating voltage at room temperature is given by Equation 2:

$$V_{LCD(nom)} = V_x \times 0.08 + 1.82$$

Where  $V_x$  is the integer value of the register  $V_A$  or  $V_B$ .

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 $V_{LCD}$  is sometimes referred as the LCD operating voltage ( $V_{oper}$ ).

### 8.4.1 **Programming ranges**

Possible values for  $V_A$  and  $V_B$  are between 0 to 63.

Table 6.	Values	of V <sub>A</sub>	and V <sub>B</sub>	and the	corresponding	V <sub>LCD</sub>	values
Allingling	- 1 T	n = n - n	- 11	I values a	wa hiadhliadhtad		

All values at $T_{ref} = 27$	°C; allowed values	are highlighted
------------------------------	--------------------	-----------------

Integer values of $V_A$ and $V_B$	Corresponding value of V <sub>LCD</sub> in V	Integer values of $V_A$ and $V_B$	Corresponding value of V <sub>LCD</sub> in V	Integer values of $V_A$ and $V_B$	Corresponding value of V <sub>LCD</sub> in V
0	V <sub>LCD</sub> switched off	22	3.58	44	5.34
1	1.90	23	3.66	45	5.42
2	1.98	24	3.74	46	5.50
3	2.06	25	3.82	47	5.58
4	2.14	26	3.90	48	5.66
5	2.22	27	3.98	49	5.74
6	2.30	28	4.06	50	5.82
7	2.38	29	4.14	51	5.90
8	2.46	30	4.22	52	5.98
9	2.54	31	4.30	53	6.06
10	2.62	32	4.38	54	6.14
11	2.70	33	4.46	55	6.22
12	2.78	34	4.54	56	6.30
13	2.86	35	4.62	57	6.38
14	2.94	36	4.70	58	6.46
15	3.02	37	4.78	59	6.54
16	3.10	38	4.86	60	6.62
17	3.18	39	4.94	61	6.70
18	3.26	40	5.02	62	6.78
19	3.34	41	5.10	63	6.86
20	3.42	42	5.18		
21	3.50	43	5.26		

#### Remarks:

- Values producing more than 6.5 V at operating temperature are not allowed. Operation above this voltage may damage the device. When programming the operating voltage, the temperature coefficient of V<sub>LCDOUT</sub> must be taken into account.
- Values below 2.2 V are below the specified operating range of the chip and are therefore not allowed.

When the LCD supply voltage is generated on-chip, the V<sub>LCD</sub> pins should be decoupled to V<sub>SS</sub> with a suitable capacitor. The generated V<sub>LCDOUT</sub> is independent of V<sub>DD</sub> and is temperature compensated.

In Equation 2 the internal charge pump is not considered. However, if the supplied voltage to  $V_{DD2}$  and  $V_{DD3}$  is below the required  $V_{LCD}$ , it is necessary to use the internal charge pump. The multiplication factor indicates the number of stages used to increase the voltage. At multiplication factor 2 one, at multiplication factor 3 two and at multiplication

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factor 4, three stages are used. A multiplication factor of for example, 4 does not mean that a voltage of  $4 \times V_{DD2,3}$  is generated in the internal high-voltage generator. The charge pump is part of a control loop. This means that the control loop aims to regulate  $V_{LCD}$  at the programmed value.

The ITO track resistance limit the speed by which the capacitors can be charged. The multiplication factor exceeds the required  $V_{LCD}$  under all circumstances (that is, at low temperatures and along with the temperature compensation, see <u>Section 10.2.2.4</u>). If still a higher multiplication factor is chosen,  $V_{LCD}$  will remain as set by <u>Equation 2</u> but the ripple will increase. The increase in ripple can be counteracted by increasing the external decoupling capacitor at  $V_{LCD}$ . A higher multiplication factor will also result in a higher current consumption (see <u>Section 16.6</u>). However the current that can be delivered will be higher, for example, for larger display area.

When the V<sub>LCD</sub> generator and the direct mode are switched off, an external voltage may be supplied at connected pins V<sub>LCDIN</sub> and V<sub>LCDOUT</sub>. V<sub>LCDIN</sub> and V<sub>LCDOUT</sub> may be higher or lower than V<sub>DD2</sub>.

In direct mode (see Icon\_ctl instruction, <u>Section 10.2.3.3</u>) the internal V<sub>LCD</sub> generator is turned off and the V<sub>LCDOUT</sub> output voltage is directly connected to V<sub>DD2</sub>. This reduces the current consumption depending on V<sub>DD2</sub> value and LCD liquid properties.

The V<sub>LCD</sub> generator ensures that, as long as V<sub>DD2</sub> and V<sub>DD3</sub> are in the valid range (2.2 V to 4 V), the required peak voltage V<sub>LCD</sub> = 6.5 V can be generated at any time.

## 8.5 LCD bias voltage generator

The intermediate bias voltages for the LCD display are also generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of  $V_{LCD}$  depends on the multiplex rate, the LCD threshold voltage ( $V_{th}$ ) and the number of bias levels. Using a 5-level bias scheme for the 1:18 multiplex rate allows  $V_{LCD} < 5 V$  for most LCD liquids.

The intermediate bias levels for the different multiplex rates are shown in <u>Table 7</u>. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

 Table 7.
 Bias levels as a function of multiplex rate

Multiplex	Number of	Bias v	Bias voltages						
rate	bias levels	<b>V</b> <sub>1</sub>	V <sub>2</sub>	V <sub>3</sub>	V <sub>4</sub>	V <sub>5</sub>	V <sub>6</sub>		
1:18	5	V <sub>LCD</sub>	$\frac{3}{4}(V_{LCD} - V_{SS})$	$\frac{l}{2}(V_{LCD} - V_{SS})$	$\frac{1}{2}(V_{LCD} - V_{SS})$	$\frac{l}{4}(V_{LCD} - V_{SS})$	V <sub>SS</sub>		
1:9	5	V <sub>LCD</sub>	$\frac{3}{4}(V_{LCD} - V_{SS})$	$\frac{l}{2}(V_{LCD} - V_{SS})$	$\frac{1}{2}(V_{LCD} - V_{SS})$	$\frac{l}{4}(V_{LCD} - V_{SS})$	V <sub>SS</sub>		
1:2	4	V <sub>LCD</sub>	$\frac{2}{3}(V_{LCD} - V_{SS})$	$\frac{2}{3}(V_{LCD} - V_{SS})$	$\frac{l}{3}(V_{LCD} - V_{SS})$	$\frac{l}{3}(V_{LCD} - V_{SS})$	V <sub>SS</sub>		

The RMS on-state voltage ( $V_{on(RMS)}$ ) for the LCD is calculated with <u>Equation 3</u> and the RMS off-state voltage ( $V_{off(RMS)}$ ) with <u>Equation 4</u>:

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$$V_{on(RMS)} = V_{LCD} \sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}}$$
 (3)

$$V_{off(RMS)} = v_{LCD} \sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}}$$
(4)

where the values of a are

a = 2 for  $\frac{1}{4}$  bias a = 3 for  $\frac{1}{5}$  bias

and the values for n are

n = 2 for 1:2 multiplex rate

n = 9 for 1:9 multiplex rate

n = 18 for 1:18 multiplex rate.

Discrimination (D) is the ratio of V<sub>on(RMS)</sub> to V<sub>off(RMS)</sub> and is determined from Equation 5.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}}$$
(5)

### 8.5.1 Electro-optical performance

Suitable values for  $V_{on(RMS)}$  and  $V_{off(RMS)}$  are dependant on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at  $V_{low}$ ) and the other at 90 % relative transmission (at  $V_{high}$ ), see Figure 3. For a good contrast performance, the following rules should be followed:

$V_{on(RMS)} \ge V_{high}$	(6)
$V_{off(RMS)} \le V_{low}$	(7)

 $V_{on(RMS)}$  and  $V_{off(RMS)}$  are properties of the display driver and are affected by the selection of a, n (see <u>Equation 3</u> to <u>Equation 5</u>) and the V<sub>LCD</sub> voltage.

 $V_{\text{low}}$  and  $V_{\text{high}}$  are properties of the LCD liquid and can be provided by the module manufacturer.

It is important to match the module properties to those of the driver in order to achieve optimum performance.



### 8.6 LCD row and column drivers

The PCF2119x contains 18 row and 80 column drivers, which drive the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. R17 and R18 drive the icon rows. Unused outputs should be left open.

The bias voltages and the timing are selected automatically when the number of lines in the display is selected. Figure 4 to Figure 6 show typical waveforms.

The waveforms used to drive LC displays inherently produce a DC voltage across the display cell. The PCF2119x compensates for the DC voltage by inverting the waveforms on alternate frames (called frame inversion mode or driving scheme A).

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### **NXP Semiconductors**

**PCF2119x** 

LCD controllers/drivers



### **NXP Semiconductors**

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LCD controllers/drivers



# 9. Display data RAM and ROM

### 9.1 DDRAM

The Display Data RAM (DDRAM) stores up to 80 characters of display data represented by 8-bit character codes. RAM locations which are not used for storing display data can be used as general purpose RAM.

The basic RAM to display addressing scheme is shown in <u>Figure 7</u>, <u>Figure 8</u> and <u>Figure 9</u>. With no display shift the characters represented by the codes in the first 32 RAM locations starting at address 00h are displayed in line 1.







When data is written to or read from the DDRAM, wrap-around occurs from the end of one line to the start of the next line. When the display is shifted each line wraps around within itself, independently of the others. Thus all lines are shifted and wrapped around together. The address ranges and wrap-around operations for the various modes are shown in Table 8.

Mode	1 × 32	2 × 16	1 × 16
Address space	00h to 4Fh	00h to 27h; 40h to 67h	00h to 27h
Read/write wrap-around (moves to next line)	4Fh to 00h	27h to 40h; 67h to 00h	27h to 00h
Display shift wrap-around (stays within line)	4Fh to 00h	27h to 00h; 67h to 40h	27h to 00h

#### Table 8. Address space and wrap-around operation

### 9.2 CGROM

The Character Generator ROM (CGROM) contains 240 character patterns in a  $5 \times 8$  dot format from 8-bit character codes. Figure 10 to Figure 15 show the character sets that are currently implemented.

<u> </u>			1	1	1	1	1							1	1		1
lower 4 bits	upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx	0000	1						-	<b>:</b>	· <b>···</b>							
хххх	0001	2	•						•					÷	 F1		
xxxx	0010	3		::					<b>!</b>								
xxxx	0011	4						::::		· 			::				
xxxx	0100	5							1	•			•				
xxxx	0101	6											<b>.</b>				···· ::
xxxx	0110	7	:				÷	Ŧ	:	÷.		:					::
xxxx	0111	8			:					₽.		:;			24	:	•
xxxx	1000	9							:::			••					
xxxx	1001	10					÷	1	·i	÷			4				
xxxx	1010	11		:	:: ::					ľ.			ņ				
xxxx	1011	12	: :		::					<b>[</b> ]-			::				
xxxx	1100	13					•••			-							•••
xxxx	1101	14										••			÷		
xxxx	1110	15	:				••••	<b>!</b> '''	••••	-				• <b>···</b>			
xxxx	1111	16								F.		•••••					

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 10. Character set 'A' in CGROM

ower 1 bits	4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx	0000	1	•							÷			÷	.÷.			÷
хххх	0001	2	<b>.</b>	•				÷.				:::	1				
xxxx	0010	3	-	::									÷				
xxxx	0011	4															
xxxx	0100	5		<b>]</b>	4								÷			¥	
xxxx	0101	6														•	•
xxxx	0110	7					V										
хххх	0111	8		•	÷												
xxxx	1000	9										T	<b>.</b>			<b>.</b>	
хххх	1001	10															
хххх	1010	11		:	•			!		<b>.</b>			•	E.			
хххх	1011	12			•	K	ľ		•	<u>.</u> :	:	<b></b>	÷				
xxxx	1100	13		:	•:					••	••	÷		•••••	·		
xxxx	1101	14		•••••								••••					
xxxx	1110	15		•			•••				1						
хххх	1111	16			:								<u>.</u>				

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are t

Fig 11. Character set 'D' in CGROM

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ower	upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
4 bits	0000	1							:::		.:						:···.
~~~~	0000		*		·•••		•••••	:	÷;	•	•••••		·:	:	:	·	:
хххх	0001	2				4											•:::
хххх	0010	3			<b>.</b>					÷		::					<b></b> .
хххх	0011	4					₽		••••		I			:	:	:	·
хххх	0100	5		••	<u>.</u>				•••				4		Ï		÷
хххх	0101	6	<u>.</u> :	1		• • •			22								
хххх	0110	7		1					÷						÷	÷	<u>ار ا</u>
хххх	0111	8			<b>.</b>						Ŧ		i			•	
хххх	1000	9				-						Ľ.					:::
хххх	1001	10								<b>;;;</b> ;					Ŧ	1	••
хххх	1010	11							÷	ľ	 	:	:: ::				
xxxx	1011	12			::: -:::								::				
хххх	1100	13										:	÷.	<b>.</b>			
xxxx	1101	14	<b>.</b>		*							•••••	•••••				
xxxx	1110	15									<b></b> :	:					
xxxx	1111	16							•							<b>:</b> :::	

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 12. Character set 'F' in CGROM

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lower	upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx	0000	1					<b>.</b>	••					÷				
xxxx	0001	2	·														 
xxxx	0010	3							<b>.</b>			<b>.</b>					
xxxx	0011	4					:	: <u>.</u> .	•	•••••						•	
xxxx	0100	5							÷				•			•	
xxxx	0101	6	••							••			<b>.</b>			•	
xxxx	0110	7							••				•				
xxxx	0111	8			:						::::		::		:::	:	•
xxxx	1000	9		:								••					
xxxx	1001	10					÷		•				1				
xxxx	1010	11		: •	:: ::								<b>i</b>				
xxxx	1011	12			:: ::				÷								
xxxx	1100	13					•••					••••					
xxxx	1101	14		•••••	•••••					<b>.</b>	<b>.</b>	•••			÷		
xxxx	1110	15					••••		•**•	· · · ·	:						<b></b>
xxxx	1111	16										*****	÷				

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 13. Character set 'l' in CGROM

lower 4 bits	upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
хххх	0000	1	-	ŀ	·#·	-			<b></b> :							÷	
xxxx	0001	2															-::::
xxxx	0010	3			<b>.</b>				<b></b> .	<b>:</b>		::					
xxxx	0011	4			1			:	·:		I				:	: <u>.</u> .	·
xxxx	0100	5	•	·									4		I		÷
xxxx	0101	6	::::	1		• • •				÷							
xxxx	0110	7	÷	1		****		÷	÷						÷	÷	••
xxxx	0111	8		·	j÷.						Ŧ	-				•	
xxxx	1000	9							3			1				<b>!</b>	24
xxxx	1001	10								<b>;;;</b> ;						1	••
xxxx	1010	11	·								••••	:4:	# #				
xxxx	1011	12						E.					# ;;	K.			
хххх	1100	13										:		<b>.</b>			
xxxx	1101	14	: 		•							•••••					
xxxx	1110	15														<b>!</b> ''	
xxxx	1111	16							•								

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 14. Character set 'R' in CGROM

LCD controlle	rs/drivers
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lower 4 bits	upper 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
хххх	0000	1														:	
xxxx	0001	2			≣												•:
xxxx	0010	3	·#·	-	ŀ	• • •				: ::::::::::::::::::::::::::::::::::::		::					<b></b> .
хххх	0011	4						•							:;	:	·
хххх	0100	5	•	••									4				÷
хххх	0101	6					:		<b>.</b>								
xxxx	0110	7					<b>.</b>										••
xxxx	0111	8		•	<b>.</b>				<u>.</u>			3	Ĩ			·	
хххх	1000	9					:::		::::			i.					33
xxxx	1001	10				ŀ	<b>.</b>		i (j	<b>;;;</b> ;					Ŧ		·!
xxxx	1010	11	<u></u>						·;;;		••••	: <b>-</b> ::	# #				
хххх	1011	12					<u> </u>		ŧ۳				:				
хххх	1100	13					- <b>‡</b> -					:					
хххх	1101	14			•							•••••					
хххх	1110	15					•					::				<b>!</b> "	
xxxx	1111	16							•••••								

The first column (0000) is the CGRAM, the other 15 columns (0001 to 1111) are the CGROM.

Fig 15. Character set 'S' in CGROM

### 9.3 CGRAM

Up to 16 user defined characters may be stored in the Character Generator RAM (CGRAM). Some CGRAM characters (see Figure 22) are also used to drive icons:

- 8 CGRAM characters if icons blink and both icon rows are used in the application
- 4 CGRAM characters if no icons blink but both icon rows are used in the application
- 0 CGRAM characters if no icons are driven by the icon rows

When the icons blink option is enabled, double the number of CGRAM characters are used since both the on and off state of an icon is defined.

The CGROM and CGRAM use a common address space, of which the first column is reserved for the CGRAM (see Figure 10 to Figure 15). An example of a user defined character is given in Section 16.14 on page 67.



Figure 16 shows the addressing principle for the CGRAM.

be read using the BF AC instruction.

#### Fig 16. Relationship between CGRAM addresses, data and display patterns

### 9.4 Cursor control circuit

The cursor control circuit generates the cursor underline and/or cursor blink as shown in Figure 17 at the DDRAM address contained in the address counter.





# **10. Registers**

The PCF2119x has two 8-bit registers, an instruction register and a data register. Only these two registers can be directly controlled by the microcontroller. Before an internal operation, the control information is stored temporarily in these registers, to allow interfacing to various types of microcontrollers which operate at different speeds or to allow interface to peripheral control ICs.

The instruction set for the parallel interface is shown in <u>Table 12</u> together with their execution time. Details about the parallel interface can be found in <u>Section 11.1</u>. Examples of operations on a 4-bit bus are given in <u>Table 40</u>, on a 8-bit bus in <u>Table 41</u>, <u>Table 42</u> and <u>Table 43</u>.

When using the l<sup>2</sup>C-bus, the instruction has to be commenced with a control byte as shown in <u>Table 9</u>. Details about the l<sup>2</sup>C-bus interface can be found in <u>Section 11.2</u>. An example of operations on the l<sup>2</sup>C-bus is given in <u>Table 44</u>.

#### Table 9. Instruction set for I<sup>2</sup>C-bus commands

Control byte								Com	mand	byte						I <sup>2</sup> C-bus command
СО	RS	0	0	0	0	0	0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	<u>[1]</u>

[1]  $R/\overline{W}$  is set together with the slave address (see <u>Table 34</u>).

#### Table 10.Control byte bit description

Bit	Symbol	Value	Description
7	CO	0	last control byte
		1	another control byte follows after data/command
6	RS	0	instruction register selected
		1	data register selected
5 to 0	-	0	default logic 0

Instructions are of 4 types, those that:

- 1. Designate PCF2119x functions like display format, data length, etc.
- 2. Set internal RAM addresses
- 3. Perform data transfer with internal RAM
- 4. Others, like read 'busy flag' and read 'address counter'

In normal use, type 3 instructions are used most frequently. However, automatic incrementing by 1 (or decrementing by 1) of internal RAM addresses after each data write lessens the microcontroller program load. The display shift in particular can be performed concurrently with display data write, enabling the designer to develop systems in minimum time with maximum programming efficiency.

During internal operation, no instructions other than the BF\_AC instruction will be executed. Because the busy flag is set to logic 1 while an instruction is being executed, check to ensure it is logic 0 before sending the next instruction or wait for the maximum instruction execution time, as given in <u>Table 12</u>. An instruction sent while the busy flag is logic 1 will not be executed.

The RS bit determines which register will be accessed and the  $R/\overline{W}$  bit indicates if it is a read or a write operation (see <u>Table 11</u>).

Symbol	Value	Description
RS		register select
	0	instruction register[1]
	1	data register <sup>[2]</sup>
R/W		read/write
	0	write operation
	1	read operation

Fable 11.	Register	access	selection
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[1] There is only write access to the instruction register, but read access to the busy flag (BF) and the address counter (AC) of the BF\_AC instruction (see Section 10.2.1.2).

[2] Write and read access.

Details of the instructions are explained in subsequent sections.

### 10.1 Data register

The data register temporarily stores data to be read from the DDRAM and CGRAM. Prior to being read by the Read\_data instruction, data from the DDRAM or CGRAM, corresponding to the address in the instruction register, is written to the data register.

### 10.2 Instruction register

The instruction register stores instruction codes such as Clear\_display, Curs\_disp\_shift, and address information for the Display Data RAM (DDRAM) and Character Generator RAM (CGRAM). The instruction register can be written to but not read from by the system controller.

The instruction register is sectioned into basic, standard and extended instructions. Bit H = 1 of the Function\_set instruction (see <u>Section 10.2.1.1</u>) sets the chip into extended instruction set mode.

Instruction	Bits <sup>[1]</sup>										Required	Reference
	RS	R/W	7	6	5	4	3	2	1	0	clock cycles <sup>[2]</sup>	
Basic instructions (	bit H =	0 or 1)	)									
NOP [3]	0	0	0	0	0	0	0	0	0	0	3	-
Function_set	0	0	0	0	1	DL	0	М	SL	Н	3	Section 10.2.1.1
BF_AC	0	1	BF	AC							0	Section 10.2.1.2
Read_data	1	1	READ	_DATA							3	Section 10.2.1.3
Write_data	1	0	WRITI	E_DATA	4						3	Section 10.2.1.4
Standard instruction	ns (bit	H = 0)										
Clear_display	0	0	0	0	0	0	0	0	0	1	165	Section 10.2.2.1
Return_home	0	0	0	0	0	0	0	0	1	0	3	Section 10.2.2.2
Entry_mode_set	0	0	0	0	0	0	0	1	I_D	S	3	Section 10.2.2.3
Display_ctl	0	0	0	0	0	0	1	D	С	В	3	Section 10.2.2.4
Curs_disp_shift	0	0	0	0	0	1	SC	RL	0	0	3	Section 10.2.2.5
Set_CGRAM	0	0	0	1	ACG						3	Section 10.2.2.6
Set_DDRAM	0	0	1	ADD							3	Section 10.2.2.7
Extended instructio	ns (bit	H = 1)										
Reserved [4]	0	0	0	0	0	0	0	0	0	1	-	-
Screen_conf	0	0	0	0	0	0	0	0	1	L	3	Section 10.2.3.1
Disp_conf	0	0	0	0	0	0	0	1	Ρ	Q	3	Section 10.2.3.2
Icon_ctl	0	0	0	0	0	0	1	IM	IB	DM	3	Section 10.2.3.3
Temp_ctl	0	0	0	0	0	1	0	0	TC1	TC2	3	Section 10.2.3.4
HV_gen	0	0	0	1	0	0	0	0	S1	S0	3	Section 10.2.3.5
VLCD_set	0	0	1	V	VA or	VB					3	Section 10.2.3.6

#### Table 12. Instruction register overview

[1] The bits 0 to 7 correspond with the data bus lines DB0 to DB7.

[2] fosc cycles.

[3] No operation.

[4] Do not use.

### 10.2.1 Basic instructions (bit H = 0 or 1)

### 10.2.1.1 Function\_set

Table 13. Function\_set bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 11
R/W	-	0	
7 to 5	-	001	fixed value
4	DL		interface data length (for parallel mode only)
		0 [1]	2 × 4 bits (DB7 to DB4)
		1 [2]	8 bits (DB7 to DB0)
3	-	0	unused

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Bit	Symbol	Value		Description
2	М		<u>[3]</u>	number of display lines
		0		1 line × 32 characters
		1	[4]	2 line × 16 characters
1	SL			multiplex mode
		0		1:18 multiplex drive mode, $1 \times 32$ or $2 \times 16$ character display
		1	[4][5]	1:9 multiplex drive mode, $1 \times 16$ character display
0	Н			instruction set control
		0		basic instruction set plus standard instruction set
		1	[4]	basic instruction set plus extended instruction set

Table 13. Function\_set bit description ... continued

[1] When 4-bit width is selected, data is transmitted in two cycles using the parallel-bus. In a 4-bit application ports DB3 to DB0 should be left open-circuit (internal pull-ups).

- [2] Default value after power-on in l<sup>2</sup>C-bus mode.
- [3] No impact if SL = 1.
- [4] Due to the internal pull-ups on DB3 to DB0 in a 4-bit application, the first Function\_set after power-on sets bits M, SL and H to logic 1. A second Function\_set must be sent to set bits M, SL and H to the required values.
- [5] Independent of bit M and bit L of the Screen\_conf instruction (see Section 10.2.3.1). Only row 1 to row 8 and row 17 are used. All other rows must be left open-circuit. The DDRAM map is the same as in the  $2 \times 16$  character display mode, however, the second line cannot be displayed.

#### 10.2.1.2 BF\_AC instructions

Bit	Symbol	Value	Description
RS	-	0	see Table 11
R/W	-	1	
7	BF	[1]	read busy flag
		0	next instruction will be executed
		1	internal operation is in progress; next instruction will not be executed until BF = 0
6 to 0	AC	0000000 to 1111111	read address counter

#### Table 14. BF\_AC bit

[1] It is recommended that the BF status is checked before the next write operation is started.

**Busy flag:** The busy flag indicates the internal status of the PCF2119x. A logic 1 indicates that the chip is busy and further instructions will not be accepted. The busy flag is output to pin DB7 when bit RS = 0 and bit R/W = 1. Instructions should only be started after checking that the busy flag is at logic 0 or after waiting for the required number of cycles.

Address counter: The address counter is used by both CGRAM and DDRAM, and its value is determined by the previous Set\_CGRAM and Set\_DDRAM instruction. After a read/write operation the address counter is automatically incremented or decremented by <u>1</u>. The address counter value is output to the bus (DB6 to DB0) when bit RS = 0 and bit R/W = 1.

#### 10.2.1.3 Read\_data

#### Table 15. Read\_data bit description

Bit	Symbol	Value	Description
RS	-	1	see <u>Table 11</u>
R/W	-	1	
7 to 0	READ_DATA	00000000 to 11111111	read data from CGRAM or DDRAM

**Read\_data from CGRAM or DDRAM:** Read\_data reads binary 8-bit data from the CGRAM or DDRAM. The most recent 'set address' command (Set\_CGRAM or Set\_DDRAM) determines whether the CGRAM or DDRAM is to be read.

The Read\_data instruction gates the content of the data register to the bus while pin E is HIGH. After pin E goes LOW again, internal operation increments (or decrements) the address counter and stores RAM data corresponding to the new address counter into the data register.

There are only three instructions that update the data register:

- Set\_CGRAM
- Set\_DDRAM
- Read\_data from CGRAM or DDRAM

Other instructions (e.g. Write\_data, Curs\_disp\_shift, Clear\_display and Return\_home) do not modify the value of the data register.

#### 10.2.1.4 Write\_data

#### Table 16. Write\_data bit description

Bit	Symbol	Value	Description
RS	-	1	see Table 11
R/W	-	0	
7 to 0	WRITE_DATA	00000000 to 11111111	write data to CGRAM or DDRAM

Write\_data to CGRAM or DDRAM: Write\_data writes binary 8-bit data to the CGRAM or the DDRAM.

The previous Set\_CGRAM or Set\_DDRAM command determines if data is written into CGRAM or DDRAM. After writing, the address counter automatically increments or decrements by 1, in accordance with the Entry\_mode\_set (see <u>Section 10.2.2.3</u>). Only bit 4 to bit 0 of CGRAM data are valid, bit 7 to bit 5 are 'don't care'.

### **10.2.2** Standard instructions (bit H = 0)

#### 10.2.2.1 Clear\_display

#### Table 17. Clear\_display bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7 to 0	-	00000001	fixed value

**Clear\_display:** writes usually the character code 20h (blank pattern) into all DDRAM addresses except for the character set 'R' where the character code 20h is not a blank pattern.

When using character set 'R', the following alternative instruction set has to be used:

- 1. Switch display off (Display\_ctl, bit D = 0).
- 2. Write a blank pattern into all DDRAM addresses (Write\_data).
- 3. Switch display on (Display\_ctl, bit D = 1).

In addition Clear\_display

- sets the DDRAM address counter to logic 0
- returns the display to its original position, if it was shifted. Thus, the display disappears and the cursor or blink position goes to the left edge of the display
- sets entry mode bit I\_D = 1 (increment mode); bit S of entry mode does not change

The instruction Clear\_display requires extra execution time. This may be allowed by checking the busy flag bit BF or by waiting until the 165 clock cycles have elapsed. The latter must be applied where no read-back options are foreseen, as in some Chip-On-Glass (COG) applications.

#### 10.2.2.2 Return\_home

#### Table 18. Return\_home bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7 to 0	-	0000010	fixed value

**Return\_home:** Sets the DDRAM address counter to logic 0 and switches a shifted display back to an unshifted state. The DDRAM content remain unchanged. The cursor or blink position goes to the left of the first display line. Bit I\_D and bit S of the Entry\_mode\_set instruction remain unchanged.

### 10.2.2.3 Entry\_mode\_set

#### Table 19. Entry\_mode\_set bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7 to 2	-	000001	fixed value
1	I_D		address increment or decrement
		0	DDRAM or CGRAM address decrements by 1, cursor moves to the left
		1	DDRAM or CGRAM address increments by 1, cursor moves to the right
0	S		shift display to the left or right
		0	display does not shift
		1	display shifts

**Bit I\_D:** When bit  $I_D = 1$  the DDRAM or CGRAM address increments by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the right.

When bit  $I_D = 0$  the DDRAM or CGRAM address decrements by 1 when data is written into or read from the DDRAM or CGRAM. The cursor or blink position moves to the left.

The cursor underline and cursor character blink are inhibited when the CGRAM is accessed.

**Bit S:** When bit S = 0, the display does not shift.

During DDRAM write, when bit S = 1 and bit  $I_D = 0$ , the entire display shifts to the right; when bit S = 1 and bit  $I_D = 1$ , the entire display shifts to the left.

Thus it appears as if the cursor stands still and the display moves. The display does not shift when reading from the DDRAM, or when writing to or reading from the CGRAM.

#### 10.2.2.4 Display\_ctl instructions

Bit	Symbol	Value	Description
RS	-	0	see Table 11
R/W	-	0	
7 to 3	-	00001	fixed value
2	D		display on or off
		0	display is off; chip is in power-down mode
		1	display is on
1	С		cursor on or off
		0	cursor is off
		1	cursor is on
0	В		character blink on or off
		0	character blink is off
		1	character blink is on

#### Table 20. Display\_ctl bit description

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**Bit D:** The display is on when bit D = 1 and off when bit D = 0. Display data in the DDRAM is not affected and can be displayed immediately by setting bit D = 1.

When the display is off (bit D = 0) the chip is in partial power-down mode:

- The LCD outputs are connected to V<sub>SS</sub>
- The V<sub>LCD</sub> generator and bias generator are turned off

Three oscillator cycles are required after sending the 'display off' instruction to ensure all outputs are at  $V_{SS}$ , afterwards the oscillator can be stopped. If the oscillator is running during partial power-down mode ('display off') the chip can still execute instructions. Even lower current consumption is obtained by inhibiting the oscillator (pin OSC to  $V_{SS}$ ).

To ensure  $I_{DD} < 1 \ \mu A$ :

- the parallel bus ports DB7 to DB0 should be connected to V<sub>DD</sub>
- pins RS and R/W should be connected to V<sub>DD</sub> or left open-circuit
- pin PD should be connected to V<sub>DD</sub>

Recovery from power-down mode:

- pin PD should be connected back to V<sub>SS</sub>
- if necessary pin OSC should be connected back to  $V_{\text{DD}}$
- a Display\_ctl instruction with bit D = 1 should be sent

**Bit C:** The cursor is displayed when bit C = 1 and inhibited when bit C = 0. Even if the cursor disappears, bit I\_D and bit S (see <u>Section 10.2.2.3</u>) remain in operation during display data write. The cursor is displayed using 5 dots in the 8th line (see Figure 17).

**Bit B:** The character, indicated by the cursor, blinks when bit B = 1. The character blink is displayed by switching between display characters and all dots on with a frequency of

$$f_{blink} = \frac{f_{osc}}{52224}$$

#### 10.2.2.5 Curs\_disp\_shift

#### Table 21. Curs\_disp\_shift bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 11
R/W	-	0	
7 to 4	-	0001	fixed value
3	SC		cursor move or display shift
		0	move cursor
		1	shift display
2	RL		shift or move to the right or left
		0	left shift or move
		1	right shift or move
1 to 0	-	00	fixed value

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**Bits SC and RL:** Curs\_disp\_shift moves the cursor position or the display to the right or left without writing or reading display data. This function is used to correct a character or move the cursor through the display.

In 2-line displays, the cursor moves to the next line when it passes the last position (40) of the line. When the displayed data is shifted repeatedly all lines shift at the same time; displayed characters do not shift into the next line.

The address counter content does not change if the only action performed is shift display (SC = 1) but increments or decrements with the shift cursor (SC = 0).

### 10.2.2.6 Set\_CGRAM

Bit	Symbol	Value	Description
RS	-	0	see Table 11
R/W	-	0	
7 to 6	-	01	fixed value
5 to 0	ACG	000000 to 111111	set CGRAM address

#### Table 22. Set\_CGRAM bit description

**Set\_CGRAM:** Sets the CGRAM address bits ACG[5:0] into the address counter. Data can then be written to or read from the CGRAM.

**Remark:** The CGRAM address uses the same address register as the DDRAM address. This register consists of 7 bits. But with the Set\_CGRAM command, only bit 5 to bit 0 are set. Bit 6 can be set using the Set\_DDRAM command first, or by using the auto-increment feature during CGRAM write. All bits 6 to 0 can be read using the BF\_AC instruction.

When writing to the lower part of the CGRAM, ensure that bit 6 of the address is not set (e.g. by an earlier DDRAM write).

### 10.2.2.7 Set\_DDRAM

#### Table 23. Set\_DDRAM bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7	-	1	fixed value
6 to 0	ADD	0000000 to 1111111	set DDRAM address

**Set\_DDRAM:** Sets the DDRAM address bits ADD[6:0] into the address counter. Data can then be written to or read from the DDRAM.

### **10.2.3** Extended instructions (bit H = 1)

#### 10.2.3.1 Screen\_conf

#### Table 24. Screen\_conf bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7 to 1	-	0000001	fixed value
0	L		screen configuration
		0	split screen standard connection
		1	split screen mirrored connection

#### Screen\_conf:

- If bit L = 0, then the two halves of a split screen are connected in a standard way i.e. column 1/81, 2/82 to 80/160.
- If bit L = 1, then the two halves of a split screen are connected in a mirrored way i.e. column 1/160, 2/159 to 80/81. This allows single layer PCB or glass layout.

### 10.2.3.2 Disp\_conf

#### Table 25. Disp\_conf bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 11
R/W	-	0	
7 to 2	-	000001	fixed value
1	Ρ		display column configuration
		0	column data: left to right;
			column data is displayed from column 1 to column 80
		1	column data: right to left;
			column data is displayed from column 80 to column 1
0	Q		display row configuration
		0	row data: top to bottom;
			row data is displayed from row 1 to row 16 and icon row data in row 17 and row 18
			in single line mode (SL = 1) row data is displayed from row 1 to row 8 and icon row data in row 17
		1	row data: bottom to top;
			row data is displayed from row 16 to row 1 and icon row data in row 18 and row 17
			in single line mode (SL = 1) row data is displayed from row 8 to row 1 and icon row data in row 17

**Bit P:** The P bit is used to flip the display left to right by mirroring the column data, as shown in <u>Figure 19</u>. This allows the display to be viewed from behind instead of front and enhances the flexibility in the assembly of equipment and avoids complicated data manipulation within the controller.


**Bit Q:** The Q bit flips the display top to bottom by mirroring the row data, as shown in Figure 20.



**Combination of bit P and bit Q:** A combination of P and Q allows the display to be rotated horizontally and vertically by 180 degree, as shown in <u>Figure 21</u>. This is useful for viewing the display from the opposite edge.



### 10.2.3.3 lcon\_ctl

Table 26. Icon\_ctl bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7 to 3	-	00001	fixed value

Bit	Symbol	Value	Description
2	IM		icon mode
		0	character mode, full display
		1	icon mode, only icons displayed
1	IB		icon blink
		0	icon blink disabled
		1	icon blink enabled
0	DM		direct mode
		0	off
		1	on

Table 26. Icon\_ctl bit description ... continued

The PCF2119x can drive up to 160 icons. See <u>Figure 22</u> and <u>Figure 23</u> for CGRAM to icon mapping.

**Bit IM:** When bit IM = 0, the chip is in character mode. In the character mode characters and icons are driven (multiplex drive mode 1:18 or 1:9). The V<sub>LCD</sub> generator, if used, produces the V<sub>LCDOUT</sub> voltage programmed with register V<sub>A</sub>.

When bit IM = 1, the chip is in icon mode. In the icon mode only the icons are driven (multiplex drive mode 1:2). The  $V_{LCD}$  generator, if used, produces the  $V_{LCDOUT}$  voltage as programmed with register  $V_B$ .

Bit IM	Mode	V <sub>LCDOUT</sub>
0	character mode	generated from V <sub>A</sub>
1	icon mode	generated from V <sub>B</sub>

Bit IB: Icon blink control is independent of the cursor/character blink function.

When bit IB = 0, the icon blink is disabled. Icon data is stored in CGRAM character 0 to 3  $(4 \times 8 \times 5 = 160 \text{ bits for } 160 \text{ icons}).$ 

When bit IB = 1, the icon blink is enabled. In this case each icon is controlled by two bits. Blink consists of two half phases (corresponding to the cursor on and off phases called even and odd phases hereafter).

Icon states for the even phase are stored in CGRAM characters 0 to 3  $(4 \times 8 \times 5 = 160 \text{ bits for } 160 \text{ icons})$ . These bits also define icon state when icon blink is not used (see Table 28).

Icon states for the odd phase are stored in CGRAM character 4 to 7 (another 160 bits for the 160 icons). When icon blink is disabled CGRAM characters 4 to 7 may be used as normal CGRAM characters.

Table 28.	Blink effect	for	icons and	cursor	character	blink
-----------	--------------	-----	-----------	--------	-----------	-------

Parameter	Even phase	Odd phase
cursor character blink	block (all on)	normal (display character)
icons	state 1; CGRAM character 0 to 3	state 2; CGRAM character 4 to 7



icon no.	phase	ROW/COL			char	acte	er co	odes	3			CC	GRA	M a	ddre	ess		(	CGF	RAM	da	ta	icon view
			7 MSE	6 3	5	4	3	2	1	0 LSB	6 MSE	5 3	4	3	2	1	0 LSB	4 MSI	3 3	2	1	0 LSB	
1-5	even	17/1-5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	
6-10	even	17/6-10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	
11-15	even	17/11-15	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0	
1	I	I					I				1			Ι				1		Ι			1
76-80	even	17/76-80	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	
81-85	even	18/1-5	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	1	0	0	0	
I	I	I					I							I				1		I			1
156-160	even	18/76-80	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	0	1	
1-5	odd (blink)	17/1-5	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	
I	I	I					I				   			Ι				   		I			1
156-160	odd (blink)	18/76-80	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	0	0	1	1	0	

CGRAM data: logic 1 of a data bit turns the icon on and logic 0 turns the icon off.

Character codes: bits 0 to 3 define the icon state when icon blink is disabled or during the even phase when icon blink is enabled. Bits 4 to 7 define the icon state during the odd phase when icon blink is enabled (not used for icons when icon blink is disabled)

### Fig 23. CGRAM to icon mapping (b)

**Bit DM:** When DM = 0, the chip is not in the direct mode. Either the internal  $V_{LCD}$  generator or an external voltage may be used to achieve  $V_{LCD}$ .

When DM = 1, the chip is in direct mode. The internal  $V_{LCD}$  generator is turned off and the output  $V_{LCDOUT}$  is directly connected to  $V_{DD2}$  (i.e. the  $V_{LCD}$  generator supply voltage).

**Remark:** In direct mode, no external V<sub>LCD</sub> is possible.

The direct mode can be used to reduce the current consumption when the required output voltage  $V_{LCDOUT}$  is close to the  $V_{DD2}$  supply voltage. This can be the case in icon mode or in MUX 1:9 (depending on LCD liquid properties).

### 10.2.3.4 Temp\_ctl

#### Table 29. Temp\_ctl bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7 to 2	-	000100	fixed value
1 to 0	TC[1:0]	00 to 11	temperature coefficient

The bit-field TC[1:0] selects the temperature coefficient for the internally generated  $V_{LCDOUT}$  (see Table 30).

Table 30.	TC[1:0]	selection of \	V <sub>LCD</sub>	temperature	coefficient
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TC[1:0]	Typical value	Description
00	–0.16 %/K	V <sub>LCD</sub> temperature coefficient 0 (default value)
10	–0.18 %/K	V <sub>LCD</sub> temperature coefficient 1
01	–0.21 %/K	V <sub>LCD</sub> temperature coefficient 2
11	–0.24 %/K	V <sub>LCD</sub> temperature coefficient 3

### 10.2.3.5 HV\_gen

### Table 31.HV\_gen bit description

Bit	Symbol	Value	Description
RS	-	0	see <u>Table 11</u>
R/W	-	0	
7 to 2	-	010000	fixed value
1 to 0	S[1:0]	00 to 11	voltage multiplier

A software configurable voltage multiplier is incorporated in the  $V_{LCD}$  generator and can be set via the HV\_gen command. The voltage multiplier control can be used to reduce current consumption by disconnecting internal voltage multiplier stages, depending on the required  $V_{LCDOUT}$  output voltage (see <u>Table 32</u>).

### Table 32. Voltage multiplier control bits

S[1:0]	Description
00	set $V_{LCD}$ generator stages to 1 (2 × voltage multiplier)
01	set $V_{LCD}$ generator stages to 2 (3 × voltage multiplier)
10	set $V_{LCD}$ generator stages to 3 (4 $\times$ voltage multiplier)
11	do not use

### 10.2.3.6 VLCD\_set

#### Table 33. VLCD\_set bit description

Bit	Symbol	Value	Description
RS	-	0	see Table 11
R/W	-	0	
7	-	1	fixed value

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Bit	Symbol	Value	Description	
6	V		set register $V_A$ or $V_B$	
		0	set register V <sub>A</sub>	
		1	set register V <sub>B</sub>	
5 to 0	$V_A$ or $V_B$	000000 to 111111	factor for calculating V <sub>LCD</sub>	

Table 33.	VLCD_	set bit	description	continued
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The V<sub>LCD</sub> value is calculated with the <u>Equation 2 on page 9</u>. The multiplication factor is programmed by instruction. Two on-chip registers (V<sub>A</sub> and V<sub>B</sub>) hold the multiplication factor for the character mode and the icon mode, respectively. The generated V<sub>LCDOUT</sub> value is independent of V<sub>DD</sub>, allowing battery operation of the chip.

V<sub>x</sub> programming:

- 1. Send Function\_set instruction with bit H = 1.
- 2. Send VLCD\_set instruction to write to the voltage register:
  - a. Bit 7 = 1 and bit 6 = 0: bit 5 to bit 0 are the multiplication factor for  $V_{LCD}$  of character mode ( $V_A$ ).
  - b. Bit 7 = 1 and bit 6 = 1: bit 5 to bit 0 are the multiplication factor for  $V_{LCD}$  of icon mode ( $V_B$ ).
  - c. Bit 5 to bit 0 = 0 switches  $V_{LCD}$  generator off (when selected).
  - d. During 'display off'/power-down the V<sub>LCD</sub> generator is also disabled.
- 3. Send Function\_set instruction with bit H = 0 to resume normal programming.

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### **11. Basic architecture**

### **11.1 Parallel interface**

The PCF2119x can send data in either two 4-bit operations or one 8-bit operation and can thus interface to 4-bit or 8-bit microcontrollers.

In 8-bit mode data is transferred as 8-bit bytes using the 8 ports DB7 to DB0. Three further control lines E, RS and R/W are required.

In 4-bit mode data is transferred in two cycles of 4 bits each using ports DB7 to DB4 for the transaction. The higher order bits (corresponding to range of bit 7 to bit 4 in 8-bit mode) are sent in the first cycle and the lower order bits (bit 3 to bit 0 in 8-bit mode) in the second cycle. Data transfer is complete after two 4-bit data transfers. It should be noted that two cycles are also required for the busy flag check. 4-bit operation is selected by instruction (see Figure 24 to Figure 26 for examples of bus protocol).

In 4-bit mode, ports DB3 to DB0 must be left open-circuit. They are pulled up to  $V_{\text{DD}}$  internally.



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### **11.2** I<sup>2</sup>C-bus interface

The I<sup>2</sup>C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are the Serial DAta line (SDA) and the Serial CLock line (SCL). Both lines must be connected to a positive supply via pull-up resistors. Data transfer may be initiated only when the bus is not busy.

Each byte of eight bits is followed by an acknowledge bit. A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

A master receiver must signal an end of data to the transmitter by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.



### Fig 27. System configuration





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### 11.2.1 I<sup>2</sup>C-bus protocol

Two  $l^2C$ -bus slave addresses (0111 010 and 0111 011) are reserved for the PCF2119x. The entire  $l^2C$ -bus slave address byte is shown in Table 34.

### Table 34.I<sup>2</sup>C slave address byte

	Slave address							
Bit	7	6	5	4	3	2	1	0
	MSB							LSB
	0	1	1	1	0	1	SA0	R/W

Bit 1 of the slave address byte, that a PCF2119x will respond to, is defined by the level tied to its SA0 input ( $V_{SS}$  for logic 0 and  $V_{DD}$  for logic 1).

Before any data is transmitted on the I<sup>2</sup>C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the START procedure.

The  $I^2$ C-bus configuration for the different PCF2119x read and write cycles is shown in Figure 31 to Figure 33.

The slow down feature of the I<sup>2</sup>C-bus protocol (receiver holds SCL line LOW during internal operations) is not used in the PCF2119x.

### 11.2.2 I<sup>2</sup>C-bus definitions

Definitions:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device addressed by a master.
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message.

- Arbitration: procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: procedure to synchronize the clock signals of two or more devices.



### Fig 31. Master transmits to slave receiver; write mode



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### 11.3 Safety notes

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

### CAUTION



Static voltages across the liquid crystal display can build up when the LCD supply voltage ( $V_{LCD}$ ) is on while the IC supply voltage ( $V_{DD}$ ) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts,  $V_{LCD}$  and  $V_{DD}$  must be applied or removed together.

### CAUTION



Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

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## 12. Internal circuitry

Table 35. De	evice protection	circuits
Symbol	Pin	Internal circuit
V <sub>DD1</sub>	1 to 6	V <sub>DD1</sub> V <sub>SS1</sub> 013aaa169
V <sub>DD2</sub>	7 to 14	$V_{DD2}$ $V_{SS1}$ $V_{SS2}$ $013aaa170$
V <sub>DD3</sub>	15 to 18	VDD3 VSS1 013aaa171
V <sub>SS1</sub>	22 to 29	
V <sub>SS2</sub>	30 to 35	V <sub>SS2</sub> V <sub>SS1</sub> 013aaa172
V <sub>LCDSENSE</sub>	36	
V <sub>LCDIN</sub>	44 to 49	$\mathbf{A}$
V <sub>LCDOUT</sub>	37 to 43	V <sub>SS1</sub>
SCL	151 to 152	013aaa173
SDA	156 to 157	
OSC	168	
PD	155	VDD1
POR	154	
T1	20	<b></b>
T2	21	
Т3	153	013aaa174
E	19	
RS	159	
R/W	158	
DB0 to DB7	160 to 167	
R1 to R18	58, 57 to 51, 142 to 149, 59, 100, 141	
C1 to C80	140 to 101, 99 to 60	V <sub>SS1</sub> 013aaa175

### 13. Limiting values

Table 36.LinIn accordance	n <mark>iting values</mark> with the Absolute Maximum Rati	ng System (IEC 60	)134	).		
Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DD1</sub>	supply voltage 1	logic		-0.5	+6.5	V
V <sub>DD2</sub>	supply voltage 2	V <sub>LCD</sub> generator		-0.5	+4.5	V
V <sub>DD3</sub>	supply voltage 3					
V <sub>LCD</sub>	LCD supply voltage			-0.5	+7.5	V
VI	input voltage	V <sub>DD</sub> related		-0.5	+6.5	V
		V <sub>LCD</sub> related		-0.5	+7.5	V
l <sub>l</sub>	input current	DC current	[1]	-10	+10	mA
lo	output current	DC current	[1]	-10	+10	mA
I <sub>DD</sub>	supply current			-50	+50	mA
I <sub>SS</sub>	ground supply current			-50	+50	mA
I <sub>DD(LCD)</sub>	LCD supply current			-50	+50	mA
P <sub>tot</sub>	total power dissipation			-	400	mW
Po	output power	dissipation per output		-	100	mW
V <sub>ESD</sub>	electrostatic discharge voltage	НВМ	[2]	-	±3000	V
		MM	[3]	-	±300	V
l <sub>lu</sub>	latch-up current		[4]	-	200	mA
T <sub>stg</sub>	storage temperature		[5]	-65	+150	°C
T <sub>amb</sub>	ambient temperature	operating device		-40	+85	°C

[1] For all diode protected input and output pins.

[2] Pass level; Human Body Model (HBM) according to Ref. 7 "JESD22-A114".

[3] Pass level; Machine Model (MM), according to Ref. 8 "JESD22-A115".

[4] Pass level; latch-up testing according to Ref. 9 "JESD78" at maximum ambient temperature (T<sub>amb(max)</sub>).

[5] According to the store and transport requirements (see <u>Ref. 12 "UM10569</u>") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

### 14. Static characteristics

### Table 37. Static characteristics

 $V_{DD1} = 1.5 \text{ V to } 5.5 \text{ V}; V_{DD2} = V_{DD3} = 2.2 \text{ V to } 4.0 \text{ V}; V_{SS} = 0 \text{ V}; V_{LCD} = 2.2 \text{ V to } 6.5 \text{ V}; T_{amb} = -40 \text{ °C to } +85 \text{ °C};$ unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Supplies							
V <sub>DD1</sub>	supply voltage 1	logic		1.5	-	5.5	V
V <sub>DD2</sub>	supply voltage 2	internal V <sub>LCD</sub> generation;		2.2	-	4.0	V
V <sub>DD3</sub>	supply voltage 3	$V_{LCD} > V_{DD2} = V_{DD3}$					
V <sub>LCD</sub>	LCD supply voltage	pins V <sub>LCD</sub> , V <sub>LCDIN</sub> , V <sub>LCDOUT</sub>		2.2	-	6.5	V
Ground supply	current using external V <sub>LCE</sub>	<u>[]</u>					
I <sub>SS</sub>	ground supply current			-	70	120	μA
		V <sub>DD</sub> = 3 V; V <sub>LCD</sub> = 5 V	[2]	-	35	80	μA
		icon mode; $V_{DD} = 3 V$ ; $V_{LCD} = 2.5 V$	[2]	-	25	45	μA
		power-down mode; $V_{DD} = 3 V$ ; $V_{LCD} = 2.5 V$ ; DB7 to DB0, RS and R/W = 1; OSC = 0; PD = 1		-	0.5	5	μA
Ground supply	current using internal V <sub>LCD</sub>	[1][3]			•		
I <sub>SS</sub>	ground supply current			-	190	400	μA
		V <sub>DD</sub> = 3 V; V <sub>LCD</sub> = 5 V	[2]	-	135	400	μA
		icon mode; $V_{DD}$ = 2.5 V; $V_{LCD}$ = 2.5 V	[2]	-	85	-	μA
Logic		·					
VI	input voltage			-0.5	-	V <sub>DD1</sub> + 0.5	V
V <sub>IL</sub>	LOW-level input voltage			V <sub>SS1</sub>	-	0.3V <sub>DD1</sub>	V
V <sub>IH</sub>	HIGH-level input voltage			0.7V <sub>DD1</sub>	-	V <sub>DD1</sub>	V
Oscillator input	t; pin OSC						
V <sub>IL</sub>	LOW-level input voltage			V <sub>SS1</sub>	-	V <sub>DD1</sub> - 1.2	V
VIH	HIGH-level input voltage			$V_{DD1}-0.1$	-	V <sub>DD1</sub>	V
Data bus; pins	DB7 to DB0						
I <sub>OL</sub>	LOW-level output current	output sink current; V <sub>OL</sub> = 0.4 V; V <sub>DD1</sub> = 5 V		1.6	4	-	mA
I <sub>ОН</sub>	HIGH-level output current	output source current; $V_{OH} = 4 V$ ; $V_{DD1} = 5 V$		1	8	-	mA
I <sub>pu</sub>	pull-up current	$V_{I} = V_{SS1}$		0.04	0.15	1	μA
ΙL	leakage current	$V_{I} = V_{DD1, 2, 3} \text{ or } V_{SS1, 2}$		-1	-	+1	μA
I <sup>2</sup> C-bus; pins	SDA and SCL	<u>.</u>					
Inputs: pins SE	A and SCL						
VI	input voltage		[4]	-0.5	-	5.5	V
V <sub>IL</sub>	LOW-level input voltage			0	-	0.3V <sub>DD1</sub>	V
V <sub>IH</sub>	HIGH-level input voltage			0.7V <sub>DD1</sub>	-	5.5	V
ILI	input leakage current	$V_{I} = V_{DD1, 2, 3} \text{ or } V_{SS1, 2}$		-1	-	+1	μA

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### Table 37. Static characteristics ...continued

 $V_{DD1} = 1.5$  V to 5.5 V;  $V_{DD2} = V_{DD3} = 2.2$  V to 4.0 V;  $V_{SS} = 0$  V;  $V_{LCD} = 2.2$  V to 6.5 V;  $T_{amb} = -40$  °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C <sub>i</sub>	input capacitance			-	5	-	pF
Output: pin SD	A						
I <sub>OL</sub>	LOW-level output current	output sink current					
		$V_{OL} = 0.4 \text{ V}; V_{DD1} > 2 \text{ V}$		3	-	-	mA
		$V_{OL} = 0.2 V_{DD1}; V_{DD1} < 2 V$		2	-	-	mA
LCD outputs							
R <sub>O</sub>	output resistance	row output, pins R1 to R18	[5]	-	10	30	kΩ
		column output, pins C1 to C80	[5]	-	15	40	kΩ
$\Delta V_{bias}$	bias voltage variation	on pins R1 to R18 and C1 to C80	<u>[6]</u>	-	20	130	mV
$\Delta V_{LCD}$	LCD voltage variation	T <sub>amb</sub> = 25 °C	[3]				
		V <sub>LCD</sub> < 3 V		-	-	160	mV
		$V_{LCD} < 4 V$		-	-	200	mV
		V <sub>LCD</sub> < 5 V		-	-	260	mV
		V <sub>LCD</sub> < 6 V		-	-	340	mV

[1] LCD outputs are open-circuit; inputs at  $V_{DD}$  or  $V_{SS}$ ; bus inactive.

[2]  $T_{amb} = 25 \circ C$ ;  $f_{osc(ext)} = 200 \text{ kHz}$ .

[3] LCD outputs are open-circuit;  $V_{LCD}$  generator is on; load current  $I_{LCD} = 5 \ \mu A$ .

[4] The I<sup>2</sup>C-bus interface of PCF2119x is 5 V tolerant.

[5] Resistance of output pins (R1 to R18 and C1 to C80) with a load current of 10  $\mu$ A; outputs measured one at a time; external LCD supply V<sub>LCD</sub> = 3 V; V<sub>DD1</sub> = V<sub>DD2</sub> = V<sub>DD3</sub> = 3 V.

[6] LCD outputs open-circuit; external LCD supply.

### **15. Dynamic characteristics**

### Table 38. Dynamic characteristics

 $V_{DD1} = 1.5 \text{ V to } 5.5 \text{ V}; V_{DD2} = V_{DD3} = 2.2 \text{ V to } 4.0 \text{ V}; V_{SS} = 0 \text{ V}; V_{LCD} = 2.2 \text{ V to } 6.5 \text{ V}; T_{amb} = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C} \text{ }^{\circ}\text{C}; unless = -40 \text{ }^{\circ}\text{C}; u$ otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Clock and osc	illator	1	J	1	1	1
f <sub>fr(LCD)</sub>	LCD frame frequency	internal clock; $V_{DD} = 5.0 V$	45	95	147	Hz
f <sub>osc</sub>	oscillator frequency	not available at any pin	140	250	450	kHz
f <sub>osc(ext)</sub>	external oscillator frequency		140	-	450	kHz
t <sub>d(startup)(OSC)</sub>	start-up delay time on pin OSC	oscillator, after power-down	-	200	300	μs
Timing charac	teristics of parallel interface <sup>[2]</sup>					
Write operation	(writing data from microcontrolle	r to PCF2119x); see Figure 34				
t <sub>cy(en)</sub>	enable cycle time		500	-	-	ns
t <sub>w(en)</sub>	enable pulse width		220	-	-	ns
t <sub>su(A)</sub>	address set-up time		50	-	-	ns
t <sub>h(A)</sub>	address hold time		25	-	-	ns
t <sub>su(D)</sub>	data input set-up time		60	-	-	ns
t <sub>h(D)</sub>	data input hold time		25	-	-	ns
Read operation	reading data from PCF2119x to	microcontroller); see Figure 35				
t <sub>cy(en)</sub>	enable cycle time		500	-	-	ns
t <sub>w(en)</sub>	enable pulse width		220	-	-	ns
t <sub>su(A)</sub>	address set-up time		50	-	-	ns
t <sub>h(A)</sub>	address hold time		25	-	-	ns
t <sub>d(DV)</sub>	data input valid delay time	V <sub>DD1</sub> > 2.2 V	-	-	150	ns
		V <sub>DD1</sub> > 1.5 V	-	-	250	ns
t <sub>h(D)</sub>	data input hold time		20	-	100	ns
Timing charac	teristics of I <sup>2</sup> C-bus interface <sup>[2]</sup> ;	see Figure 36				
f <sub>SCL</sub>	SCL clock frequency		-	-	400	kHz
t <sub>LOW</sub>	LOW period of the SCL clock		1.3	-	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		0.6	-	-	μs
t <sub>SU;DAT</sub>	data set-up time		100	-	-	ns
t <sub>HD;DAT</sub>	data hold time		0	-	-	ns
t <sub>r</sub>	rise time of both SDA and SCL signals	<u>[1][3]</u>	15 + 0.1 C <sub>b</sub>	-	300	ns
t <sub>f</sub>	fall time of both SDA and SCL signals	[1][3]	15 + 0.1 C <sub>b</sub>	-	300	ns
C <sub>b</sub>	capacitive load for each bus line		-	-	400	pF
t <sub>SU;STA</sub>	set-up time for a repeated START condition		0.6	-	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		0.6	-	-	μs

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#### Table 38. Dynamic characteristics ...continued

 $V_{DD1} = 1.5 \text{ V to } 5.5 \text{ V}; V_{DD2} = V_{DD3} = 2.2 \text{ V to } 4.0 \text{ V}; V_{SS} = 0 \text{ V}; V_{LCD} = 2.2 \text{ V to } 6.5 \text{ V}; T_{amb} = -40 \text{ °C to } +85 \text{ °C}; unless \text{ V}$ otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>SU;STO</sub>	set-up time for STOP condition		0.6	-	-	μS
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	-	50	ns
t <sub>BUF</sub>	bus free time between a STOP and START condition		1.3	-	-	μS

[1] Tested on sample base.

All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V<sub>IL</sub> and V<sub>IH</sub> with an [2] input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

[3]  $C_b$  = total capacitance of one bus line in pF.



### Fig 34. Parallel bus write operation sequence; writing data from microcontroller to **PCF2119x**



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### **16. Application information**

### 16.1 General application information

Experience showed that the external capacitors (Cext) in an application should be

- from pins  $V_{LCD}$  to  $V_{SS} \ge 100 \text{ nF}$  and
- for pins  $V_{DD}$  to  $V_{SS} \ge 470$  nF.

Higher capacitor values are recommended for ripple reduction, but depending on the application lower values may also lead to a good optical performance. The most suitable capacitor values can be found by testing the application and can be applied as long as they do not violate the specifications given in <u>Section 13</u> to <u>Section 15</u>. The capacitors should be placed as close as possible to the display connections on the PCB.

For COG applications the recommended ITO track resistance is to be minimized for the I/O and supply connections. Optimized values for these tracks are below 50  $\Omega$  for the supply and below 100  $\Omega$  for the I/O connections. Higher track resistance reduce performance and increase current consumption. To avoid accidental triggering of Power-On Reset (POR) (especially in COG applications), the supplies must be adequately decoupled. Depending on power supply quality, V<sub>DD1</sub> may have to be risen above the specified minimum.

When external LCD supply voltage is supplied,  $V_{LCDOUT}$  should be left open-circuit to avoid any stray current, and  $V_{LCDIN}$  must be connected to  $V_{LCDSENSE}$ .

The PCF2119x l<sup>2</sup>C-bus interface is compatible with systems, where the l<sup>2</sup>C pull-up resistors are connected to a 5 V  $\pm$ 10 % supply.



### 16.2 Power supply connections for internal V<sub>LCD</sub> generation

The value of the capacitor should be at least 100 nF. Fig 38. Recommended  $V_{LCD}$  connections for internal  $V_{LCD}$  generation

## 16.3 Power supply connections for external V<sub>LCD</sub> generation



PCF2119X **Product data sheet**  **Remark:** When using an external  $V_{LCD}$ , the internal  $V_{LCD}$  generator **must never** be switched on and direct mode must be avoided otherwise damages will occur.

### **16.4** Information about V<sub>LCD</sub> connections

 $V_{LCDIN}$  — This input is used for generating the 5 LCD bias levels. It is the power supply for the bias level buffers.

 $V_{LCDOUT}$  — This is the V<sub>LCD</sub> output if V<sub>LCD</sub> is generated internally. In this case pin V<sub>LCDOUT</sub> must be connected to V<sub>LCDIN</sub> and to V<sub>LCDSENSE</sub>. If V<sub>LCD</sub> is generated externally, V<sub>LCDOUT</sub> must be left unconnected.

 $V_{LCDSENSE}$  — This input is used for the voltage multiplier's regulation circuitry. When using the internal V<sub>LCD</sub> generation, this pin must be connected to V<sub>LCDOUT</sub> and V<sub>LCDIN</sub>. When using an external V<sub>LCD</sub> supply it must be connected to V<sub>LCDIN</sub> only.

### 16.5 Reducing current consumption

Reducing current consumption can be achieved by one of the options given in Table 39.

When  $V_{LCD}$  lies outside the  $V_{DD}$  range and must be generated, it is usually more efficient to use the on-chip  $V_{LCD}$  generator than an external regulator.

Original mode	Alternative mode
character mode	icon mode (control bit IM)
display on	display off (control bit D)
V <sub>LCD</sub> generator operating	direct mode
any mode	power-down mode (pin PD)

### Table 39. Reducing current consumption

### 16.6 Charge pump characteristics

Typical graphs of the total power consumption of the PCF2119x using the internal charge pump are illustrated in Figure 41, Figure 42 and Figure 43.

The graphs were obtained under the following conditions:

- T<sub>amb</sub> = 25 °C
- $V_{DD1} = V_{DD2} = V_{DD3} = 2.2 V$  (minimum), 2.7 V (typical) and 4.0 V (maximum)
- Normal mode
- f<sub>osc</sub> = internal oscillator
- multiplex drive mode 1:18
- Typical current load for  $I_{LCD} = 10 \ \mu A$ .

For each multiplication factor there is a separate line. The line ends where it is not possible to get a higher voltage under its conditions (a higher multiplication factor is needed to get higher voltages).

Connecting different displays may result in different current consumption. This affects the efficiency and the optimum multiplication factor to be used to generate a certain output voltage.

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### 16.7 Interfaces



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### 16.8 Connections with LCD modules



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### 16.9 4-bit operation, 1-line display using external reset

The program must set functions prior to a 4-bit operation (see <u>Table 40</u>). When power is turned on, 8-bit operation is automatically selected and the PCF2119x attempts to perform the first write as an 8-bit operation. Since nothing is connected to ports DB0 to DB3, a rewrite is then required. However, since one operation is completed in two accesses of 4-bit operation, a rewrite is required to set the functions (see <u>Table 40</u> step 3). Thus, DB4 to DB7 of the Function\_set are written twice.

Step	Instru	uction	1				Display	Operation			
	RS	R/W	DB7	DB6	DB5	DB4					
1	powe	r supp	ly on					initialized by the external reset; no display appears			
2	Func	tion_s	et					sets to 4-bit operation; in this instance operation is handled as			
	0	0	0	0	1	0		8-bit by initialization and only this instruction completes with one write			
3	Func	tion_s	et					sets to 4-bit operation, selects 1-line display and $V_{LCD} = V_0$ ;			
	0	0	0	0	1	0		4-bit operation starts from this point and resetting is needed			
	0	0	0	0	0	0					
4	Displa	ay_ctl						turns display and cursor on; entire display is blank after			
	0	0	0	0	0	0	_	initialization			
	0	0	1	1	1	0					
5	Entry	_mode	e_set					sets mode to increment the address by 1 and to shift the cursor			
	0	0	0	0	0	0	_	to the right at the time of write to the DDRAM or CGRAM;			
	0	0	0	1	1	0					
6	Write	_data	to CG	RAM/I	DDRA	М		writes 'P'; the DDRAM has already been selected by			
	1	0	0	1	0	1	P_	initialization at power-on; the cursor is incremented by 1 and shifted to the right			
	1	0	0	0	0	0					

### Table 40. 4-bit operation, 1-line display example; using external reset (character set 'A')

### 16.10 8-bit operation, 1-line display using external reset

Table 41 and Table 42 show an example of a 1-line display in 8-bit operation. The PCF2119x functions must be set by the Function\_set instruction prior to display. Since the DDRAM can store data for 80 characters, the RAM can be used for advertising displays



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when combined with display shift operation. Since the display shift operation changes display position only and the DDRAM contents remain unchanged, display data entered first can be displayed when the Return\_home operation is performed.

 Table 41.
 8-bit operation, 1-line display example; using external reset (character set 'A')

Step	Instr	uctior	n							Display	Operation	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-	
1	powe	er supp	oly on							-		initialized by the external reset; no display appears
2	Func	tion_s	et									sets to 8-bit operation, selects 1-line
	0	0	0	0	1	1	0	0	0	0		display and $V_{LCD} = V_0$
3	Displ	ay_ctl										turns on display and cursor; entire
	0	0	0	0	0	0	1	1	1	0	_	display is blank after initialization
4	Entry	_mod	e_set									sets mode to increment the address
	0	0	0	0	0	0	0	1	1	0	-	by 1 and to shift the cursor to the right at the time of the write to the DDRAM/CGRAM; display is not shifted
5	Write	_data	to CG	RAM/	DDRA	М						writes 'P'; the DDRAM has already
	1	0	0	1	0	1	0	0	0	0	P_	been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right
6	Write	_data	to CG	RAM/	DDRA	M						writes 'H'
	1	0	0	1	0	0	1	0	0	0	PH_	_
7 to 10						:					PHILIP_	writes 'ILIP'
11	Write	_data	to CG	RAM/	DDRA	М						writes 'S'
	1	0	0	1	0	1	0	0	1	1	PHILIPS_	_
12	Entry	_mod	e_set									sets mode for display shift at the time
	0	0	0	0	0	0	0	1	1	1	PHILIPS_	of write
13	Write	_data	to CG	RAM/	DDRA	M						writes space
	1	0	0	0	1	0	0	0	0	0	HILIPS _	_
14	Write	_data	to CG	RAM/	DDRA	М						writes 'M'
	1	0	0	1	0	0	1	1	0	1	ILIPS M_	_
15 to 19						:					MICROK	writes 'ICROK'
20	Write	_data	to CG	RAM/	DDRA	М						writes 'O'
	1	0	0	1	0	0	1	1	1	1	MICROKO_	
21	Curs	_disp_	shift									shifts only the cursor position to the left
	0	0	0	0	0	1	0	0	0	0		_
22	Curs	_disp_	shift									shifts only the cursor position to the left
	0	0	0	0	0	1	0	0	0	0	MICRO <u>K</u> O	_
23	Write	_data	to CG	RAM/	DDRA	M						writes 'C' correction; display moves to
	1	0	0	1	0	0	0	0	1	1	ICROC <u>O</u>	the left
24	Curs	_disp_	shift									shifts the display and cursor to the
	0	0	0	0	0	1	1	1	0	0		right
25	Curs	_disp_	shift									shifts only the cursor to the right
	0	0	0	0	0	1	0	1	0	0	MICROCO	

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### Table 41. 8-bit operation, 1-line display example; using external reset (character set 'A') ... continued

Step	Instr	uction	1								Display	Operation
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
26	Write	_data	to CG	RAM/	DDRA	М						writes 'M'
	1	0	0	1	0	0	1	1	0	1	ICROCOM_	-
27	Retu	n_hor	ne								returns both display and cursor to the	
	0	0	0	0	0	0	0	0	1	0	PHILIPS M	original position (address 0)

### Table 42. 8-bit operation, 1-line display and icon example; using external reset (character set 'A')

Step	Instr	uctior	า								Display	Operation			
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	-				
1	powe	er supp	oly on									initialized by the external reset; no display appears			
2	Func	tion_s	et									sets to 8-bit operation, selects 1-line			
	0	0	0	0	1	1	0	0	0	0		display and $V_{LCD} = V_0$			
3	Displ	ay_ctl										turns on display and cursor; entire			
	0	0	0	0	0	0	1	1	1	0	_	display is blank after initialization			
4	Entry	/_mod	e_set									sets mode to increment the address			
	0	0	0	0	0	0	0	1	1	0	-	by 1 and to shift the cursor to the right at the time of the write to the DD/CGRAM; display is not shifted			
5	Set_	CGRA	М									sets the CGRAM address to position of			
	0	0	0	1	0	0	0	0	0	0	_	character 0; the CGRAM is selected			
6	Write	_data	to CG	RAM/	DDRA	М						writes data to CGRAM for icon even			
	1	0	0	0	0	0	1	0	1	0	_	phase; icons appears			
7						:					_				
8	Set_	CGRA	М									sets the CGRAM address to position of			
	0	0	0	1	1	1	0	0	0	0	_	character 4; the CGRAM is selected			
9	Write	_data	to CG	RAM/	DDRA	М						writes data to CGRAM for icon odd			
	1	0	0	0	0	0	1	0	1	0	_	phase			
10						:					_				
11	Func	tion_s	et									sets bit H = 1			
	0	0	0	0	1	1	0	0	0	1	_				
12	Icon_	ctl										icons blink			
	0	0	0	0	0	0	1	0	1	0	_				
13	Func	tion_s	et									sets bit H = 0			
	0	0	0	0	1	1	0	0	0	1	_				
14	Set_	DDRA	M			1				1		sets the DDRAM address to the first			
	0	0	1	0	0	0	0	0	0	0		position; DDRAM is selected			
15	Write	_data	to CG	RAM/	DDRA	M				1		writes 'P'; the cursor is incremented			
	1	0	0	1	0	1	0	0	0	0	P_	by 1 and shifted to the right			
16	Write	_data	to CG	RAM/	DDRA	М	-			1		writes 'H'			
	1	0	0	1	0	0	1	0	0	0	PH_				

Г

Table 42.	0-0	n ope	allon	,	e uisp	nay ai	using	external res	er (character ser A)continued			
Step	Instr	uction	1								Display	Operation
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
17 to 21						:				PHILIPS_	writes 'ILIPS'	
22	Retur	n_hor	ne								returns both display and cursor to the	
	0	0	0	0	0	0	0	0	1	0	<b>P</b> HILIPS	original position (address 0)

### Table 42. 8-bit operation, 1-line display and icon example; using external reset (character set 'A') ... continued

### 16.11 8-bit operation, 2-line display

For a 2-line display the cursor automatically moves from the first to the second line after the 40th digit of the first line has been written. Thus, if there are only 8 characters in the first line, the DDRAM address must be set after the 8th character is completed (see <u>Table 43</u>). It should be noted that both lines of the display are always shifted together; data does not shift from one line to the other.

Table 43. 8-bit operation, 2-line display example; using external reset (character set 'A')

	Instr	uction	ו													
Step	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation				
1	powe	er supp	oly on									initialized by the external reset; no display appears				
2	Func	tion_s	et									sets to 8-bit operation; selects 2-line				
	0	0	0	0	1	1	0	1	0	0		display and V <sub>LCD</sub> generator off				
3	displ	ay mo	de on/	off cor	ntrol							turns on display and cursor; entire				
	0 0 0 0 0 0 0 1 1 0									0	_	display is blank after initialization				
4	Entry_mode_set										sets mode to increment the address					
	0	0	0	0	0	0	0	1	1	0	-	by 1 and to shift the cursor to the right at the time of write to the CG/DDRAM; display is not shifted				
5	Write_data to CGRAM/DDRAM											writes 'P'; the DDRAM has already				
	1	0	0	1	0	1	0	0	0	0	P_	been selected by initialization at power-on; the cursor is incremented by 1 and shifted to the right				
6 to 10						:					PHILIP_	writes 'HILIP'				
11	Write	_data	to CG	RAM/	DDRA	М						writes 'S'				
	1	0	0	1	0	1	0	0	1	1	PHILIPS_					
12	Set_	DDRA	M									sets DDRAM address to position the				
	0	0	1	1	0	0	0	0	0	0	PHILIPS -	cursor at the head of the 2nd line				
13	Write	_data	to CG	o CGRAM/ DDRAM						1		writes 'M'				
	1	0	0	1	0	0	1	1	0	1	PHILIPS M_					
14 to 18						:					PHILIPS MICROC_	writes 'ICROC'				
19	Write	_data	to CG	RAM/	DDRA	М						writes 'O'				
	1	0	0	1	0	0	1	1	1	1	PHILIPS MICROCO					

	Instr	uction	1									
Step	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display	Operation
20	Write	_data	to CG	RAM/I	DDRA	М						sets mode for display shift at the time
	0	0	0	0	0	0	0	1	1	1	PHILIPS MICROCO_	of write
21	Write	_data	to CG	RAM/I	DDRA	Μ					writes 'M'; display is shifted to the left;	
	1	0	0	1	0	0	1	1	0	1	HILIPS ICROCOM_	the first and second lines shift together
22						:					:	
23	Retu	rn_hor	ne								returns both display and cursor to the	
	0	0	0	0	0	0	0	0	1	0	<mark>P</mark> HILIPS MICROCOM	original position (address 0)

### Table 43. 8-bit operation, 2-line display example; using external reset (character set 'A') ...continued

### 16.12 I<sup>2</sup>C-bus operation, 1-line display

A control byte is required with most commands (see Table 44).

### Table 44. Example of I<sup>2</sup>C-bus operation; 1-line display (using external reset, assuming pin SA0 = $V_{SS}$ )<sup>[1]</sup>

Step	l <sup>2</sup> C-b	us by	te							Display	Operation
1	l <sup>2</sup> C-b	us sta	rt								initialized; no display appears
2	slave	addre	ess for	write							during the acknowledge cycle SDA will be
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/W	Ack		pulled-down by the PCF2119x
	0	1	1	1	0	1	0	0	1	-	
3	send	a con	trol by	te for I	Functio	on_set	t				control byte sets RS for following data bytes
	СО	RS	0	0	0	0	0	0	Ack		
	0	0	0	0	0	0	0	0	1	-	
4	Func	tion_s	et								selects 1-line display and $V_{LCD} = V_0$ ; SCL
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack		pulse during acknowledge cycle starts
	0	0	1	Х	0	0	0	0	1	-	execution of instruction
5	Displa	ay_ctl								1	turns on display and cursor; entire display
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	_	shows character code 20h (blank in
	0	0	0	0	1	1	1	0	1	-	ASCII-like character sets)
6	Entry	_mode	e_set							1	sets mode to increment the address by 1
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	_	and to shift the cursor to the right at the time
	0	0	0	0	0	1	1	0	1	-	is not shifted
7	l <sup>2</sup> C-b	us sta	rt	1		1				-	for writing data to DDRAM, RS must be set to 1; therefore a control byte is needed
8	slave	addre	ess for	write							
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/W	Ack	_	
	0	1	1	1	0	1	0	0	1	-	
9	send	a con	trol by	te for \	Write_	data					
	со	RS	0	0	0	0	0	0	Ack	_	
	0	1	0	0	0	0	0	0	1	-	
L		1			1				1	1	

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Table 44.	Exa	mple	of I <sup>2</sup> C	-bus o	operat	tion; 1	-line o	displa	y (usi	ng external r	reset, assuming pin SA0 = V <sub>SS</sub> )[1]continued
Step	l <sup>2</sup> C-b	us by	te							Display	Operation
10	Write	_data	to DD	RAM							writes 'P'; the DDRAM has been selected at
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	P_	power-on; the cursor is incremented by 1 and shifted to the right
	0	1	0	1	0	0	0	0	1		and shinted to the right
11	Write	_data	to DD	RAM							writes 'H'
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PH_	
	0	1	0	0	1	0	0	0	1		
12 to 15					:					PHILIP_	writes 'ILIP'
16	Write	_data	to DD	RAM							writes 'S'
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PHILIPS_	
	0	1	0	1	0	0	1	1	1		
17	optio	nal l²C	-bus S	STOP						PHILIPS_	
18	l <sup>2</sup> C-b	us sta	rt							PHILIPS_	
19	slave	addre	ess for	write							
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/W	Ack	PHILIPS_	
	0	1	1	1	0	1	0	0	1		
20	contr	ol byte	•								
	СО	RS	0	0	0	0	0	0	Ack	PHILIPS_	
	1	0	0	0	0	0	0	0	1		
21	Retu	n_hor	ne								sets DDRAM address 0 in address counter
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PHILIPS	(also returns shifted display to original
	0	0	0	0	0	0	1	0	1		instruction does not update the data register
22	l <sup>2</sup> C-b	us sta	rt							<b>P</b> HILIPS	
23	slave	addre	ess for	read							during the acknowledge cycle the content of
	SA6	SA5	SA4	SA3	SA2	SA1	SA0	R/W	Ack	<b>P</b> HILIPS	the data register is loaded into the internal
	0	1	1	1	0	1	0	1	1	-	PC-bus interface to be shifted out; in the previous instruction neither a 'set address'
											nor a Read_data has been performed;
											therefore the content of the data register
											1 while still in $I^2C$ -write mode
24	contr	ol byte	for re	ad							DDRAM content will be read from following
	со	RS	0	0	0	0	0	0	Ack	PHILIPS	instructions
	0	1	1	0	0	0	0	0	1		
25	Read	data	: 8 × S	CL + r	nastei	r ackn	owledo	qe <mark>[2]</mark>			$8 \times SCL$ ; content loaded into interface
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PHILIPS	during previous acknowledge cycle is
	х	х	х	х	х	Х	х	Х	0		shifted out over SDA; MSB is DB7; during
											address 01 is loaded into the I <sup>2</sup> C-bus
											interface
26	Read	_data:	8 × S	CL + r	naste	r ackn	owledg	ge <mark>[2]</mark>			$8 \times SCL$ ; code of letter 'H' is read first;
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Ack	PHILIPS	during master acknowledge code of 'l' is
	0	1	0	0	1	0	0	0	0		

PCF2119X Product data sheet

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#### Table 44. Example of I<sup>2</sup>C-bus operation; 1-line display (using external reset, assuming pin SA0 = V<sub>SS</sub>)<sup>[1]</sup> ...continued I<sup>2</sup>C-bus byte Operation Step Display 27 Read\_data: 8 × SCL + no master acknowledge<sup>[2]</sup> no master acknowledge; after the content of the I<sup>2</sup>C-bus interface register is shifted out DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 Ack **PHILIPS** no internal action is performed; no new data 0 0 0 1 1 0 0 1 1 is loaded to the interface register, data register is not updated, address counter is not incremented and cursor is not shifted I<sup>2</sup>C-bus STOP PHILIPS 28

[1] X = don't care.

[2] SDA is left at high-impedance by the microcontroller during the read acknowledge.

### 16.13 Initialization

### Table 45. Initialization by instruction, 8-bit interface ([1])

Step	Instr										Description		
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
1	powe	r-on o	r unkn	iown s	tate								
2	wait 2	2 ms									after internal reset has been applied		
3	Func	tion_s	et								interface is 8 bits long; BF cannot be checked before		
	0	0	0	0	1	1	Х	Х	Х	Х	this instruction		
4	wait 2	2 ms											
5	Func	tion_s	et								interface is 8 bits long; BF cannot be checked before		
	0 0 0 0 1 1 X X X									Х	this instruction		
6	wait r	nore t	han 40	)μs									
7	Func	tion_s	et								interface is 8 bits long; BF cannot be checked before		
	0	0	0	0	1	1	Х	Х	Х	Х	this instruction		
BF can b specified	e cheo instru	cked a ction t	fter th ime (s	e follov ee <mark>Tab</mark>	wing ir ole 12)	struct	ions; \	when I	BF is r	not che	ecked, the waiting time between instructions is the		
8	Func	tion_s	et (inte	erface	is 8 bi	ts long	g)				specify number of display lines		
	0	0	0	0	1	1	0	М	0	Н			
9	Displa	ay_ctl		1					1		display off		
	0	0	0	0	0	0	1	0	0	0			
10	Clear	_displ	ay	1					1				
	0 0 0 0 0 0 0 0 0									1			
11	Entry	_mode	e_set	1					1				
	0	0	0	0	0	0	0	1	I_D	S			
12	initial	ization	ends										

[1] X = don't care.

Step	Instr	uction	I				Description
	RS	R/W	DB7	DB6	DB5	DB4	-
1	powe	er-on o	r unkn	own s	tate		
2	wait 2	2 ms a	fter int	ernal	reset ł	nas be	en applied
3	Func	tion_se	ət				interface is 8 bits long; BF cannot be checked
	0	0	0	0	1	1	before this instruction
4	wait 2	2 ms					
5	Func	tion_se	et				interface is 8 bits long; BF cannot be checked
	0	0	0	0	1	1	before this instruction
6	wait r	more tl	nan 40	) μ <b>s</b>			
7	Func	tion_se	ət				interface is 8 bits long; BF cannot be checked
	0	0	0	0	1	1	before this instruction
BF can between	be cheo instruc	cked a ctions	fter the	e follov specifi	wing ir ed ins	nstruct tructio	ions; when BF is not checked, the waiting time in time (see <u>Table 12</u> )
8	Func	tion_se	ət				
	0	0	0	0	1	0	set interface to 4 bit long interface is 8 bit long
9	Func	tion_se	ət				
	0	0	0	0	1	0	set interface to 4 bits long
	0	0	0	М	0	Н	specify number of display line
10	Displ	ay_ctl					
	0	0	0	0	0	0	
	0	0	1	0	0	0	display off
11	Clear	_displ	ay				
	0	0	0	0	0	0	
	0	0	0	0	0	1	
12	Entry_mode_set						
	0	0	0	0	0	0	
	0	0	0	1	I_D	S	
				:			
13	Initial	ization	ends				

 Table 46.
 Initialization by instruction, 4-bit interface; not applicable for I<sup>2</sup>C-bus operation

### 16.14 User defined characters and symbols

Up to 16 user defined characters may be stored in the CGRAM. The content of the CGRAM is lost during power-down, therefore the CGRAM has to be rewritten after every power-on.



Below some source code is printed, which shows how a user defined character is defined - in this case the euro currency sign. The display used is a 2 lines by 16 characters display and the interface is the  $l^2C$ -bus:

```
// Write a user defined character into the CGRAM
startI2C();
// PCF2119 slave address for write, SAO is connected to Vdd
SendI2CAddress(0x76);
// MSB (Continuation bit Co) = 0, more than one byte may follow. Bit6, RS=0, next byte
// is command byte
i2c_write(0x00);
// 2 lines x 16, 1/18 duty, basic instruction set. Next byte will be another command.
i2c_write(0x24);
// Set CGRAM address to 0
i2c write(0x40);
// Repeated Start condition
startI2C();
SendI2CAddress(0x76);
// RS=1, next byte is a data byte
i2c_write(0x40);
// Here the data bytes to define the character
// Behind the write commands the 5x8 dot matrix is shown, the 1 represents a on pixel.
// The Euro currency character can be recognized by the 0/1 pattern (see Figure 48)
i2c_write(0x06); // 00110
i2c_write(0x09); // 01001
i2c_write(0x08); // 01000
i2c_write(0x1E); // 11110
i2c_write(0x1E); // 11110
i2c_write(0x08); // 01000
i2c write(0x09); // 01001
i2c_write(0x06); // 00110
i2c stop();
// Until here the definition of the character and writing it into the CGRAM. Now it
// still needs to be displayed. See below.
```

```
PCF2119x
```

```
// PCF2119, setting of proper display modes
startI2C();
// PCF2119 slave address for write, SAO is connected to Vdd
SendI2CAddress(0x76);
// MSB (Continuation bit Co) = 0, more than one byte may follow. Bit6, RS=0, next byte
// is command byte
i2c_write(0x00);
// 2 lines x 16, 1/18 duty, extended instruction set. Next byte will be another
// command.
i2c_write(0x25);
// Set display configuration to right to left, column 80 to 1. Row data displ. top to
// bottom,1 to 16.
i2c_write(0x06);
// Set to character mode, full display, icon blink disabled
i2c_write(0x08);
// Set voltage multiplier to 2
i2c write(0x40);
// Set Vlcd and store in register VA
i2c write(0xA0);
// Change from extended instruction set to basic instruction set
i2c_write(0x24);
// Display control: set display on, cursor off, no blink
i2c_write(0x0C);
// Entry mode set, increase DDRAM after access, no shift
i2c write(0x06);
// Return home, set DDRAM address 0 in address counter
i2c_write(0x02);
// Clear entire display, set DDRAM address to 0 in address counter
i2c_write(0x01);
// Repeated Start condition because RS needs to be changed from 0 to 1
startI2C();
SendI2CAddress(0x76);
// RS=1, next byte is data
i2c_write(0x40);
// Write the character at address 0, which is the previously defined Euro currency
// character
i2c_write(0x00);
i2c_stop();
```

### 17. Bare die outline



Fig 49. Bare die outline of PCF2119x

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### Table 47. Dimensions of PCF2119x

Original dimensions are in mm.

Unit (mm)	Α	<b>A</b> <sub>1</sub>	b	b <sub>1</sub>	D	E	е	e <sub>1</sub>	L
max		0.0225							
nom	0.38 <mark>[1]</mark>	0.0175	0.05	0.1	7.6	1.7	0.07	0.35	0.09
min		0.0125							

[1] PCF2119RU/2DB/2 has a PI scratch protection coating, adding 3.6  $\mu$ m to to the die thickness.

#### Table 48. Pin location

All X and Y coordinates are referenced to the center of the chip (dimensions in  $\mu$ m).

Symbol	Pin	Х	Y	Description
V <sub>DD1</sub>	1	+745	-274	logic supply voltage 1
V <sub>DD1</sub>	2	+745	-204	
V <sub>DD1</sub>	3	+745	-134	
V <sub>DD1</sub>	4	+745	-64	
V <sub>DD1</sub>	5	+745	+6	
V <sub>DD1</sub>	6	+745	+76	
V <sub>DD2</sub>	7	+745	+146	V <sub>LCD</sub> generator supply voltage 2
V <sub>DD2</sub>	8	+745	+216	
V <sub>DD2</sub>	9	+745	+286	
V <sub>DD2</sub>	10	+745	+356	
V <sub>DD2</sub>	11	+745	+426	
V <sub>DD2</sub>	12	+745	+496	
V <sub>DD2</sub>	13	+745	+566	
V <sub>DD2</sub>	14	+745	+636	
V <sub>DD3</sub>	15	+745	+706	
V <sub>DD3</sub>	16	+745	+776	
V <sub>DD3</sub>	17	+745	+846	
V <sub>DD3</sub>	18	+745	+916	
E	19	+745	+986	data bus clock input
T1	20	+745	+1196	test pin 1
T2	21	+745	+1406	test pin 2
V <sub>SS1</sub>	22	+745	+1616	ground 1
V <sub>SS1</sub>	23	+745	+1686	
V <sub>SS1</sub>	24	+745	+1756	
V <sub>SS1</sub>	25	+745	+1826	
V <sub>SS1</sub>	26	+745	+1896	
V <sub>SS1</sub>	27	+745	+1966	
V <sub>SS1</sub>	28	+745	+2036	
V <sub>SS1</sub>	29	+745	+2106	

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Symbol	Pin	Х	Υ	Description
V <sub>SS2</sub>	30	+745	+2176	ground 2
V <sub>SS2</sub>	31	+745	+2246	
V <sub>SS2</sub>	32	+745	+2316	
V <sub>SS2</sub>	33	+745	+2386	
V <sub>SS2</sub>	34	+745	+2456	
V <sub>SS2</sub>	35	+745	+2666	
V <sub>LCDSENSE</sub>	36	+745	+2736	input for voltage multiplier regulation
V <sub>LCDOUT</sub>	37	+745	+2806	V <sub>LCD</sub> output
V <sub>LCDOUT</sub>	38	+745	+2876	
V <sub>LCDOUT</sub>	39	+745	+2946	
V <sub>LCDOUT</sub>	40	+745	+3016	
V <sub>LCDOUT</sub>	41	+745	+3086	V <sub>LCD</sub> output
V <sub>LCDOUT</sub>	42	+745	+3156	
V <sub>LCDOUT</sub>	43	+745	+3226	
V <sub>LCDIN</sub>	44	+745	+3296	input for generation of LCD bias levels
V <sub>LCDIN</sub>	45	+745	+3366	
V <sub>LCDIN</sub>	46	+745	+3436	
V <sub>LCDIN</sub>	47	+745	+3506	
V <sub>LCDIN</sub>	48	+745	+3576	
V <sub>LCDIN</sub>	49	+745	+3646	
dummy	50	-745	+3576	dummy
R8	51	-745	+3506	LCD row driver output
R7	52	-745	+3436	
R6	53	-745	+3366	
R5	54	-745	+3296	
R4	55	-745	+3226	
R3	56	-745	+3156	
R2	57	-745	+3086	
R1	58	-745	+3016	
R17	59	-745	+2946	
C80	60	-745	+2876	LCD column driver output
C79	61	-745	+2806	
C78	62	-745	+2736	
C77	63	-745	+2666	
C76	64	-745	+2596	
C75	65	-745	+2526	
C74	66	-745	+2456	
C73	67	-745	+2386	
C72	68	-745	+2316	
C71	69	_745	+2246	

 Table 48.
 Pin location ...continued
Symbol	Pin	Х	Y	Description
C70	70	-745	+2176	LCD column driver output
C69	71	-745	+2106	
C68	72	-745	+2036	
C67	73	-745	+1966	
C66	74	-745	+1896	
C65	75	-745	+1756	
C64	76	-745	+1686	
C63	77	-745	+1616	
C62	78	-745	+1546	
C61	79	-745	+1476	
C60	80	-745	+1406	
C59	81	-745	+1336	
C58	82	-745	+1266	
C57	83	-745	+1196	
C56	84	-745	+1126	
C55	85	-745	+1056	
C54	86	-745	+986	
C53	87	-745	+916	
C52	88	-745	+846	
C51	89	-745	+776	
C50	90	-745	+706	
C49	91	-745	+636	
C48	92	-745	+566	
C47	93	-745	+496	
C46	94	-745	+426	
C45	95	-745	+356	
C44	96	-745	+286	
C43	97	-745	+216	
C42	98	-745	+146	
C41	99	-745	+76	
R17DUP	100	-745	+6	LCD row driver output
C40	101	-745	-64	LCD column driver output
C39	102	-745	-134	
C38	103	-745	-204	
C37	104	-745	-274	
C36	105	-745	-344	
C35	106	-745	-414	
C34	107	-745	-484	
C33	108	-745	-554	
C32	109	-745	-624	

 Table 48.
 Pin location ...continued

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Symbol	Pin	X	Y	Description
C31	110	-745	-694	LCD column driver output
C30	111	-745	-764	
C29	112	-745	-834	
C28	113	-745	-904	
C27	114	-745	-974	
C26	115	-745	-1044	
C25	116	-745	-1114	
C24	117	-745	-1184	
C23	118	-745	-1254	
C22	119	-745	-1324	
C21	120	-745	-1394	
C20	121	-745	-1464	
C19	122	-745	-1534	
C18	123	-745	-1604	
C17	124	-745	-1674	
C16	125	-745	-1744	
C15	126	-745	-1884	
C14	127	-745	-1954	
C13	128	-745	-2024	
C12	129	-745	-2094	
C11	130	-745	-2164	
C10	131	-745	-2234	
C9	132	-745	-2304	
C8	133	-745	-2374	
C7	134	-745	-2444	
C6	135	-745	-2514	
C5	136	-745	-2584	
C4	137	-745	-2654	
C3	138	-745	-2724	
C2	139	-745	-2794	
C1	140	-745	-2864	
R18	141	-745	-2934	LCD row driver output
R9	142	-745	-3004	
R10	143	-745	-3074	
R11	144	-745	-3144	
R12	145	-745	-3214	
R13	146	-745	-3284	
R14	147	-745	-3354	
R15	148	-745	-3424	
R16	149	-745	-3494	

 Table 48.
 Pin location ...continued

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Symbol	Pin	Х	Y	Description
dummy	150	-745	-3704	dummy
SCL	151	+745	-3704	I <sup>2</sup> C-bus serial clock input
SCL	152	+745	-3634	
Т3	153	+745	-3494	test pin 3
POR	154	+745	-3424	external Power-On Reset (POR) input
PD	155	+745	-3214	power-down mode select input
SDA	156	+745	-3004	I <sup>2</sup> C-bus serial data input/output
SDA	157	+745	-2934	
R/W	158	+745	-2584	read/write input
RS	159	+745	-2374	register select input
DB0	160	+745	-2164	8-bit bidirectional data bus; bit 0
DB1	161	+745	-1954	8-bit bidirectional data bus; bit 1
DB2	162	+745	-1744	8-bit bidirectional data bus; bit 2
DB3/SA0	163	+745	-1534	8-bit bidirectional data bus; bit 3
DB4	164	+745	-1324	8-bit bidirectional data bus; bit 4
DB5	165	+745	-1114	8-bit bidirectional data bus; bit 5
DB6	166	+745	-904	8-bit bidirectional data bus; bit 6
DB7	167	+745	-694	8-bit bidirectional data bus; bit 7
OSC	168	+745	-484	oscillator or external clock input

#### Table 48. Pin location ...continued

#### Table 49. Alignment mark location

All X and Y coordinates are referenced to the center of the chip (dimensions in  $\mu m$ ).

Symbol	Pin	X	Y
AM1	-	+745	-2689
AM2	-	+745	+2561
AM3	-	-745	+3681
AM4	-	-745	-3599

## **18. Handling information**

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in JESD625-A, IEC 61340-5 or equivalent standards.

## **19. Packing information**



## **19.1** Packing information on the tray

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#### Table 50. Specification of 3 inch tray details

Tray details are shown in Figure 50. Nominal values without production tolerances.

Tray details													
Dimensions													
В	С	D	E	F	G	Н	J	K	L	М	Ν	0	Unit
3.0	7.69	1.81	76.0	68.0	57.0	6.5	9.5	63	4.2	2.6	3.2	0.50	mm
r of poo	kets												
x direction						y direction							
7						22							
	tails ions B 3.0 r of poo	tails ions B C 3.0 7.69 r of pockets on	C         D           3.0         7.69         1.81           of pockets         D	C         D         E           3.0         7.69         1.81         76.0           of pockets         on         Feature         Feature         Feature	tails           ions           B         C         D         E         F           3.0         7.69         1.81         76.0         68.0           of pockets	tails           ions           B         C         D         E         F         G           3.0         7.69         1.81         76.0         68.0         57.0           of pockets	tails           ions           B         C         D         E         F         G         H           3.0         7.69         1.81         76.0         68.0         57.0         6.5           of pockets         y direct           con	tails           ions           B         C         D         E         F         G         H         J           3.0         7.69         1.81         76.0         68.0         57.0         6.5         9.5           of pockets         y direction           Dn         y direction	tails           ions           B         C         D         E         F         G         H         J         K           3.0         7.69         1.81         76.0         68.0         57.0         6.5         9.5         63           of pockets           y direction           22	tails           ions           B         C         D         E         F         G         H         J         K         L           3.0         7.69         1.81         76.0         68.0         57.0         6.5         9.5         63         4.2           of pockets           y direction           Z2	tails         ions         B       C       D       E       F       G       H       J       K       L       M         3.0       7.69       1.81       76.0       68.0       57.0       6.5       9.5       63       4.2       2.6         of pockets         y direction         22	tails           ions           B         C         D         E         F         G         H         J         K         L         M         N           3.0         7.69         1.81         76.0         68.0         57.0         6.5         9.5         63         4.2         2.6         3.2           of pockets           y direction           22	tails         ions         B       C       D       E       F       G       H       J       K       L       M       N       O         3.0       7.69       1.81       76.0       68.0       57.0       6.5       9.5       63       4.2       2.6       3.2       0.50         of pockets         y direction         22



**PCF2119x** 

# 20. Appendix

## 20.1 LCD character driver selection

#### Table 51. Selection of LCD character drivers

	Type name	Numbe	er of			Character	V <sub>DD1</sub> (V)	V <sub>DD2</sub> (V)	V <sub>LCD</sub> (V)	f <sub>fr</sub> (Hz)	V <sub>LCD</sub> (V)	V <sub>LCD</sub> (V)	T <sub>amb</sub> (°C)	Interface	AEC-
		Lines	× Chara	cters	lcons	set					charge pump	temp. comp			Q100
	PCF2113AU	1 × 24	2 × 12	-	120	A	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
	PCF2113DU	1 × 24	2 × 12	-	120	D	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
All inform	PCF2113EU	1 × 24	2 × 12	-	120	E	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
ation provid	PCF2113WU	1 × 24	2 × 12	-	120	W	1.8 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
ed in this do	PCF2116AU	1 × 24	2 × 24	4 × 12	-	A	2.5 to 6	2.5 to 6	3.5 to 9	65	Y	N	-40 to 85	l <sup>2</sup> C / Parallel	N
cument is s	PCF2116CU	1 × 24	2 × 24	4 × 12	-	С	2.5 to 6	2.5 to 6	3.5 to 9	65	Y	Ν	-40 to 85	l <sup>2</sup> C / Parallel	N
ubject to leg	PCF2119AU	1 × 32	2 × 16	-	160	A	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
al disclaime	PCF2119DU	1 × 32	2 × 16	-	160	D	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
ers.	PCF2119FU	1 × 32	2 × 16	-	160	F	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
	PCF2119IU	1 × 32	2 × 16	-	160	I	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
© NXP Se	PCF2119RU	1 × 32	2 × 16	-	160	R	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
miconducto	PCF2119SU	1 × 32	2 × 16	-	160	S	1.5 to 5.5	2.2 to 4	2.2 to 6.5	95	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
rs N.V. 201	PCF21219DUGR	1 × 32	2 × 16	-	160	R	1.5 to 5.5	2.2 to 4	2.2 to 6.5	220	Y	Y	-40 to 85	l <sup>2</sup> C / Parallel	N
5. All rig	PCA2117DUGR	$1 \times 40$	2  imes 20	-	200	R	2.5 to 5.5	2.5 to 5.5	4 to 16	45 to 360[1]	Y	Y	-40 to 105	I <sup>2</sup> C / SPI	Y
jhts res	PCA2117DUGS	$1 \times 40$	2  imes 20	-	200	S	2.5 to 5.5	2.5 to 5.5	4 to 16	45 to 360[1]	Y	Y	-40 to 105	I <sup>2</sup> C / SPI	Y

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[1] Software programmable.

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# 21. Abbreviations

Table 52. Abbre	eviations
Acronym	Description
CGRAM	Character Generator RAM
CGROM	Character Generator ROM
CMOS	Complementary Metal-Oxide Semiconductor
COG	Chip-On-Glass
DC	Direct Current
DDRAM	Display Data RAM
НВМ	Human Body Model
l <sup>2</sup> C	Inter-Integrated Circuit
IC	Integrated Circuit
ΙΤΟ	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
MUX	Multiplexer
PCB	Printed-Circuit Board
PI	Polyimide
POR	Power-On Reset
RAM	Random Access Memory
RMS	Root Mean Square
ROM	Read Only Memory
SCL	Serial CLock line
SDA	Serial DAta line

### 22. References

- [1] AN10170 Design guidelines for COG modules with NXP monochrome LCD drivers
- [2] AN10706 Handling bare die
- [3] AN10853 ESD and EMC sensitivity of IC
- [4] AN11267 EMC and system level ESD design guidelines for LCD drivers
- [5] IEC 60134 Rating systems for electronic tubes and valves and analogous semiconductor devices
- [6] IEC 61340-5 Protection of electronic devices from electrostatic phenomena
- [7] JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [8] JESD22-A115 Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)
- [9] JESD78 IC Latch-Up Test
- [10] JESD625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [11] UM10204 I<sup>2</sup>C-bus specification and user manual
- [12] UM10569 Store and transport requirements

# 23. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
PCF2119X v.12	20150416	Product data sheet	-	PCF2119X v.11				
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.							
	<ul> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>							
	<ul> <li>Adjusted desc</li> </ul>	ription in <u>Section 16.1</u>						
	<ul> <li>Corrected des</li> </ul>	cription of the dummy pins in Ta	able 4 and Table 48					
PCF2119X v.11	20130715	Product data sheet	-	PCF2119X v.10				
PCF2119X v.10	20111031	Product data sheet	-	PCF2119X v.9				
PCF2119X v.9	20110414	Product data sheet	-	PCF2119X v.8				
PCF2119X v.8	20110404	Product data sheet	-	PCF2119X v.7				
PCF2119X v.7	20101115	Product data sheet	-	PCF2119X v.6				
PCF2119X v.6	20100908	Product data sheet	-	PCF2119X_5				
PCF2119X_5	20090813	Product data sheet	-	PCF2119X_4				
PCF2119X_4	20030130	Product specification	-	PCF2119X_3				
PCF2119X_3	20020116	Product specification	-	PCF2119X_2				
PCF2119X_2	19990302	Product specification	-	PCF2119X_1				
PCF2119X_1	19971121	Objective specification	-	-				

#### Table 53. Revision history

## 24. Legal information

#### 24.1 Data sheet status

Document status[1][2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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