PCAL9714

Ultra low-voltage translating 14-bit SPI I/O expander with Agile I/O features, interrupt output, and reset

Rev. 1.0 — 1 May 2023 Product data sheet

1 General description

The PCAL9714 is a 14-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Serial Peripheral Interface (SPI). The ultra low-voltage interface allows for direct connection with the microcontroller operating down to 1.1 V.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level down to 1.1 V to I/O devices operating at a different voltage level 1.65 V to 5.5 V. The PCAL9714 has built-in level shifting feature that makes these devices extremely flexible in mixed power supply systems where communication between incompatible I/O voltages is required, allowing seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL9714: $V_{DD(SPI)}$ and $V_{DD(P)}$. $V_{DD(SPI)}$ provides the supply voltage for the interface at the master side (for example, a microcontroller) and the $V_{DD(P)}$ provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCAL9714 is provided through $V_{DD(SPI)}$. $V_{DD(SPI)}$ should be connected to the V_{DD} of the external SPI interface lines. This indicates the V_{DD} level of the SPI to the PCAL9714, while the voltage level on Port P of the PCAL9714 is determined by the $V_{DD(P)}$.

The PCAL9714 works with the SPI speed at 5 MHz and implements Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pullup/pulldown resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

Additional Agile I/O Plus features include interrupts specified by level or edge, and they can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pullup and pulldown resistors eliminate the need for discrete components.

The system master can reset the PCAL9714 in the event of a time-out or other improper operation by asserting a LOW in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the SPI state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the part.

The PCAL9714 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

($\overline{\text{INT}}$) can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the SPI. Thus, the PCAL9714 can remain a simple slave device. The input latch feature holds or latches the input pin state and keeps the logic values that created the interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed SPI-bus address and allow up to four devices to share the same SPI bus.

2 Features and benefits

- SPI bus to parallel port expander
- 5 MHz SPI bus
- Operating power supply voltage range of 1.1 V to 5.5 V on the SPI bus side
- Allows bidirectional voltage-level translation and GPIO expansion between 1.1 V to 5.5 V on SPI and 1.8 V, 2.5 V, 3.3 V or 5.5 V Port P
- Low standby current consumption: 2.0 µA typical at 3.3 V V_{DD}
- 5.5 V tolerant I/O ports and SPI bus pins
- Active LOW reset input ($\overline{\text{RESET}}$)
- Open-drain active LOW interrupt output ($\overline{\text{INT}}$)
- Internal power-on reset
- Power-up with all channels configured as inputs
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Package offered: HVQFN24

2.1 Agile I/O features

- Output port configuration: bank selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - Input latch: Input Port register values changes are kept until the Input Port register is read
  - Pullup/pulldown enable: floating input or pullup/pulldown resistor enable
  - Pullup/pulldown selection: 100 kΩ pullup/pulldown resistor selection
  - Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

2.2 Additional Agile I/O Plus features

- Interrupt edge specification on a bit-by-bit basis
- Interrupt individual clear without disturbing other events
- Read all interrupt events without clear
- Switch debounce hardware

3 Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCAL9714HN	9714	HVQFN24	plastic, thermal enhanced very thin quad flat package; 0.125 dimple wettable flank; 24 terminals; 0.5 mm pitch; 4 mm x 4 mm x 0.85 mm body	SOT616-3
PCAL9714HN/Q900 [1]	Q714	HVQFN24	plastic, thermal enhanced very thin quad flat package; 0.125 dimple wettable flank; 24 terminals; 0.5 mm pitch; 4 mm x 4 mm x 0.85 mm body	SOT616-3

[1] Automotive AEC-Q100 (Grade 1) compliant. Contact NXP support for PPAP.

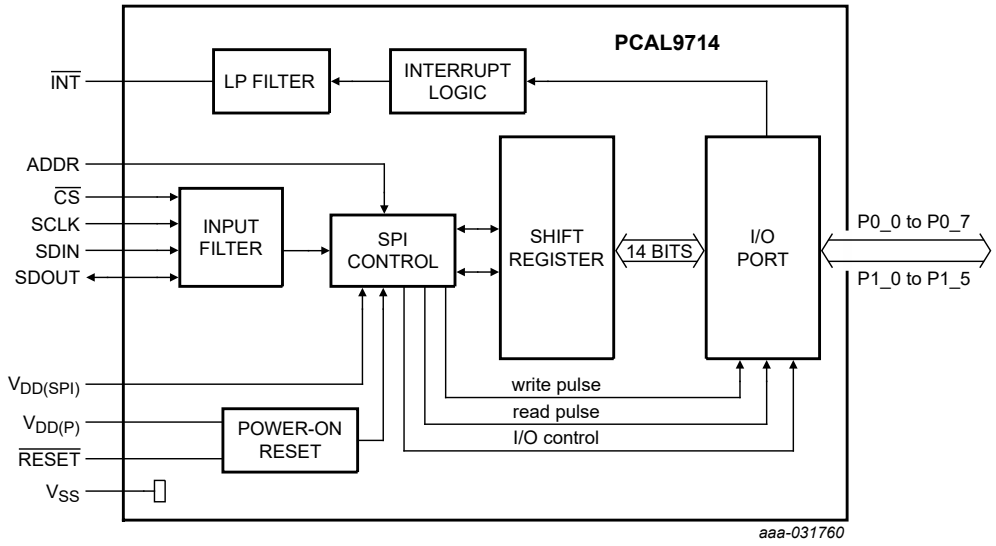
3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCAL9714HN	PCAL9714HNMP	HVQFN24	Reel 13” Q2/T3 SMD DP	6000	T_{amb} = -40 °C to +85 °C
PCAL9714HN/Q900 [1]	PCAL9714HN/Q900MP	HVQFN24	Reel 13” Q2/T3 SMD DP	6000	T_{amb} = -40 °C to +125 °C

[1] Automotive AEC-Q100 (Grade 1) compliant. Contact NXP support for PPAP.

4 Block diagram

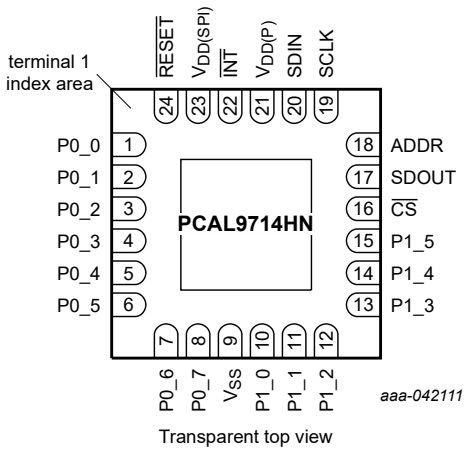


1. All I/Os are set to inputs at reset.

Figure 1. Block diagram of PCAL9714 (positive logic)

5 Pinning information

5.1 Pinning



Transparent top view

1. The exposed center pad, if used, must be connected only as a secondary ground or must be left electrically open.

Figure 2. Pin configuration for HVQFN24

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$\overline{INT}$	22	Interrupt output. Connect to $V_{DD(SPI)}$ or $V_{DD(P)}$ through a pullup resistor.
$V_{DD(SPI)}$	23	Supply voltage of SPI bus. Connect directly to the V_{DD} of the external SPI master. Provides voltage-level translation.
$\overline{RESET}$	24	Active LOW reset input. Connect to $V_{DD(SPI)}$ if no external logic signal is driving the pin.
P0_0[1]	1	Port 0 input/output 0.
P0_1[1]	2	Port 0 input/output 1.
P0_2[1]	3	Port 0 input/output 2.
P0_3[1]	4	Port 0 input/output 3.
P0_4[1]	5	Port 0 input/output 4.
P0_5[1]	6	Port 0 input/output 5.
P0_6[1]	7	Port 0 input/output 6.
P0_7[1]	8	Port 0 input/output 7.
V_{SS}	9	Ground.
P1_0[2]	10	Port 1 input/output 0.
P1_1[2]	11	Port 1 input/output 1.
P1_2[2]	12	Port 1 input/output 2.
P1_3[2]	13	Port 1 input/output 3.
P1_4[2]	14	Port 1 input/output 4.

Table 3. Pin description...*continued*

Symbol	Pin	Description
P1_5[2]	15	Port 1 input/output 5.
$\overline{CS}$	16	SPI chip select.
SDOUT	17	SPI serial data output.
ADDR	18	Address input. Connect directly to $V_{DD(P)}$ or ground.
SCLK	19	SPI clock.
SDIN	20	SPI serial data input.
$V_{DD(P)}$	21	Supply voltage of PCAL9714 for Port P.

[1] Pins P0_0 to P0_7 correspond to bits P0.0 to P0.7. At power-on, all I/O are configured as input.
[2] Pins P1_0 to P1_5 correspond to bits P1.0 to P1.5. At power-on, all I/O are configured as input.

6 Functional description

6.1 Device address

The bus master must send the target slave address followed by a read or write operation. The slave address of the PCAL9714 is shown in Figure 3. Slave address pin ADDR choose one of two slave addresses. To conserve power, no internal pullup resistors are incorporated on ADDR. Table 4 shows both slave addresses by connecting ADDR to V_{DD} or V_{SS}.

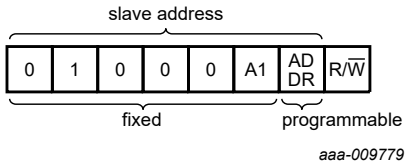


Figure 3. PCAL9714 device address

The last bit of the first byte defines the reading from or writing to the PCAL9714. When set to logic 1 a read is selected, while logic 0 selects a write operation. See Section 6.10.1.1 for a description of the SPI protocol.

Table 4. PCAL9714 address map

ADDR	Device family high-order address bits						Variable portion of address	Address
	A6	A5	A4	A3	A2	A1	A0	
V_{SS}	0	1	0	0	0	0	0	40h
V_{DD}	0	1	0	0	0	0	1	42h

6.2 Interface definition

Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
SPI bus slave address	L	H	L	L	L	L	ADDR	R/$\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	-	-	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

6.3 Pointer register and command byte

Following the first byte of the slave address, the bus master sends a command byte, which is write only and stored in the pointer register in the PCAL9714. The lowest 7 bits (B[6:0] in Table 6) are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in Figure 4. At power-up or hardware reset, the pointer register defaults to 00h, with the AI bit set to ‘0’ and the lowest seven bits set to ‘000 0000’.

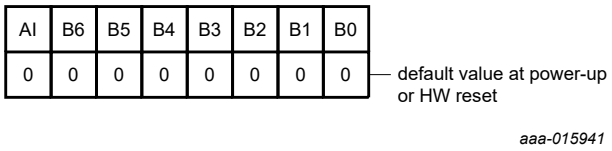
When the Auto-Increment bit is set (AI = 1), the seven low-order bits of the pointer

register are automatically incremented after a read or write until the chip select ($\overline{CS}$) is deasserted. This allows the user to program the registers sequentially without modifying the pointer register. The contents of these bits will roll over to ‘000 0000’ after the last register (address = 5Ch) is accessed. Unimplemented register

addresses (reserved registers) are skipped. If more than 36 bytes are written, the address will loop back to the register which is indicated by the seven low-order bits in the pointer register, and

previously-written data will be overwritten. The deassertion of chip select (CS) condition will keep the pointer register value in the last read or write location.

When the Auto-Increment bit is cleared (AI = 0), the 2 least significant bits are automatically incremented after a read or write for 3-register group which allows the user to program each of the 3-register group sequentially. If more than 3 bytes of data are read or written when AI is 0, previous data in the selected registers will be overwritten. For example: if input port 1 is read first, the next 2nd byte will be input port 2, and next 3nd byte will be input port 0, there is no limit on the number of data bytes for this read operation. There are two special 6-register groups: output drive strength (40h~43h) and interrupt edge (50h~53h) registers will allow user to program each of the 6-register group sequentially. Only Output port configuration register location (4Fh) remains in the same location after a successive read or write.



AI = Auto-Increment

Figure 4. Pointer register bits

Table 6. Command byte

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx[1]
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx[1]
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111
0	1	0	0	0	0	0	0	40h	Output drive strength register 0A	read/write byte	1111 1111
0	1	0	0	0	0	0	1	41h	Output drive strength register 0B	read/write byte	1111 1111
0	1	0	0	0	0	1	0	42h	Output drive strength register 1A	read/write byte	1111 1111
0	1	0	0	0	0	1	1	43h	Output drive strength register 1B	read/write byte	1111 1111
0	1	0	0	0	1	0	0	44h	Input latch register 0	read/write byte	0000 0000
0	1	0	0	0	1	0	1	45h	Input latch register 1	read/write byte	0000 0000
0	1	0	0	0	1	1	0	46h	Pullup/pulldown enable register 0	read/write byte	0000 0000

Table 6. Command byte...*continued*

Pointer register bits								Command byte (hexadecimal)	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	1	0	0	0	1	1	1	47h	Pullup/pulldown enable register 1	read/write byte	0000 0000
0	1	0	0	1	0	0	0	48h	Pullup/pulldown selection register 0	read/write byte	1111 1111
0	1	0	0	1	0	0	1	49h	Pullup/pulldown selection register 1	read/write byte	1111 1111
0	1	0	0	1	0	1	0	4Ah	Interrupt mask register 0	read/write byte	1111 1111
0	1	0	0	1	0	1	1	4Bh	Interrupt mask register 1	read/write byte	1111 1111
0	1	0	0	1	1	0	0	4Ch	Interrupt status register 0	read byte	0000 0000
0	1	0	0	1	1	0	1	4Dh	Interrupt status register 1	read byte	0000 0000
0	1	0	0	1	1	1	1	4Fh [2]	Output port configuration register	read/write byte	0000 0000
0	1	0	1	0	0	0	0	50h	Interrupt edge register 0A	read/write byte	0000 0000
0	1	0	1	0	0	0	1	51h	Interrupt edge register 0B	read/write byte	0000 0000
0	1	0	1	0	0	1	0	52h	Interrupt edge register 1A	read/write byte	0000 0000
0	1	0	1	0	0	1	1	53h	Interrupt edge register 1B	read/write byte	0000 0000
0	1	0	1	0	1	0	0	54h	Interrupt clear register 0	write byte	0000 0000
0	1	0	1	0	1	0	1	55h	Interrupt clear register 1	write byte	0000 0000
0	1	0	1	0	1	1	0	56h	Input port read without interrupt clear 0	read byte	xxxx xxxx[1]
0	1	0	1	0	1	1	1	57h	Input port read without interrupt clear 1	read byte	xxxx xxxx[1]
0	1	0	1	1	0	0	0	58h	Output configuration register 0 (bit-wise)	read/write byte	0000 0000
0	1	0	1	1	0	0	1	59h	Output configuration register 1 (bit-wise)	read/write byte	0000 0000
0	1	0	1	1	0	1	0	5Ah[2]	Switch debounce enable 0	read/write byte	0000 0000
0	1	0	1	1	0	1	1	5Bh[2]	Switch debounce enable 01	read/write byte	0000 0000
0	1	0	1	1	1	0	0	5Ch	Switch debounce count	read/write byte	0000 0000

[1] Undefined
[2] Successive

6.4 Register descriptions

6.4.1 Input port registers (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value ‘X’ is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 6.10.1.2.

Table 7. Input port 0 register (address 00h)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

Table 8. port 1 register (address 01h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	-	-	X	X	X	X	X	X

6.4.2 Output port registers (02h, 03h)

The Output port registers (registers 2 and 3) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2 .

Table 9. Output port 0 register (address 02h)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 10. Output port 1 register (address 03h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	-	-	1	1	1	1	1	1

6.4.3 Polarity inversion register pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with ‘1’), the corresponding port pin’s polarity is inverted in the input register. If a bit in this register is cleared (written with a ‘0’), the corresponding port pin’s polarity is retained. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2 .

Table 11. Polarity inversion port 0 register (address 04h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Polarity inversion port 0 register (address 04h)

Table 12. Polarity inversion port 1 register (address 05h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0

Table 12. Polarity inversion port 1 register (address 05h)*...continued*

Bit	7	6	5	4	3	2	1	0
Default	-	-	0	0	0	0	0	0

6.4.4 Configuration registers (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2.

Table 13. Configuration port 0 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 14. Configuration port 1 register (address 07h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	-	-	1	1	1	1	1	1

6.4.5 Output drive strength registers (40h, 41h, 42h, 43h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 41 CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41 CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See 7.2 for more details. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2.

Table 15. Current control port 0A register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 16. Current control port 0B register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 17. Current control port 1A register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	

Table 17. Current control port 1A register (address 42h)*...continued*

Bit	7	6	5	4	3	2	1	0
Default	1	1	1	1	1	1	1	1

Table 18. Current control port 1B register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	-		-		CC1.5		CC1.4	
Default	-	-	-	-	1	1	1	1

6.4.6 Input latch registers (44h, 45h)

The input latch registers (registers 44 and 45) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0 and 1). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See Figure 12

For example, if the P0_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read ‘1’. The next read of the input port register bit 4 register should now read ‘0’.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is not cleared if the input latch register changes from latched to non-latched configuration.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2.

Table 19. Input latch port 0 register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

Table 20. Input latch port 1 register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	-	-	0	0	0	0	0	0

6.4.7 Pullup/pulldown enable registers (46h, 47h)

These registers allow the user to enable or disable pullup/pulldown resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pullup/pulldown resistors. Setting the bit to logic 0 disconnects the pullup/pulldown resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see Section 6.4.11). Use the pullup/pulldown registers to select either a pullup or pulldown resistor. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2.

Table 21. Pullup/pulldown enable port 0 register (address 46h)

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

Table 22. Pullup/pulldown enable port 1 register (address 47h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	-	-	0	0	0	0	0	0

6.4.8 Pullup/pulldown selection registers (48h, 49h)

The I/O port can be configured to have pullup or pulldown resistor by programming the pullup/pulldown selection register. Setting a bit to logic 1 selects a 100 kΩ pullup resistor for that I/O pin. Setting a bit to logic 0 selects a 100 kΩ pulldown resistor for that I/O pin. If the pullup/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 kΩ with minimum of 50 kΩ and maximum of 150 kΩ. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2 .

Table 23. Pullup/pulldown selection port 0 register (address 48h)

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

Table 24. Pullup/pulldown selection port 1 register (address 49h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	-	-	1	1	1	1	1	1

6.4.9 Interrupt mask registers (4Ah, 4Bh)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be deasserted. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2 .

Table 25. Interrupt mask port 0 register (address 4Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

Table 26. Interrupt mask port 1 register (address 4Bh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	-	-	1	1	1	1	1	1

6.4.10 Interrupt status registers (4Ch, 4Dh)

These read-only registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2 .

Table 27. Interrupt status port 0 register (address 4Ch) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

Table 28. Interrupt status port 1 register (address 4Dh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	-	-	0	0	0	0	0	0

6.4.11 Output port configuration register (4Fh)

The output port configuration register selects port-wise push-pull or open-drain I/O stage.

A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see Fig 5). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (4Fh) before the configuration register (06h and 07h) sets the port pins as outputs.

ODEN0 configures Port 0_x and ODEN1 configures Port 1_x.

Table 29. Output port configuration register (address 4Fh)

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

6.4.12 Interrupt edge registers (50h, 51h, 52h, 53h)

These registers determine what action on an input pin will cause an interrupt along with the Interrupt Mask registers (4Ah and 4Bh). If the Interrupt Mask is enabled (a 0 in the Mask register) and the action at the corresponding pin matches the required activity, the $\overline{INT}$ output will become active. The default value for each pin is 0 or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input port (00h or 01h). If the Interrupt edge register entry is set to 03h, any edge, positive- or negative-going, causes an interrupt event. If an entry is 01h, only a positive-going edge will cause an interrupt event, while a 02h will require a negative-going edge to cause an interrupt event. A register write operation is described in 6.10.1.1. A register read operation is described in Section 6.10.1.2 .

Table 30. Interrupt edge port 0A register (address 50h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Table 31. Interrupt edge port 0B register (address 51h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Table 32. Interrupt edge port 1A register (address 52h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Table 33. Interrupt edge port 1B register (address 53h)

Bit	7	6	5	4	3	2	1	0
Symbol	-		-		IE1.5		IE1.4	
Default	-	-	-	-	0	0	0	0

6.4.13 Interrupt clear registers (54h, 55h)

These write-only registers clear individual interrupt sources. Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the $\overline{INT}$will be cleared. After writing a logic 1 the bit returns to logic 0. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2.

Table 34. Interrupt clear port 0 register (address 54h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

Table 35. Interrupt clear port 1 register (address 55h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	-	-	0	0	0	0	0	0

6.4.14 Input port without interrupt clear registers (56h, 57h)

These read-only registers function exactly like Input Port 0 and 1 (00h and 01h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. The port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. A register write operation is described in Section 6.10.1.1. A register read operation is described in Section 6.10.1.2 .

Table 36. Input port without interrupt clear port 0 register (address 56h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	II0.7	II0.6	II0.5	II0.4	II0.3	II0.2	II0.1	II0.0
Default	x	x	x	x	x	x	x	x

Table 37. Input port without interrupt clear port 1 register (address 57h) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	II1.5	II1.4	II1.3	II1.2	II1.1	II1.0
Default	-	-	x	x	x	x	x	x

6.4.15 Output port configuration register pair (bit-wise) (58h, 59h)

The output port configuration registers modify bit-wise push-pull or open-drain states set by the port-wise setting in Output port configuration register (4Fh). If the ODENx (4Fh) bit is set to logic 0 (push-pull), any bit set to logic 1 in the IOCRx register (4Fh) will reverse the output state of that pin only to open-drain. When the ODENx bit is set to logic 1 (open-drain), a logic 1 in IOCRx will set that pin only to push-pull. The recommended command sequence is to program ODENx (4Fh) first, then this register (58h, 59h) before the configuration register (06h and 07h) sets the port pins as outputs.

Table 38. Output port configuration register 0 (bit-wise) (address 58h)

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

Table 39. Output port configuration register 1 (bit-wise) (address 59h)

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	-	-	0	0	0	0	0	0

6.4.16 Switch debounce enable registers (5Ah, 5Bh)

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P0_0 is designated as the oscillator input. If P0_0 is not configured as input and if SD0.0 is not set to logic 1, then switch debounce logic is not connected to any pin. See 6.9 for "Switch debounce circuitry" for further information.

Table 40. Switch debounce enable Port 0 register (address 5Ah) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

Table 41. Switch debounce enable Port 1 register (address 5Bh) bit description

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	-	-	0	0	0	0	0	0

6.4.17 Switch debounce count register (5Ch)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P0_0, determines the debounce time (for example, the debounce time will be 10 ms if this register is set to 0Ah and external oscillator frequency is 1 MHz). See Section 6.9 for further information.

Table 42. Switch debounce count register (address 5Ch) bit description

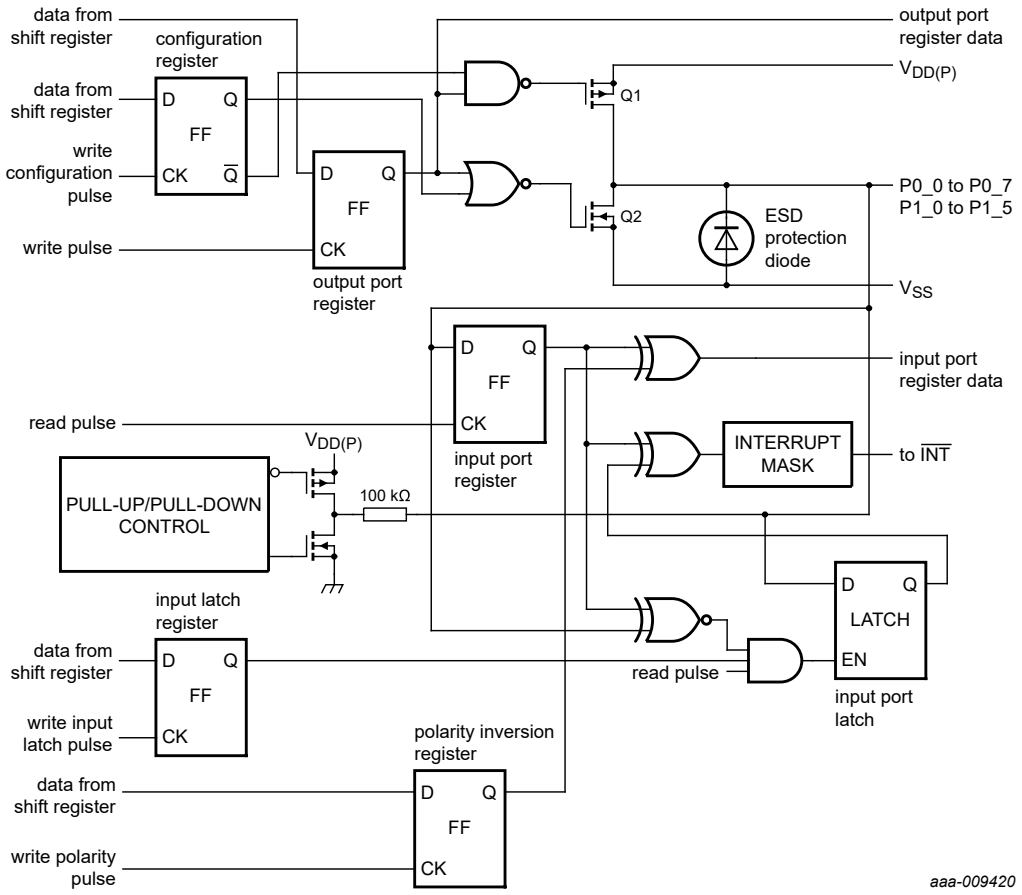
The switch debounce logic is disabled if this register is set to 00h.

Bit	7	6	5	4	3	2	1	0
Symbol	SDC0.7	SDC0.6	SDC0.5	SDC0.4	SDC0.3	SDC0.2	SDC0.1	SDC0.0
Default	0	0	0	0	0	0	0	0

6.5 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high impedance input. The input voltage may be raised above $V_{DD(P)}$ to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either $V_{DD(P)}$ or V_{SS}. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



On power-up or reset, all registers return to default values

Figure 5. Simplified schematic of the I/Os (P0_0 to P0_7, P1_0 to P1_5)

6.6 Power-on reset

When power (from 0 V) is applied to $V_{DD(P)}$, an internal power-on reset holds the PCAL9714 in a reset condition until $V_{DD(P)}$ has reached VPOR. At that time, the reset condition is released and the PCAL9714 registers and SPI bus state machine initializes to their default states. After that, $V_{DD(P)}$ must be lowered to below VPOR and back up to the operating voltage for a power-reset cycle. See Section 7.3.

6.7 Reset input ($\overline{RESET}$)

The $\overline{RESET}$ input can be asserted to initialize the system while keeping the $V_{DD(P)}$ at its operating level. A reset can be accomplished by holding the $\overline{RESET}$ pin LOW for a minimum of tw(rst) The PCAL9714 registers and SPI bus state machine are changed to their default state once $\overline{RESET}$ is LOW (0). When $\overline{RESET}$ is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pullup resistor to $V_{DD(SPI)}$ if no active connection is used.

6.8 Interrupt output ($\overline{INT}$)

The $\overline{INT}$ output has an open-drain structure and requires pullup resistor to $V_{DD(P)}$ or $V_{DD(SPI)}$ depending on the application. When any current input port state differs from its corresponding input port register state, the interrupt output pin is asserted (logic 0) to indicate the system master (MCU) that one of input port states has

changed. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

In order to enable the interrupt output, the following three conditions must be satisfied:

• The GPIO must be configured as an input port by writing "1" to configuration port registers (06h, 07h)

• The interrupt mask registers (4Ah, 4Bh) must set to "0" to unmask interrupt sources.

• The interrupt edge registers (50h to 55h) select what action on each input pin will cause an interrupt; there are four different interrupt trigger modes: level trigger, rising-edge trigger, falling-edge trigger, or any edge trigger.

The input latch registers (44h, 45h) control each input pin either to enable latched input state or non-latched input state. When input pin is set to latch state, it will hold or latch the input pin state (keep the logic value) and generate an interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

Any interrupt status bit can be cleared and $\overline{INT}$ pin deasserted by using one of the following methods and conditions:

- Power on reset (POR), hardware reset from $\overline{RESET}$ pin
- Read input port registers (00h, 01h)
- Write logic 1 to interrupt clear registers (54h, 55h)
- Write logic 1 to interrupt mask registers (4Ah, 4Bh)
- Write logic 0 to configuration registers (06h, 07h), set pin as output port.
- Input pin goes back to its initial state in level trigger and non-latch mode
- Input pin goes back to its initial state in level trigger and change latch to non-latch Mode
- Change the interrupt trigger mode from level trigger to edge trigger or vice versa in interrupt edge registers

When using the input latch feature, the input pin state is latched. The interrupt is deasserted only when data is read from the port that generated the interrupt. The interrupt reset occurs when $\overline{CS}$ is deasserted (from LOW to HIGH). Any change of the inputs after resetting is detected and is transmitted as $\overline{INT}$.

6.9 Switch debounce circuitry

Mechanical switches do not make clean make-or-break connections and the contacts can ‘bounce’ for a significant period of time before settling into a steady-state condition. This can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The PCAL9714 implements hardware to ease the hardware interface by debouncing switch closures with dedicated hardware. P0_0 to P0_7, P1_0 to P1_5 can enable this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a programmable duration. The circuit block diagram (Figure 7) shows the functional blocks consisting of an external oscillator, counter, exclusive-NOR gate, and D flip-flop. When the input does not equal the output, the XNOR gate issues a counter reset. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output. Figure 8 shows the typical opening and closing switch debounce operation.

To use the debounce circuitry, set the port pins (P0_0 to P0_7, and P1_0 to P1_5) with switches attached in the Switch Debounce Enable 0 and 1 registers (5Ah, 5Bh). Connect an external oscillator signal on P0_0 which serves as a time base to the debounce timer. Finally, set a delay time in the Switch Debounce Count register (5Ch). The combination of time base of the external oscillator and the debounce count sets the qualification period or t_{DP} in Figure 8. Note that all debounce counters will use the same time base and count, but they all function independently.

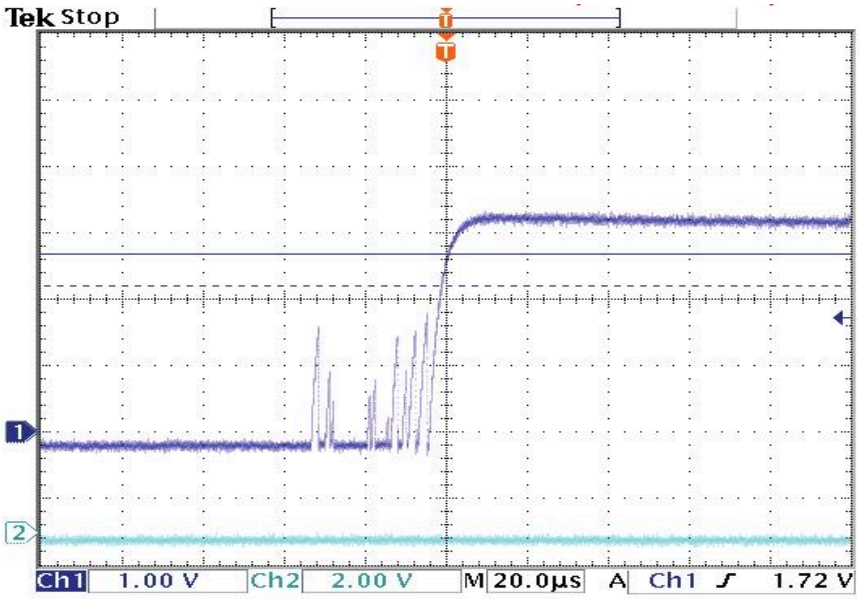
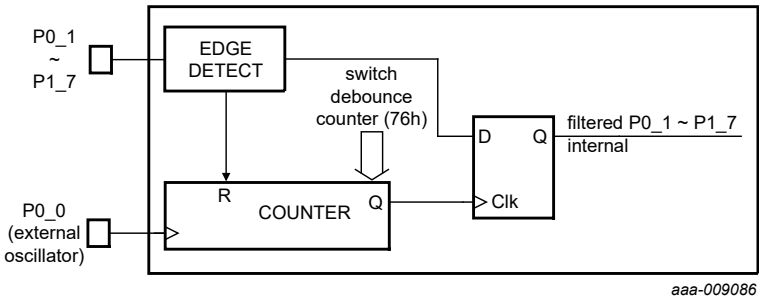
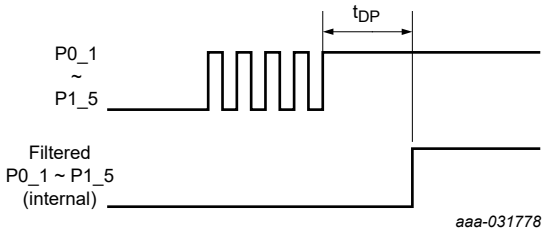


Figure 6. Switch contact bounce



When the external clock is first connected, it must wait 9 clock cycles for the debounce circuit in normal operation.

Figure 7. Debounce block diagram



t_{DP} = [PERIOD of EXT CLOCK] * [Debounce counter(5C)] = 1 µs * 10 = 10 µs (if external clock = 1 MHz, debounce count register (5Ch) = 0Ah)

Figure 8. Switch debounce timing

6.10 Bus transactions

The PCAL9714 is an SPI bus slave device. Data is exchanged between the master and PCAL9714 through read and write commands using the SPI bus.

6.10.1 SPI interface (addressable SPI)

This SPI interface of the PCAL9714 is called Global Chip Select or Addressable SPI.

This is a slave-only SPI and not fully duplex, that is, it cannot read/write at the same time.

The SPI interface consists of four pins $\overline{CS}$ SCLK, SDIN and SDOUT. Table 43 shows the pin names and description for the SPI interface.

Table 43. SPI pins

SPI pin name	Pin description
$\overline{CS}$	Chip Select input (sometimes called SS). The chip select line selects the slave device by the host processor (bus master). If multiple slave devices are connected to the same $\overline{CS}$ signal all the connected slaves are selected. Slave devices that are not selected do not interfere with the SPI bus activity. This signal is sometimes called SS or Slave Select. This is an active LOW signal.
SCLK	Serial clock input. SCLK is the serial clock input to the device. This clock synchronizes shifting and sampling of the information on the two data lines. It should be in its idle state (LOW) during the falling and rising edge of $\overline{CS}$.
SDIN	Serial data input (sometimes called MOSI). Serial Data Input. Data is sampled into the shift register on the rising edge of SCLK. The device ignores all activity on SDIN except when $\overline{CS}$ is asserted (LOW). This signal is sometimes called MOSI or Master Out, Slave In.
SDOUT	Serial data output (sometimes called MISO). Serial Data Output. SDOUT is always high-impedance except when a valid slave is addressed with R/$\overline{W}$ set to one and a valid register address is specified. SDOUT is driven on the falling edge of SCLK. This signal is sometimes called MISO or Master In, Slave Out.

This SPI implementation allows multiple slaves to be connected to the same $\overline{CS}$ with each slave identified using a unique slave address. PCAL9714 supports only one address pin or 4 slave addresses, as shown in Section 6.1.

The data transfers are [16 + (N × 8)] bits wide for N bytes of data with MSB transferred first. The first 7 bits indicate the address of the slave to be accessed, the eighth bit indicates the types of access (read or write), the next 8 bits specify the register address, and the last N × 8 bits consist of data.

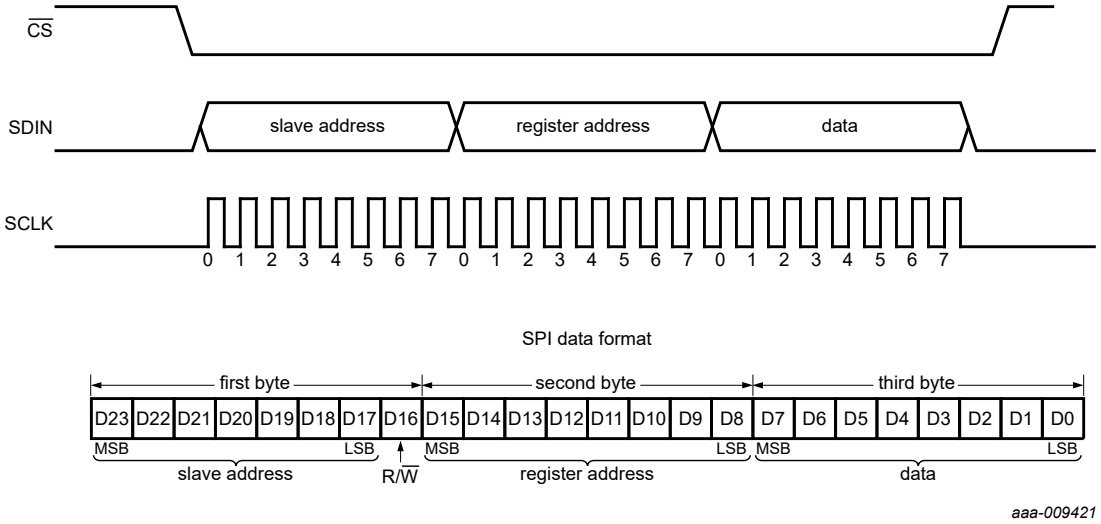


Figure 9. SPI data format

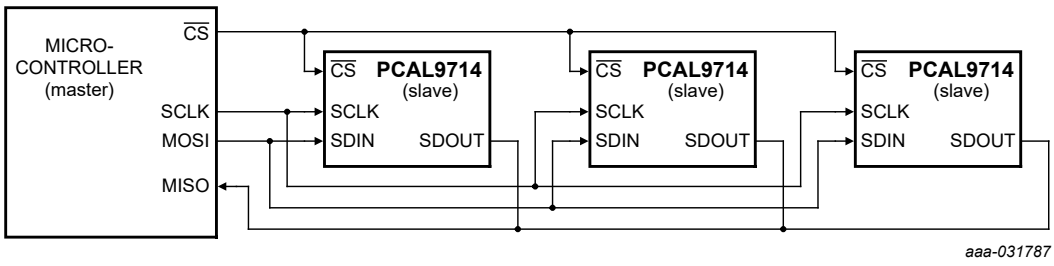


Figure 10. System level connections

6.10.1.1 SPI write access sequence

Register write sequences always begin from the bus idle condition. The bus idle condition refers to the $\overline{CS}$ being HIGH and the SCLK being LOW.

The registers are written using the following write sequence for one byte of data (from a bus idle condition):

1. Drive $\overline{CS}$ LOW. This enables the internal shift register.
2. Shift 24 bits of data into the device in a MSB-first fashion. Data is driven on the falling edge of SCLK and must be stable during the rising edge of SCLK.
3. The eighth bit of the data should be a '0', indicating it is write transfer.
4. The second 8 bits of data should be the address of the register that is intended to write.
5. After the last bit of data is transferred, drive SCLK LOW if there is no more data to be transferred.
6. Deassert $\overline{CS}$ (drive it HIGH).

If fewer than 24 bits of data are transferred before deasserting $\overline{CS}$ then the data is ignored and the register will not be updated. The write transfer format is shown in Figure 11.

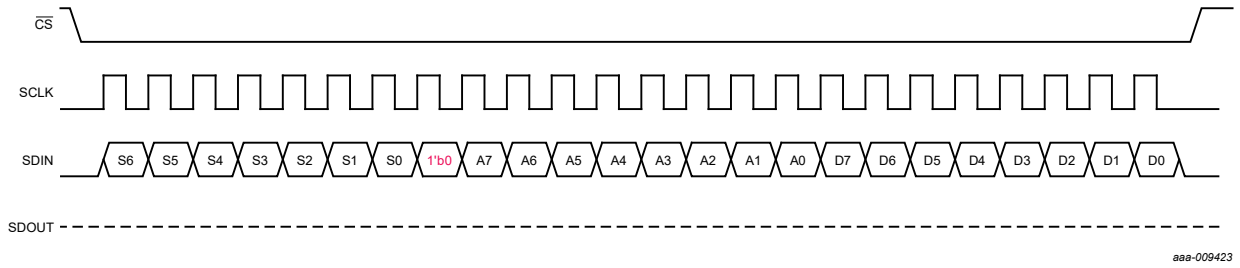


Figure 11. SPI write access

If more than 24 bits of data are transferred, that is, there are more than 24 clock pulses before deasserting the $\overline{CS}$, the register address is auto incremented. Auto Increment is discussed in Section 6.10.1.3.

6.10.1.2 SPI read access sequence

The registers are read using the following read sequence for one byte of data (from a bus idle condition):

1. Drive $\overline{CS}$ LOW.
2. Shift 24 bits of data into the device in an MSB-first fashion. The eighth bit should be a '1' indicating it is read transfer.
3. The next 8 bits should be the address of the register that is intended to read.
4. The last 8 bits sent in by the master are dummy data bits which are ignored.
5. The MSB of the read data is driven on the falling edge of the 17th clock cycle on SDOUT.
6. After all 8 bits have been read deassert $\overline{CS}$.

The read transfer format is shown in Figure 12.

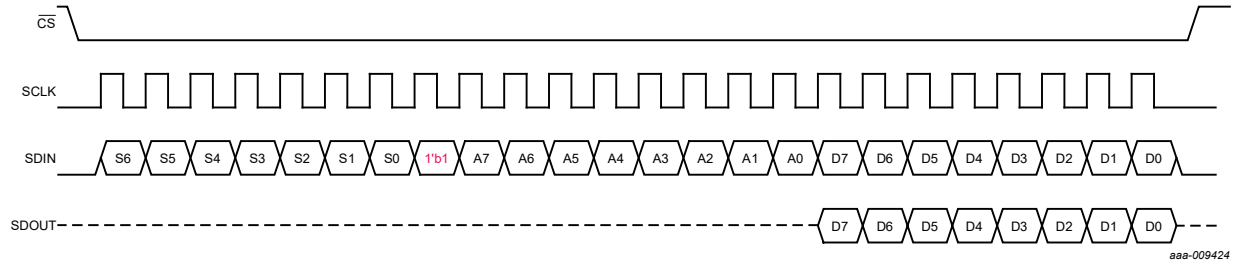


Figure 12. SPI read access

The SDOUT pin is high-impedance for the first 16 cycles of the read cycle. The SDOUT pin is driven only if a valid register address has been specified. The dummy data on the SDIN for the last 8 clock pulses is not clocked into the register.

If more than 24 clocks are issued before deasserting $\overline{CS}$, then the register address is automatically incremented and the following register in the register map is read out.

A write and a read cannot occur in a single transaction. The Chip Select ($\overline{CS}$) must be deasserted between a read and write operation

6.10.1.3 SPI and auto increment

Auto Increment is completely dependent on the deassertion of chip select. The register address is incremented sequentially and once the last address in the register map is reached, the address is rolled over to the first address in the register map.

When reading using auto increment it is the user's responsibility to supply clock pulses that are multiple of 8 to read out the whole register.

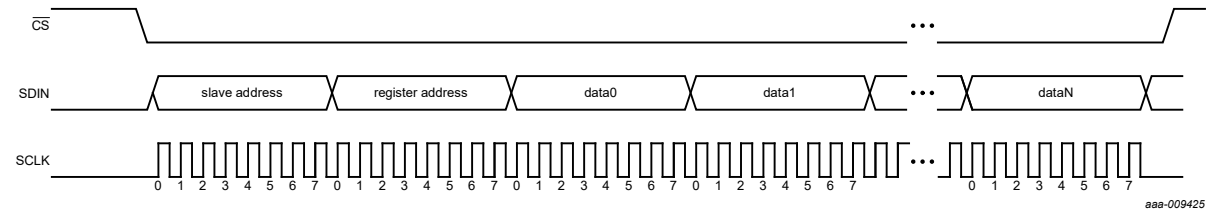


Figure 13. Auto increment and write

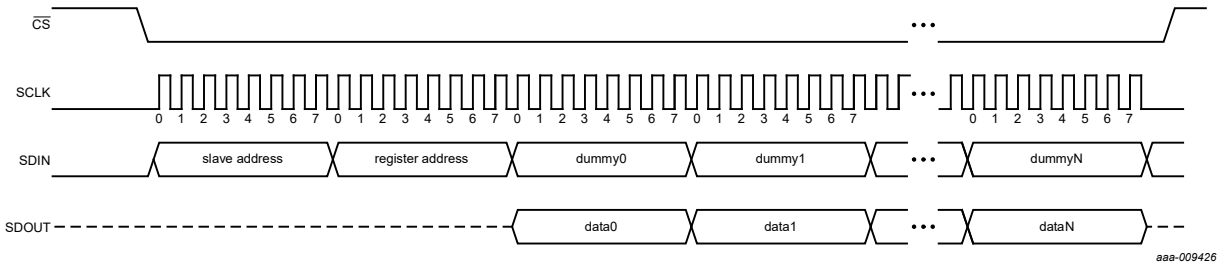
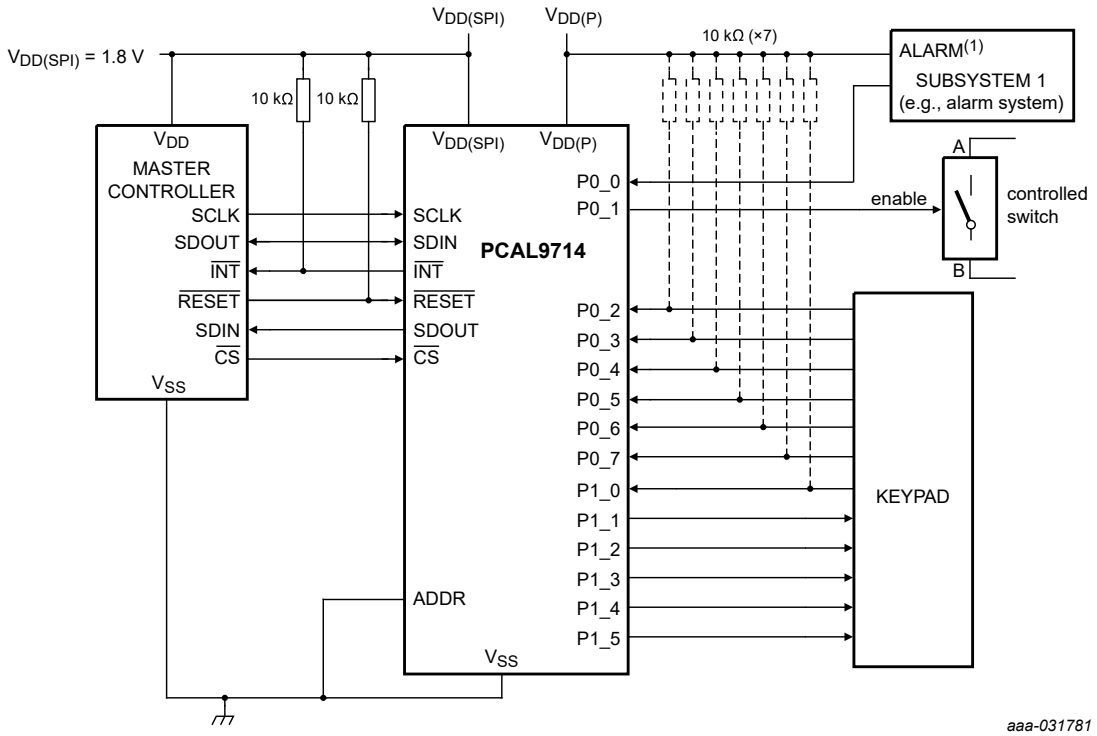


Figure 14. Auto increment and read

7 Application information



Device address configured as 0100 000x for this example.

P0_0 and P0_2 through P1_0 are configured as inputs.

P0_1 and P1_1 through P1_5 are configured as outputs.

1. External resistors are required for inputs (on P port) that may float. Also, internal pullup or pulldown may be used to eliminate the need for external components. If a driver to an input will never let the input float, a resistor is not needed. If an output in the P port is configured as a push-pull output there is no need for external pullup resistors. If an output in the P port is configured as an open-drain output, external pullup resistors are required.

Figure 15. Typical application

7.1 Minimizing IDD when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 15. Since the LED acts as a diode, when the LED is off the I/ O V_I is about 1.2 V less than $V_{DD(P)}$. The supply current, $I_{DD(P)}$, increases as V_I becomes lower than $V_{DD(P)}$.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 16 shows a high value resistor in parallel with the LED. Figure 17 shows $V_{DD(P)}$ less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above $V_{DD(P)}$ and prevents additional supply current consumption when the LED is off.

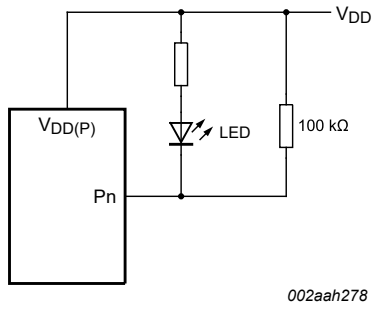


Figure 16. High value resistor in parallel with the LED

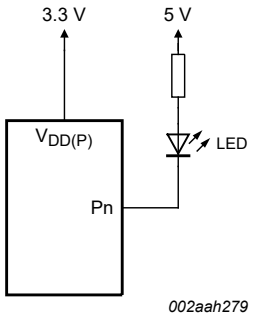


Figure 17. Device supplied by a lower voltage

7.2 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

Fig 18 shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 10b, then only two of the fingers are active, reducing the current drive capability by 50 %.

Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through V_{DD} and V_{SS} package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

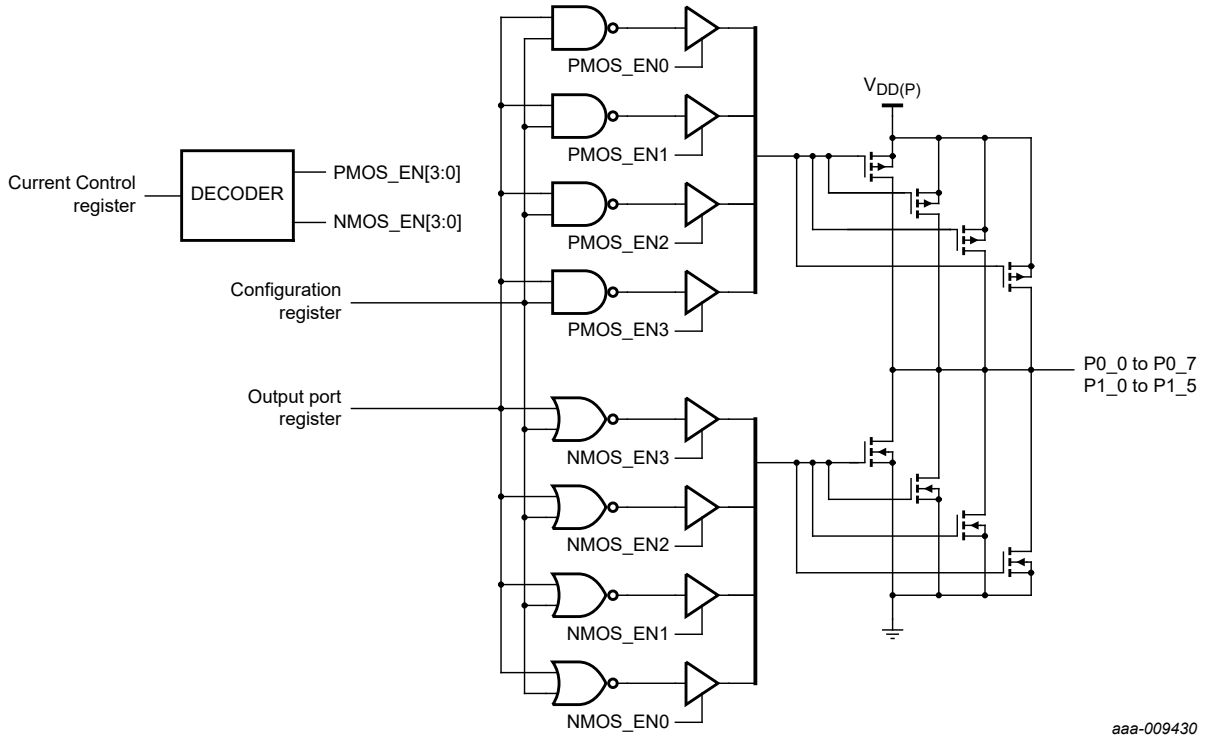


Figure 18. Simplified output stage

7.3 Power-on reset requirements

In the event of a glitch or data corruption, PCAL9714 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in Figure 19 and Figure 20.

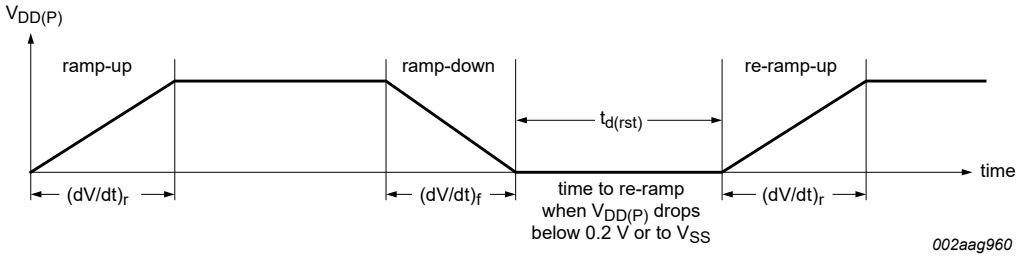


Figure 19. $V_{DD(P)}$ is lowered below 0.2 V or to 0 V and then ramped up to $V_{DD(P)}$

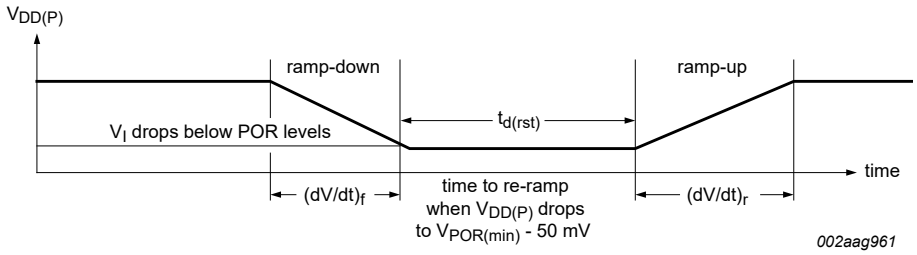


Figure 20. $V_{DD(P)}$ is lowered below the POR threshold, then ramped back up to $V_{DD(P)}$

Table 44 specifies the performance of the power-on reset feature for PCAL9714 for both types of power-on reset.

Table 44. Recommended supply sequencing and ramp rates

T_{amb} = 25 °C (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	Figure 19		0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	Figure 19		0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	Figure 19; re-ramp time when $V_{DD(P)}$ drops below 0.2 V or to V_{SS})		1	-	-	µs
		Figure 20; re-ramp time when $V_{DD(P)}$ drops to $V_{POR(min)}$ - 50 mV)		1	-	-	µs
$\Delta V_{DD(gl)}$	glitch supply voltage difference	Figure 21	[1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	Figure 21	[2]	-	-	10	µs
$V_{POR(trip)}$	power-on reset trip voltage	falling $V_{DD(P)}$		0.7	-	-	V
		rising $V_{DD(P)}$		-	-	1.5	V

[1] Level that $V_{DD(P)}$ can glitch down to with a ramp rate = 0.4 µs/V, but not cause a functional disruption when $t_{w(gl)VDD}$ < 1 µs.
[2] Glitch width that will not cause a functional disruption when $\Delta V_{DD(gl)} = 0.5 \times V_{DD(P)}$.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ($t_{w(gl)VDD}$) and glitch height ($\Delta V_{DD(gl)}$) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 21 and Table 44 provide more information on how to measure these specifications.

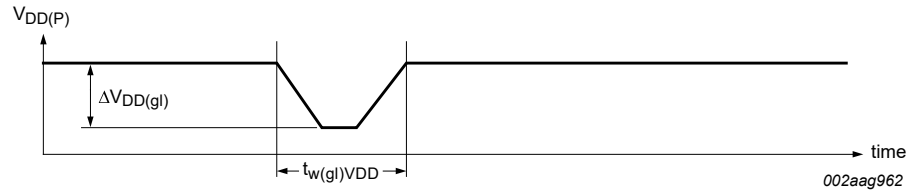


Figure 21. Glitch width and glitch height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the SPI bus state machine are initialized to their default states. The value of V_{POR} differs based on the $V_{DD(P)}$ being lowered to or from 0 V. Figure 22 and Table 44 provide more details on this specification.

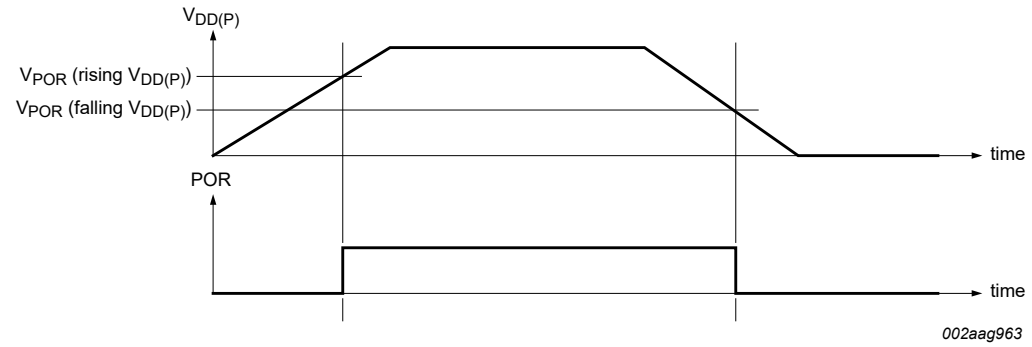


Figure 22. Power-on reset voltage (V_{POR})

7.4 Device current consumption with internal pullup and pulldown resistors

The PCAL9714 integrates programmable pullup and pulldown resistors to eliminate external components when pins are configured as inputs and pullup or pulldown resistors are required (for example, nothing is driving the inputs to the power supply rails. Since these pullup and pulldown resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pullup or pulldown function is selected in registers 48h and 49h, while the resistor is connected by the enable registers 46h and 47h. The configuration of the resistors is shown in Figure 5.

If the resistor is configured as a pullup, that is, connected to V_{DD}, a current will flow from the $V_{DD(P)}$ pin through the resistor to ground when the pin is held LOW. This current will appear as additional I_{DD} upsetting any current consumption measurements.

In the same manner, if the resistor is configured as a pulldown and the pin is held HIGH, current will flow from the power supply through the pin to the V_{SS} pin. While this current will not be measured as part of I_{DD}, one must be mindful of the 200 mA limiting value through V_{SS}.

The pullup and pulldown resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 kΩ with a nominal 100 kΩ value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See Figure 26 for a graph of supply current versus the number of pullup resistors.

8 Limiting values

Table 45. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(SPI)}$	SPI bus supply voltage			-0.5	+6.5	V
$V_{DD(P)}$	supply voltage port P			-0.5	+6.5	V
$V_{I(P)}$	input voltage on all ports		[1]	-0.5	+6.5	V
$V_{O(P)}$	output voltage on all ports		[1]	-0.5	+6.5	V
$V_{I(I)}$	input voltage on SPI-bus, $\overline{RESET}$, ADDR			-0.5	+6.5	V
$V_{O(I)}$	output voltage on SPI-bus, $\overline{INT}$			-0.5	+6.5	V
I_{IK}	input clamping current	ADDR, $\overline{RESET}$, SCLK, $\overline{CS}$; $V_I < 0$ V		-	±20	mA
I_{OK}	output clamping current	$\overline{INT}$; $V_O < 0$ V		-	±20	mA
I_{IOK}	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD(P)}$		-	±20	mA
		SDIN, SDOUT; $V_O < 0$ V or $V_O > V_{DD(SPI)}$		-	±20	mA
I_{OL}	LOW-level output current	continuous; P port; V_O = 0 V to $V_{DD(P)}$		-	50	mA
		continuous; SDOUT, $\overline{INT}$; V_O = 0 V to $V_{DD(SPI)}$		-	25	mA
I_{OH}	HIGH-level output current	continuous; P port; V_O = 0 V to $V_{DD(P)}$		-	25	mA
I_{DD}	supply current	continuous through V_{SS}		-	200	mA
$I_{DD(P)}$	supply current port P	continuous through $V_{DD(P)}$		-	160	mA
$I_{DD(SPI)}$	SPI bus supply current	continuous through $V_{DD(SPI)}$		-	10	mA
T_{stg}	storage temperature			-65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	+150	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

9 Recommended operating conditions

Table 46. Operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(SPI)}$	SPI supply voltage			1.1	5.5	V
$V_{DD(P)}$	supply voltage port P			1.65	5.5	V
V_{IH}	HIGH-level input voltage	SCLK, SDIN, $\overline{CS}$, $\overline{RESET}$, ADDR		$0.7 \times V_{DD(SPI)}$	5.5	V
		P1_5 to P0_0		$0.7 \times V_{DD(P)}$	5.5	V
V_{IL}	LOW-level input voltage	SCLK, SDIN, $\overline{CS}$, $\overline{RESET}$, ADDR		-0.5	$0.3 \times V_{DD(SPI)}$	V
		P1_5 to P0_0		-0.5	$0.3 \times V_{DD(P)}$	V
I_{OH}	HIGH-level output current	P1_5 to P0_0		-	10	mA
I_{OL}	LOW-level output current	P1_5 to P0_0		-	25	mA
T_{amb}	ambient temperature	operating in free air; PCAL9714HN		-40	+85	°C
		operating in free air; PCAL9714HN/Q900		-40	+125	°C

10 Thermal characteristics

Table 47. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	HVQFN24 package	[1]	66	K/W

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

11 Static characteristics

Table 48. Static characteristics for PCAL9714HN

T_{amb} = -40 °C to +85 °C; $V_{DD(SPI)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	I_I = -18 mA		-1.2	-	-	V
V_{POR}	power-on reset voltage	$V_I = V_{DD(P)}$ or V_{SS}; I_O = 0 mA		-	1.2	1.5	V
V_{OH}	HIGH-level output voltage[2]	P port; I_{OH} = -8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		1.2	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.8	-	-	V
		$V_{DD(P)}$ = 3 V		2.6	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.1	-	-	V
		P port; I_{OH} = -2.5 mA and CCX.X = 00b; I_{OH} = -5 mA and CCX.X = 01b; I_{OH} = -7.5 mA and CCX.X = 10b; I_{OH} = -10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.7	-	-	V
		$V_{DD(P)}$ = 3 V		2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.0	-	-	V
		SDOUT port					
		$V_{DD(SPI)} \leq$ 1.65 V, I_{OH} = -0.4 mA		0.8 x $V_{DD(SPI)}$	-	-	V
		$V_{DD(SPI)}$ > 1.65 V, I_{OH} = -4 mA		$V_{DD(SPI)}$ - 0.3	-	-	V
V_{OL}	LOW-level output voltage[2]	P port; I_{OL} = 8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.25	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.2	V
		P port; I_{OL} = 2.5 mA and CCX.X = 00b; I_{OL} = 5 mA and CCX.X = 01b; I_{OL} = 7.5 mA and CCX.X = 10b; I_{OL} = 10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.3	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.2	V
		SDOUT port					
		$V_{DD(SPI)} \leq$ 1.65 V, I_{OL} = 1.2 mA		-	-	0.2 x $V_{DD(SPI)}$	V
		$V_{DD(SPI)}$ > 1.65 V, I_{OL} = 4 mA		-	-	0.4	V
I_{OL}	LOW-level output current[3]	$\overline{INT}$; V_{OL} = 0.4 V; $V_{DD(P)}$ = 1.65 V to 5.5 V		3	[4]	-	mA
I_I	input current	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; $V_{DD(P)}$ = 1.65 V to 5.5 V; $V_I = V_{DD(SPI)}$ or V_{SS}		-	-	±1	µA

Table 48. Static characteristics for PCAL9714HN*...continued*

T_{amb} = -40 °C to +85 °C; $V_{DD(SPI)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{IH}	HIGH-level input current	P port without internal pullup resistor; V_I = $V_{DD(P)}$; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{IL}	LOW-level input current	P port without internal pullup resistor; V_I = V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{DD}	supply current	$I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on ADDR, SDIN, $\overline{CS}$ and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs					
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 5 MHz		-	500	750	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 5 MHz		-	300	500	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 5 MHz		-	200	350	µA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 0 MHz		-	3	12	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 0 MHz		-	2	6.5	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 0 MHz		-	1.5	4.5	µA
		Active mode; $I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on SDIN, $\overline{CS}$, ADDR, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; f_{SCLK} = 5 MHz; continuous register read with 100 pF load on SDOUT					
		$V_{DD(P)}$ = 3.6 V to 5.5 V		-	2500	4200	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V		-	2200	3200	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V		-	1800	2800	µA
		with pullups enabled; $I_{DD(SPI)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = V_{SS}; I_O = 0 mA; I/O = inputs with pullup enabled; f_{SCLK} = 0 kHz					
		$V_{DD(P)}$ = 1.65 V to 5.5 V		-	1.65	2.4	mA
ΔI_{DD}	additional quiescent supply current[5]	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; one input at $V_{DD(SPI)}$ - 0.6 V, other inputs at $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	30	µA
		P port, ADDR; one input at $V_{DD(P)}$ - 0.6 V, other inputs at $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	80	µA
C_i	input capacitance[6]	V_I = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	6	7	pF
C_{io}	input/output capacitance[6]	$V_{I/O}$ = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7	8	pF
		$V_{I/O}$ = $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7.5	8.5	pF
$R_{pu(int)}$	internal pullup resistance	input/output		50	100	150	kΩ
$R_{pd(int)}$	internal pulldown resistance	input/output		50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V or 3.6 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at $V_{DD(P)}$ = $V_{DD(SPI)}$ = 3.3 V and T_{amb} = 25 °C.
[2] The total current sourced by all I/Os must be limited to 160 mA.
[3] Each I/O must be externally limited to a maximum of 25 mA and each octal (P0_0 to P0_7 and P1_0 to P1_5) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and $V_{DD(SPI)}$ = $V_{DD(P)}$ = 3.3 V. Typical value for $V_{DD(SPI)}$ = $V_{DD(P)}$ < 2.5 V, V_{OL} = 0.6 V.
[5] Internal pullup/pulldown resistors disabled.
[6] Value not tested in production, but guaranteed by design and characterization.

Table 49. Static characteristics for PCAL9714HN/Q900

T_{amb} = -40 °C to +125 °C; $V_{DD(SPI)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	I_I = -18 mA		-1.2	-	-	V
V_{POR}	power-on reset voltage	V_I = $V_{DD(P)}$ or V_{SS}; I_O = 0 mA		-	1.2	1.5	V
V_{OH}	HIGH-level output voltage [2]	P port; I_{OH} = -8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		1.2	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.8	-	-	V
		$V_{DD(P)}$ = 3 V		2.6	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.1	-	-	V
		P port; I_{OH} = -2.5 mA and CCX.X = 00b; I_{OH} = -5 mA and CCX.X = 01b; I_{OH} = -7.5 mA and CCX.X = 10b; I_{OH} = -10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		1.1	-	-	V
		$V_{DD(P)}$ = 2.3 V		1.7	-	-	V
		$V_{DD(P)}$ = 3 V		2.5	-	-	V
		$V_{DD(P)}$ = 4.5 V		4.0	-	-	V
		SDOUT port					
		$V_{DD(SPI)}$ ≤ 1.65 V, I_{OH} = -0.4 mA		0.8 x $V_{DD(SPI)}$	-	-	V
		$V_{DD(SPI)}$ > 1.65 V, I_{OH} = -4 mA		$V_{DD(SPI)}$ - 0.3	-	-	V
V_{OL}	LOW-level output voltage [2]	P port; I_{OL} = 8 mA; CCX.X = 11b					
		$V_{DD(P)}$ = 1.65 V		-	-	0.45	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.25	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.20	V
		P port; I_{OL} = 2.5 mA and CCX.X = 00b; I_{OL} = 5 mA and CCX.X = 01b; I_{OL} = 7.5 mA and CCX.X = 10b; I_{OL} = 10 mA and CCX.X = 11b;					
		$V_{DD(P)}$ = 1.65 V		-	-	0.5	V
		$V_{DD(P)}$ = 2.3 V		-	-	0.3	V
		$V_{DD(P)}$ = 3 V		-	-	0.25	V
		$V_{DD(P)}$ = 4.5 V		-	-	0.2	V
		SDOUT port					

Table 49. Static characteristics for PCAL9714HN/Q900*...continued*

T_{amb} = -40 °C to +125 °C; $V_{DD(SPI)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
		$V_{DD(SPI)}$ ≤ 1.65 V, I_{OH} = 1.2 mA		-	-	0.2 x $V_{DD(SPI)}$	V
		$V_{DD(SPI)}$ > 1.65 V, I_{OH} = 4 mA		-	-	0.4	V
I_{OL}	LOW-level output current [3]	$\overline{INT}$; V_{OL} = 0.4 V; $V_{DD(P)}$ = 1.65 V to 5.5 V		3	[4]	-	mA
I_I	input current	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; $V_{DD(P)}$ = 1.65 V to 5.5 V; V_I = $V_{DD(SPI)}$ or V_{SS}		-	-	±1	µA
I_{IH}	HIGH-level input current	P port; V_I = $V_{DD(P)}$; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{IL}	LOW-level input current	P port; V_I = V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	1	µA
I_{DD}	supply current	$I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on ADDR, SDIN, $\overline{CS}$ and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs					
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 5 MHz		-	500	750	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 5 MHz		-	300	500	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 5 MHz		-	200	350	µA
		$V_{DD(P)}$ = 3.6 V to 5.5 V; f_{SCLK} = 0 MHz		-	3	12	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V; f_{SCLK} = 0 MHz		-	2	6.5	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V; f_{SCLK} = 0 MHz		-	1.5	4.5	µA
		Active mode; $I_{DD(SPI)}$ + $I_{DD(P)}$; SCLK, SDIN, $\overline{CS}$, P port, ADDR, $\overline{RESET}$; V_I on SDIN, $\overline{CS}$, ADDR, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = $V_{DD(P)}$; I_O = 0 mA; I/O = inputs; f_{SCLK} = 5 MHz; continuous register read with 100 pF load on SDOUT					
		$V_{DD(P)}$ = 3.6 V to 5.5 V		-	2500	4200	µA
		$V_{DD(P)}$ = 2.3 V to 3.6 V		-	2200	3200	µA
		$V_{DD(P)}$ = 1.65 V to 2.3 V		-	1800	2800	µA
		with pullups enabled; $I_{DD(SPI)}$ + $I_{DD(P)}$; P port, ADDR, $\overline{RESET}$; V_I on ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$ = $V_{DD(SPI)}$ or V_{SS}; V_I on P port = V_{SS}; I_O = 0 mA; I/O = inputs with pullup enabled; f_{SCLK} = 0 kHz					
		$V_{DD(P)}$ = 1.65 V to 5.5 V		-	1.65	2.4	mA
ΔI_{DD}	additional quiescent supply current[5]	ADDR, SCLK, SDIN, $\overline{CS}$, and $\overline{RESET}$; one input at $V_{DD(SPI)}$ - 0.6 V, other inputs at $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	30	µA
		P port, ADDR; one input at $V_{DD(P)}$ - 0.6 V, other inputs at $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	-	80	µA
C_i	input capacitance[6]	V_I = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	6	7	pF
C_{io}	input/output capacitance[6]	$V_{I/O}$ = $V_{DD(SPI)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7	8	pF

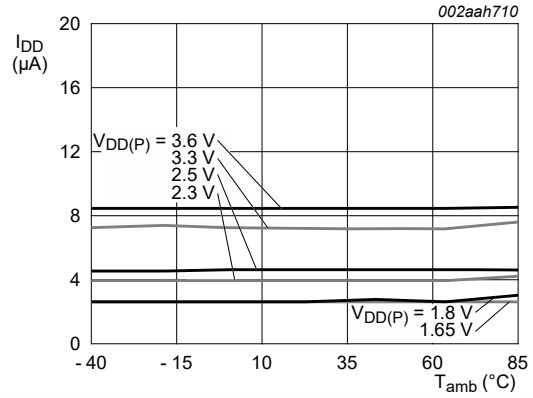
Table 49. Static characteristics for PCAL9714HN/Q900...*continued*

T_{amb} = -40 °C to +125 °C; $V_{DD(SPI)}$ = 0.8 V to 3.6 V; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
		$V_{I/O}$ = $V_{DD(P)}$ or V_{SS}; $V_{DD(P)}$ = 1.65 V to 5.5 V		-	7.5	8.5	pF
$R_{pu(int)}$	internal pullup resistance	input/output		50	100	150	kΩ
$R_{pd(int)}$	internal pulldown resistance	input/output		50	100	150	kΩ

[1] For I_{DD}, all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V or 3.6 V V_{DD}) and T_{amb} = 25 °C. Except for I_{DD}, the typical values are at $V_{DD(P)}$ = $V_{DD(SPI)}$ = 3.3 V and T_{amb} = 25 °C.
[2] The total current sourced by all I/Os must be limited to 160 mA.
[3] Each I/O must be externally limited to a maximum of 25 mA and each octal (P0_0 to P0_7 and P1_0 to P1_5) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
[4] Typical value for T_{amb} = 25 °C. V_{OL} = 0.4 V and $V_{DD(SPI)}$ = $V_{DD(P)}$ = 3.3 V. Typical value for $V_{DD(SPI)}$ = $V_{DD(P)}$ < 2.5 V, V_{OL} = 0.6 V.
[5] Internal pullup/pulldown resistors disabled.
[6] Value not tested in production, but guaranteed by design and characterization.

11.1 Typical characteristics



I_{DD} = $I_{DD(I2C\text{-}bus)}$ + $I_{DD(P)}$

Figure 23. Supply current versus ambient temperature

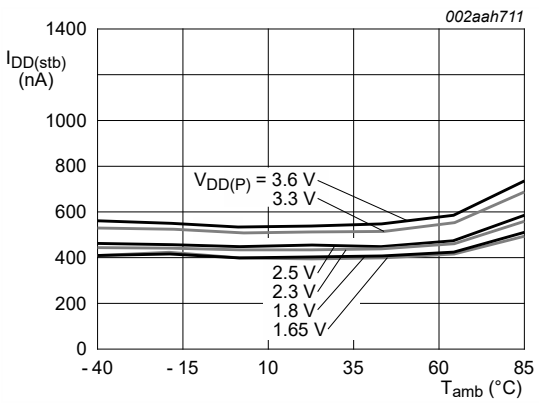
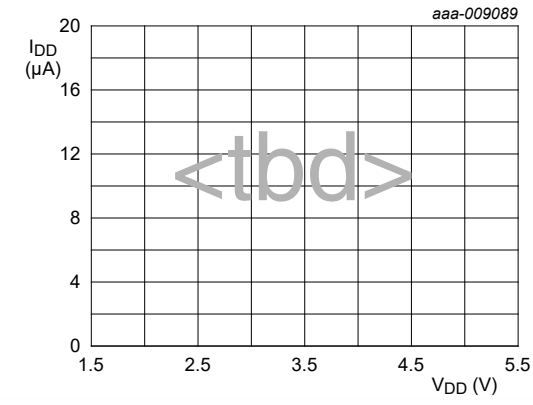


Figure 24. Standby supply current versus ambient temperature



T_{amb} = 25 °C

I_{DD} = $I_{DD(I2C\text{-}bus)}$ + $I_{DD(P)}$

Figure 25. Supply current versus supply voltage

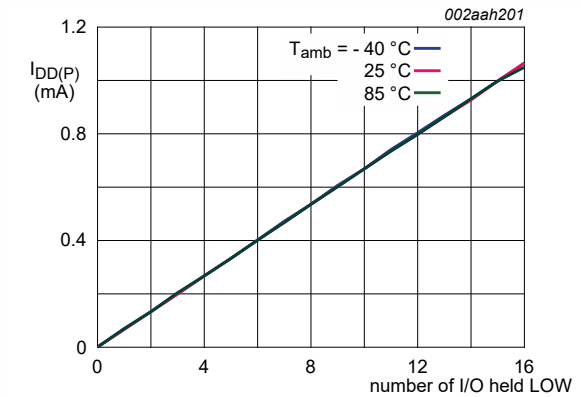
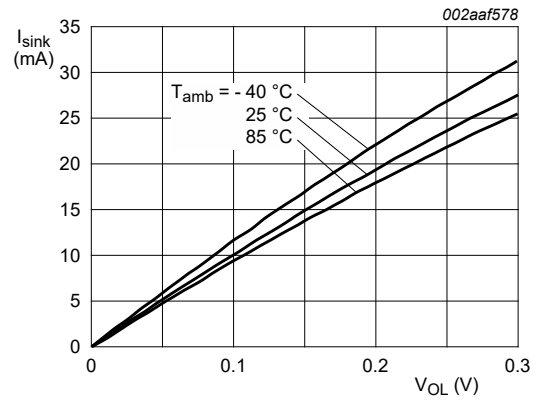
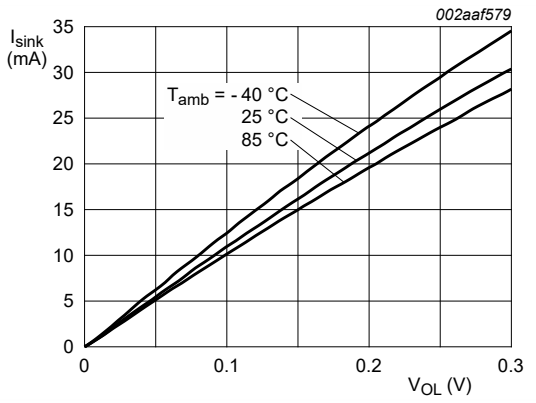


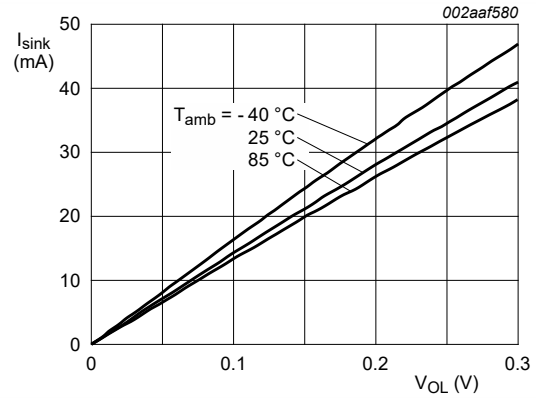
Figure 26. Supply current versus number of I/O held LOW



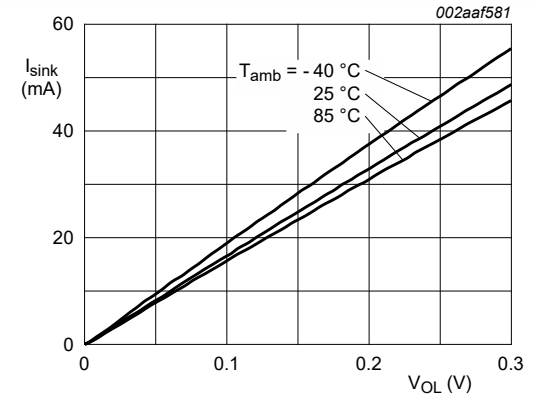
a. $V_{DD(P)}$ = 1.65 V



b. $V_{DD(P)}$ = 1.8 V

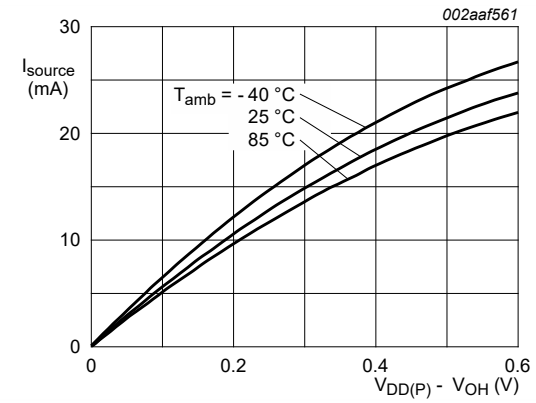


c. $V_{DD(P)}$ = 2.5 V

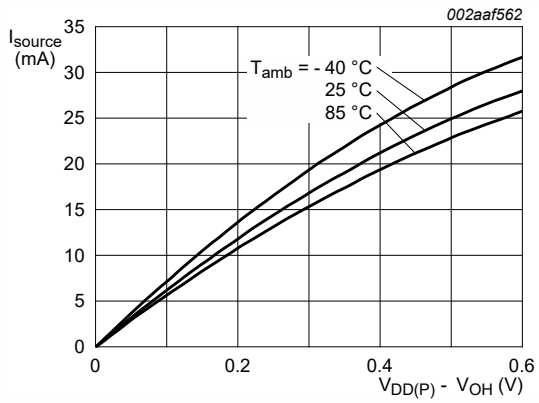


d. $V_{DD(P)}$ = 3.3 V

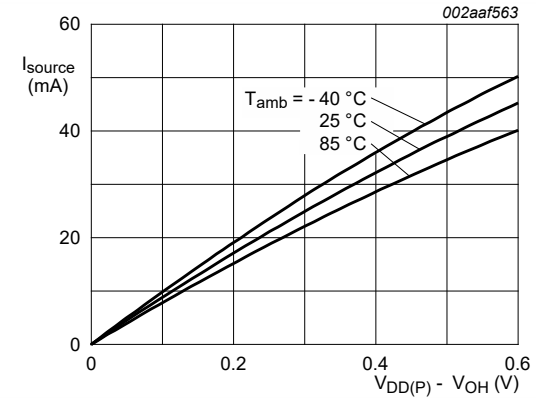
Figure 27. I/O sink current versus LOW-level output voltage with CCX.X = 11b



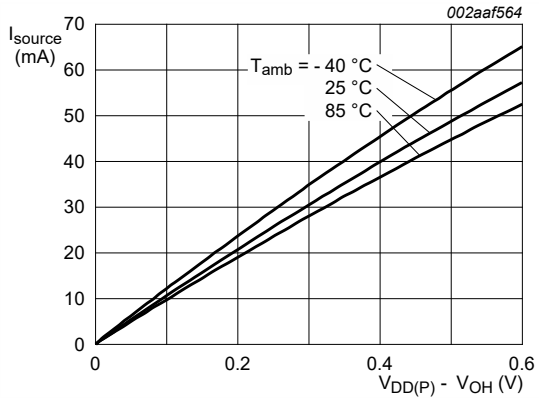
a. $V_{DD(P)}$ = 1.65 V



b. $V_{DD(P)}$ = 1.8 V

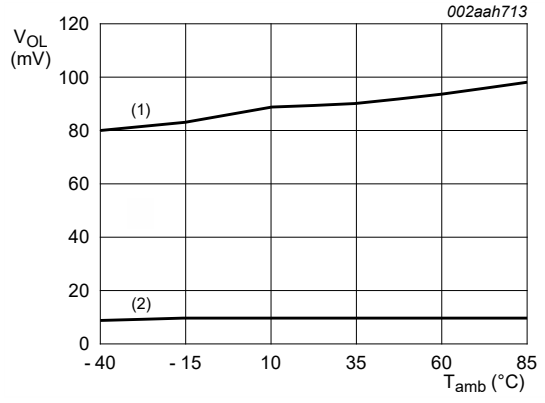


c. $V_{DD(P)}$ = 2.5 V



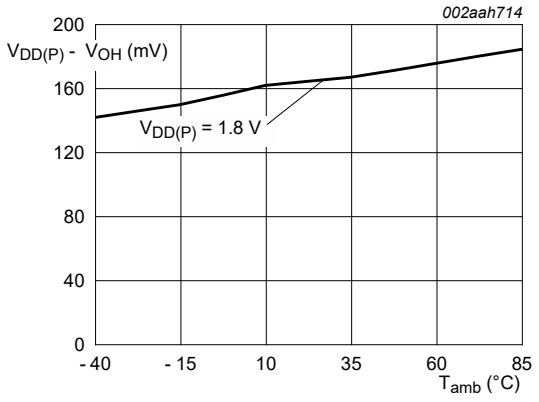
d. $V_{DD(P)}$ = 3.3 V

Figure 28. I/O source current versus HIGH-level output voltage with CCX.X = 11b



1. $V_{DD(P)}$ = 1.8 V; I_{sink} = 10 mA
2. $V_{DD(P)}$ = 1.8 V; I_{sink} = 1 mA

Figure 29. LOW-level output voltage versus temperature with CCX.X = 11b



I_{source} = -10 mA

Figure 30. I/O high voltage versus temperature with CCX.X = 11b

12 Dynamic characteristics

Table 50. SPI bus interface timing requirements

Guaranteed by design; over recommended operating free air temperature range, unless otherwise specified. See Figure 32

Symbol	Parameter	Conditions		$V_{DD(SPI)}$ ≤ 1.65 V		$V_{DD(SPI)}$ ≤ 5.5 V		Unit
				Min	Max	Min	Max	
f_{SCLK}	maximum input clock frequency			-	2	-	5	MHz
t_{LOW}	LOW period of the SCLK clock			250	-	100	-	ns
t_{HIGH}	HIGH period of the SCLK clock			250	-	100	-	ns
t_{DS}	SDIN to SCLK set-up time			20	-	20	-	ns
t_{DH}	SDIN to SCLK hold time			30	-	30	-	ns
t_{CSS}	CSn to SCLK rise set-up time			100	-	100	-	ns
t_{CS_HI}	minimum CSn deasserted HIGH time			200	-	200	-	ns
t_{CSH}	SCLK fall to CSn deasserted hold time			20	-	20	-	ns
$t_{DIS(SDOUT)}$	SDOUT disable time	CL = 100 pF		-	150	-	150	ns
$t_{V(SDOUT)}$	SDOUT valid time	CL = 100 pF		-	200	-	200	ns

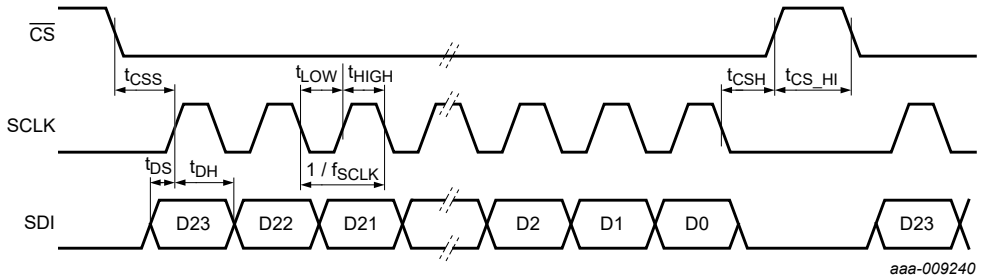


Figure 31. Definition of timing

Table 51. Reset timing requirements

Over recommended operating free air temperature range, unless otherwise specified. See Figure 34.

Symbol	Parameter	Conditions		SPI bus		Unit
				Min	Max	
$t_{w(rst)}$	reset pulse width			150	-	ns
$t_{rec(rst)}$	reset recovery time			500	-	ns
t_{rst}	reset time		[1]	600	-	ns

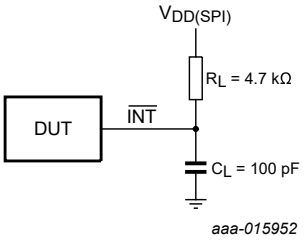
[1] Minimum time for SDOUT to become HIGH.

Table 52. Switching characteristics

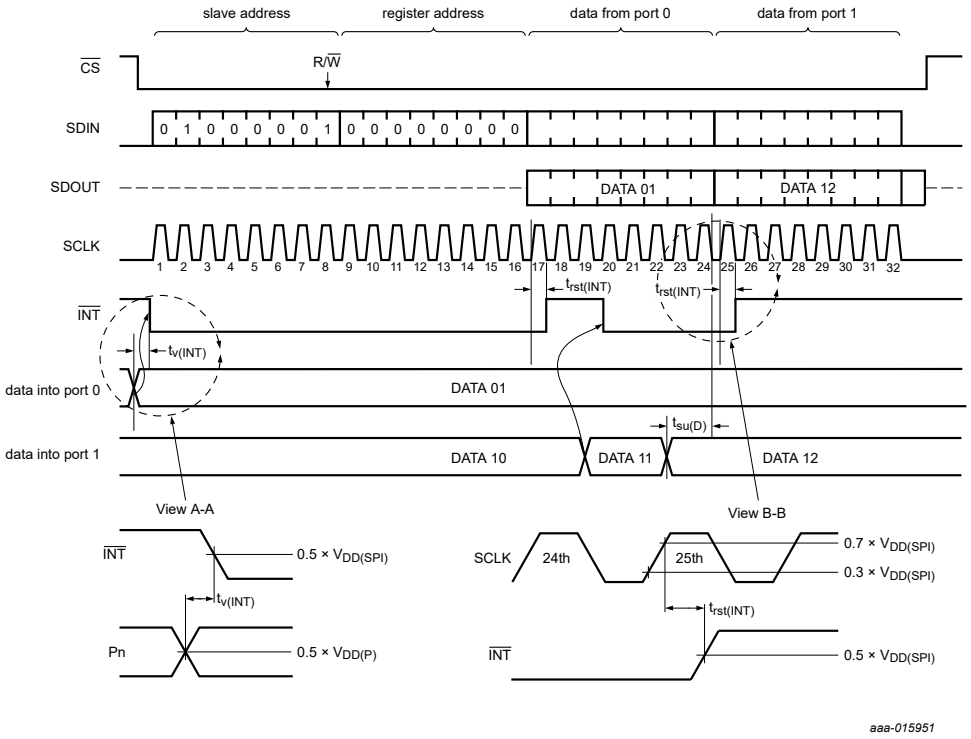
Over recommended operating free air temperature range; C_L ≤ 100 pF; unless otherwise specified. See Figure 33.

Symbol	Parameter	Conditions	SPI bus		Unit
			Min	Max	
$t_{v(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	µs
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCLK to $\overline{INT}$	-	1	µs
$t_{v(Q)}$	data output valid time	from SCLK to P port	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCLK	30	-	ns
$t_{h(D)}$	data input hold time	from P port to SCLK	10	-	ns

13 Parameter measurement information



a. Interrupt load configuration

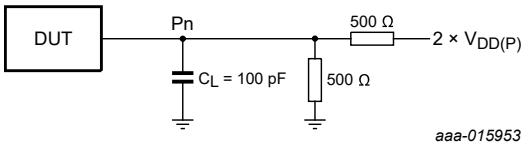


b. Voltage waveforms

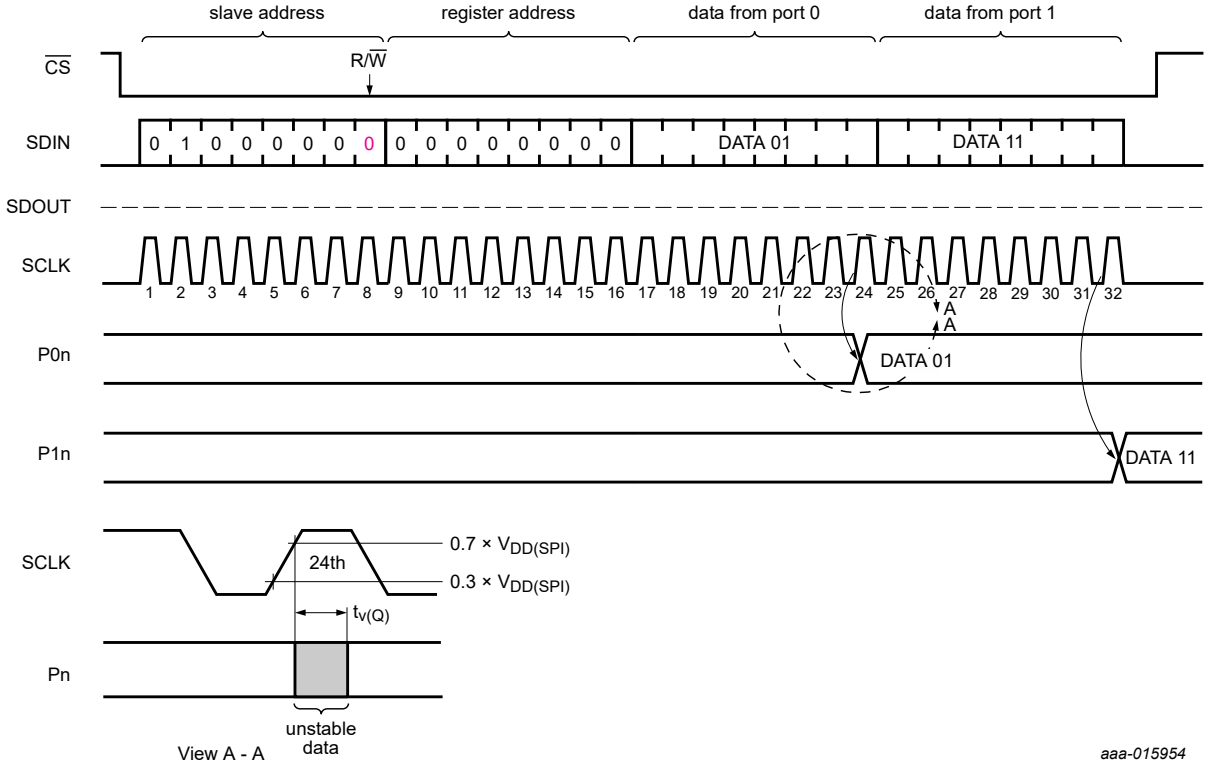
All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Zo = 50 Ω; tr/tf ≤ 30 ns.

All parameters and waveforms are not applicable to all devices. b. Voltage waveforms

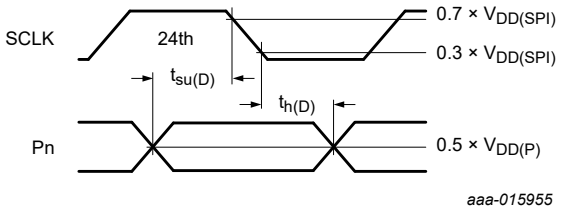
Figure 32. Interrupt load circuit and voltage waveforms



a. P port load configuration



b. Write mode (R/$\overline{W}$ = 0)



c. Read mode (R/$\overline{W}$ = 1)

C_L includes probe and jig capacitance.

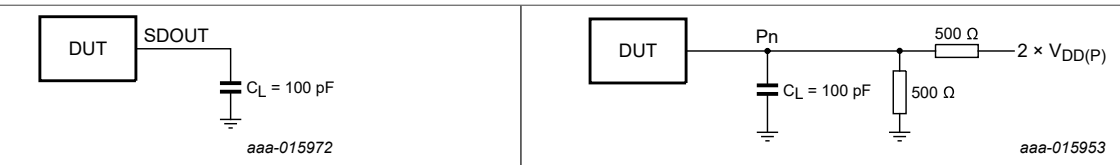
$t_{V(Q)}$ is measured from 0.7 x VDD(SPI) on SCLK to 50 % I/O (Pn) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

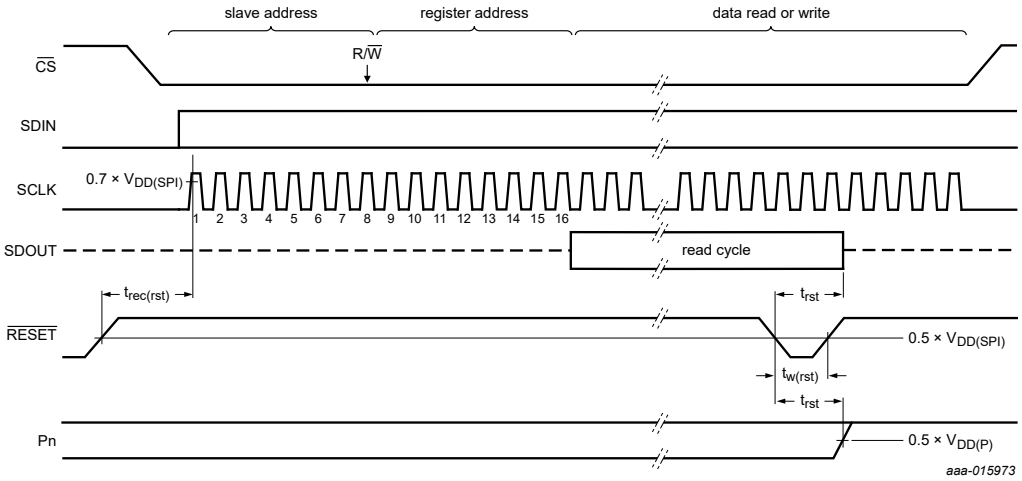
All parameters and waveforms are not applicable to all devices.

Figure 33. P port load circuit and voltage waveforms



a. SDOUT load configuration

b. P port load configuration



c. $\overline{RESET}$ timing

C_L includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r/t_f ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

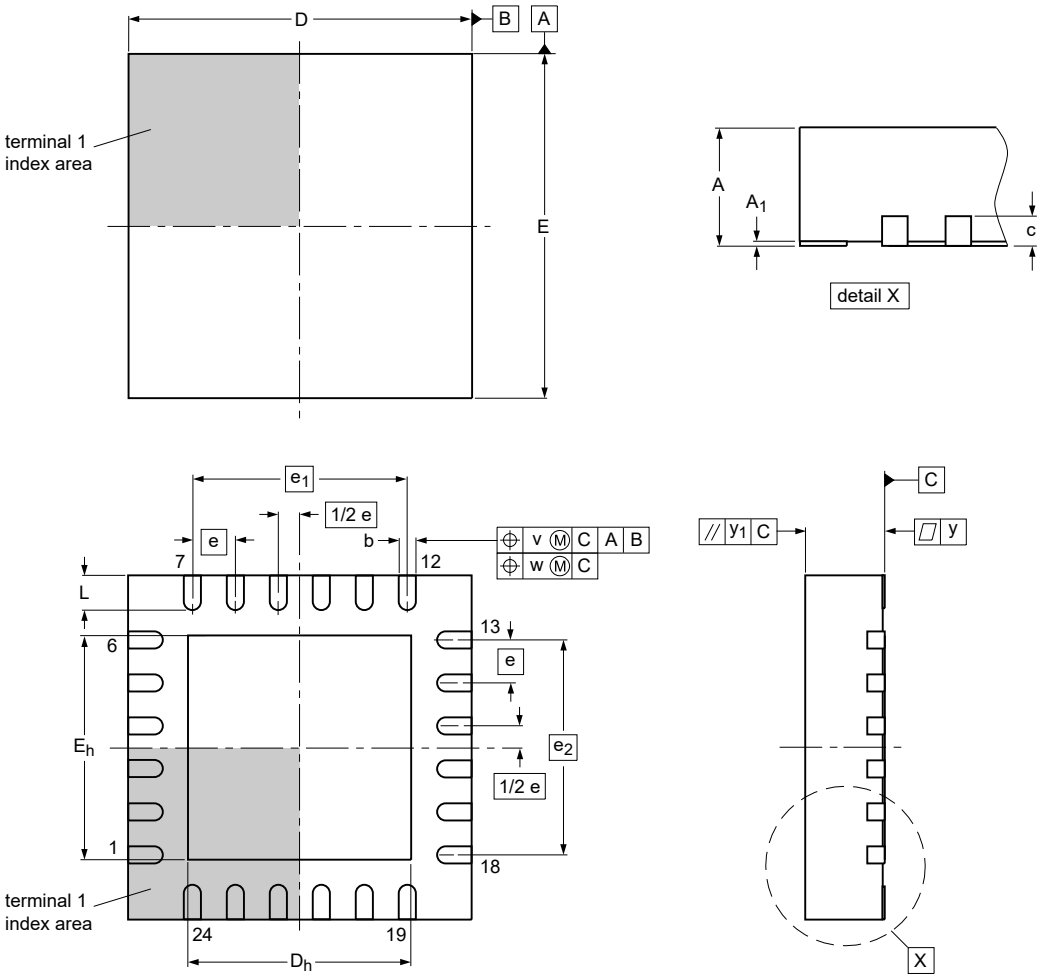
I/Os are configured as inputs.

All parameters and waveforms are not applicable to all devices.

Figure 34. Reset load circuits and voltage waveforms

14 Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm **SOT616-3**



Dimensions (mm are the original dimensions)

Unit(1)		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	max	1	0.05	0.30	0.2	4.1	2.75	4.1	2.75	0.5	2.5	2.5	0.5	0.1	0.05	0.05	0.1
	nom																
	min		0.00	0.18		3.9	2.45	3.9	2.45				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot616-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT616-3		MO-220				~~16-02-17~~ 16-07-14

Figure 35. Package outline SOT616-3 (HVQFN24)

15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 36) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 53 and Table 54

Table 53. SnPb eutectic process (from J-STD-020D)

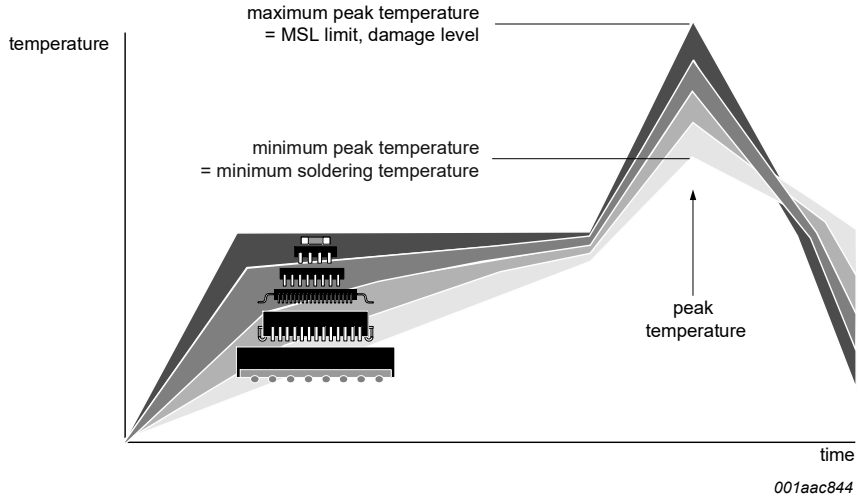
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 54. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 36.



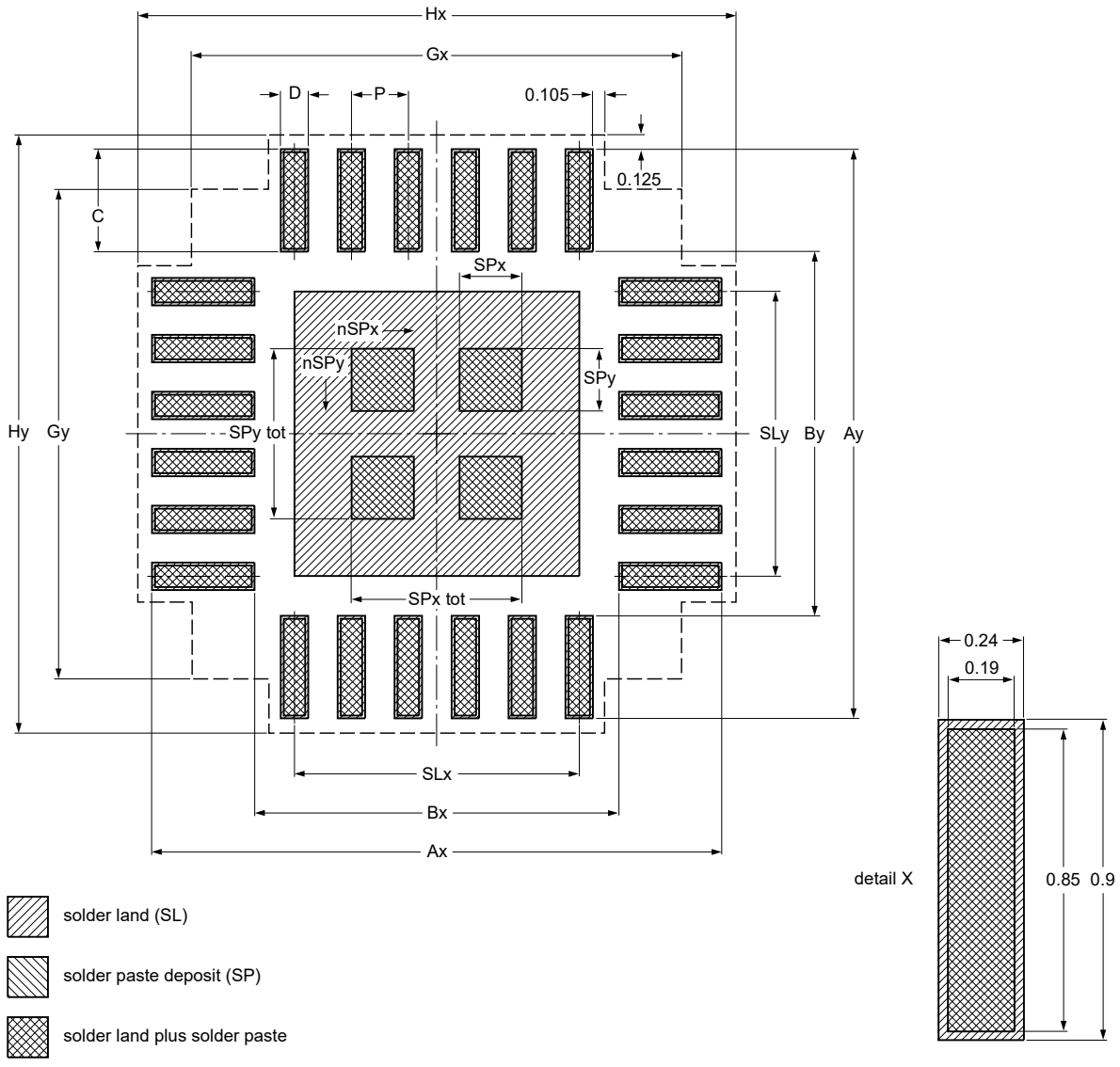
MSL: Moisture Sensitivity Level

Figure 36. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16 Soldering: PCB footprints

Footprint information for reflow soldering of HVQFN24 package **SOT616-3**



Hx	Hy
5.25	5.25

Dimensions in mm

P	Ax	Ay	Bx	By	SLx	SLy	SPx	SPy	SPx tot	SPy tot	C	D	nSPx	nSPy	Gx	Gy
0.50	5.00	5.00	3.20	3.20	2.50	2.50	0.55	0.55	1.50	1.50	0.90	0.24	2	2	4.30	4.30

Issue date ~~09-06-15~~ 14-06-12 *sot616-3_fr*

Figure 37. PCB footprint for SOT616-3 (HVQFN24); reflow soldering

17 Abbreviations

Table 55. Abbreviations

Symbol	Parameter
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
I^2C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
PCB	Printed-Circuit Board
POR	Power-On Reset
SMBus	System Management Bus
SPI	Serial Peripheral Interface

18 Revision history

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCAL9714 v.1.0	20230501	Product data sheet	-	-

19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

19.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

19.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com

Date of release: 1 May 2023
Document identifier: PCAL9714

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

PCAL9714HN/Q900MP PCAL9714HNMP