PCA9542A

2-channel I²C-bus multiplexer and interrupt logic

Rev. 5.1 — 15 July 2015 Product data sheet

1. General description

The PCA9542A is a 1-of-2 bidirectional translating multiplexer, controlled via the I²C-bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register. Two interrupt inputs, $\overline{INT0}$ and $\overline{INT1}$, one for each of the SCx/SDx downstream pairs, are provided. One interrupt output, $\overline{INT}$, which acts as an AND of the two interrupt inputs, is provided.

A power-on reset function puts the registers in their default state and initializes the I²C-bus state machine with no channels selected.

The pass gates of the multiplexer are constructed such that the V_{DD} pin can be used to limit the maximum high voltage which will be passed by the PCA9542A. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V, or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O pins are 5 V tolerant.

2. Features and benefits

- 1-of-2 bidirectional translating multiplexer
- I²C-bus interface logic; compatible with SMBus
- 2 active LOW interrupt inputs ($\overline{INT0}$, $\overline{INT1}$)
- Active LOW interrupt output ($\overline{INT}$)
- 3 address pins allowing up to 8 devices on the I²C-bus
- Channel selection via I²C-bus
- Powers up with all multiplexer channels deselected
- Low R_{on} switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO14, TSSOP14

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9542AD	PCA9542AD	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
PCA9542APW	PA9542A	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9542AD	PCA9542AD,112	SO14	Standard marking *IC's tube - DSC bulk pack	1140	T_{amb} = −40 °C to +85 °C
	PCA9542AD,118	SO14	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
PCA9542APW	PCA9542APW,112	TSSOP14	Standard marking *IC's tube - DSC bulk pack	2400	T_{amb} = −40 °C to +85 °C
	PCA9542APW,118	TSSOP14	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C

4. Block diagram

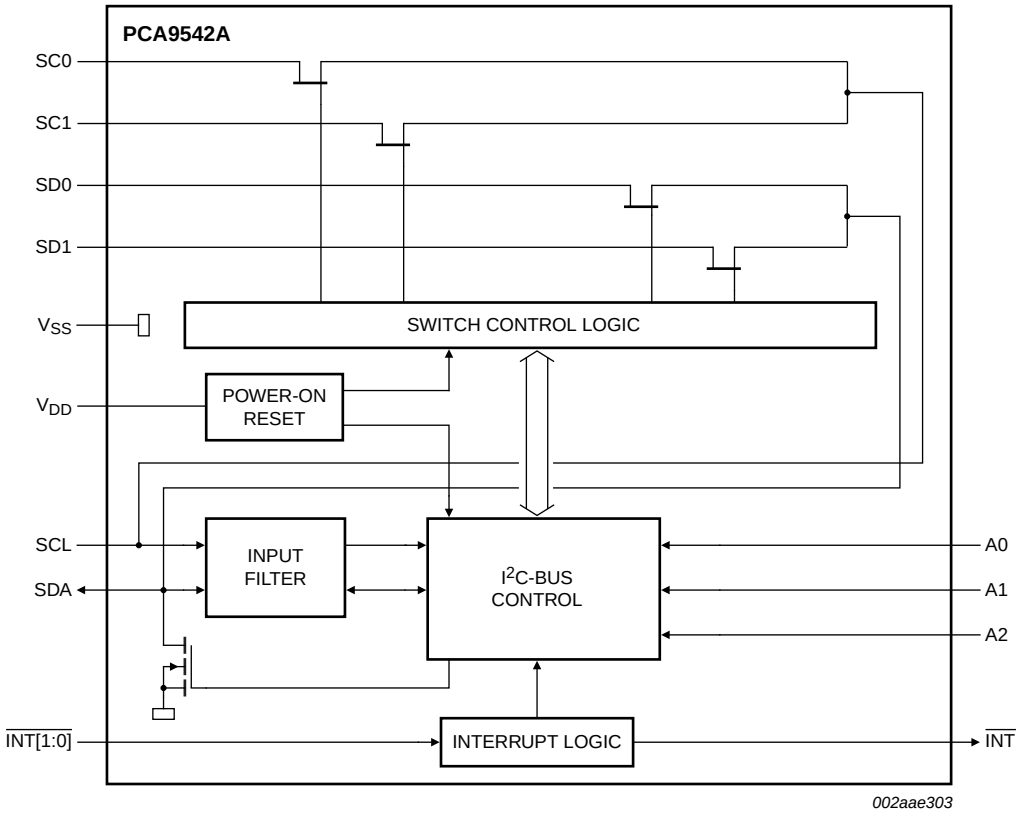


Fig 1. Block diagram of PCA9542A

5. Pinning information

5.1 Pinning

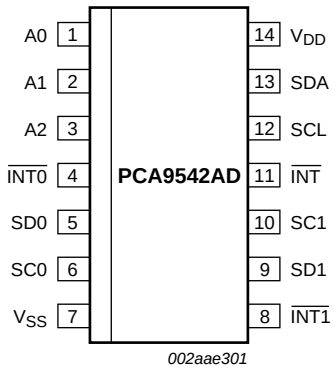


Fig 2. Pin configuration for SO14

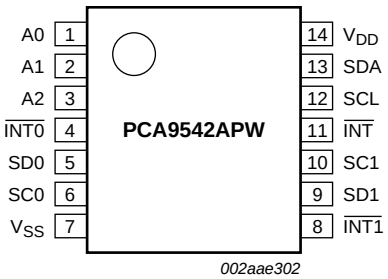


Fig 3. Pin configuration for TSSOP14

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2
$\overline{INT0}$	4	active LOW interrupt input 0
SD0	5	serial data 0
SC0	6	serial clock 0
V_{SS}	7	supply ground
$\overline{INT1}$	8	active LOW interrupt input 1
SD1	9	serial data 1
SC1	10	serial clock 1
$\overline{INT}$	11	active LOW interrupt output
SCL	12	serial clock line
SDA	13	serial data line
V_{DD}	14	supply voltage

6. Functional description

Refer to Figure 1 “Block diagram of PCA9542A”.

6.1 Device addressing

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9542A is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

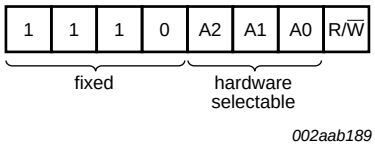


Fig 4. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

6.2 Control register

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9542A which will be stored in the control register. If multiple bytes are received by the PCA9542A, it will save the last byte received. This register can be written and read via the I²C-bus.

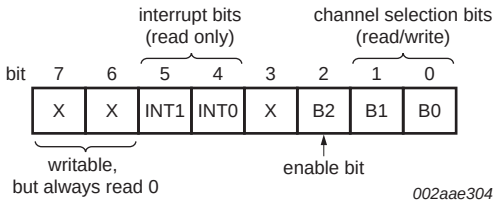


Fig 5. Control register

6.2.1 Control register definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the control register. This register is written after the PCA9542A has been addressed. The 3 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, it will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCx/SDx lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

Bits INT0, INT1, D6 and D7 are all writable, but will read the chip status. INT0 and INT1 indicate the state of the corresponding interrupt input. D7 and D6 always read 0.
See Section 6.3.

Table 4. Control register: Write—channel selection; Read—channel status

D7	D6	INT1	INT0	D3	B2	B1	B0	Command
X	X	X	X	X	0	X	X	no channel selected
X	X	X	X	X	1	0	0	channel 0 enabled
X	X	X	X	X	1	0	1	channel 1 enabled
X	X	X	X	X	1	1	X	no channel selected
0	0	0	0	0	0	0	0	no channel selected; power-up default state

6.3 Interrupt handling

The PCA9542A provides 2 interrupt inputs, one for each channel and one open-drain interrupt output. When an interrupt is generated by any device, it will be detected by the PCA9542A and the interrupt output will be driven LOW. The channel need not be active for detection of the interrupt. A bit is also set in the control byte.

Bits 5:4 of the control byte correspond to channel 1, channel 0 of the PCA9542A, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the PCA9542A and read the contents of the control byte to determine which channel contains the device generating the interrupt. The master can then reconfigure the PCA9542A to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can be providing an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{DD} through a pull-up resistor.

Table 5. Control register read — interrupt

D7	D6	INT1	INT0	D3	B2	B1	B0	Command
0	0	X	0	X	X	X	X	no interrupt on channel 0
			1					interrupt on channel 0
0	0	0	X	X	X	X	X	no interrupt on channel 1
		1						interrupt on channel 1

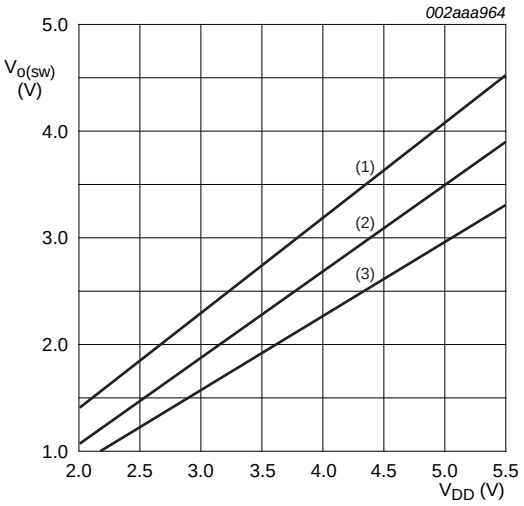
Remark: The two interrupts can be active at the same time. D6 and D7 always read 0.

6.4 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9542A in a reset condition until V_{DD} has reached V_{POR}. At this point, the reset condition is released and the PCA9542A registers and I²C-bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter, V_{DD} must be lowered below 0.2 V for at least 5 μs in order to reset the device.

6.5 Voltage translation

The pass gate transistors of the PCA9542A are constructed such that the V_{DD} voltage can be used to limit the maximum voltage that will be passed from one I²C-bus to another.



(1) maximum
(2) typical
(3) minimum

Fig 6. Pass gate voltage versus supply voltage

Figure 6 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section 12 “Dynamic characteristics” of this data sheet). In order for the PCA9542A to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{o(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. Looking at Figure 6, we see that $V_{o(sw)(max)}$ will be at 2.7 V when the PCA9542A supply voltage is 3.5 V or lower so the PCA9542A supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 13).

More Information can be found in Application Note *AN262, PCA954X family of I²C/SMBus multiplexers and switches*.

7. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 7).

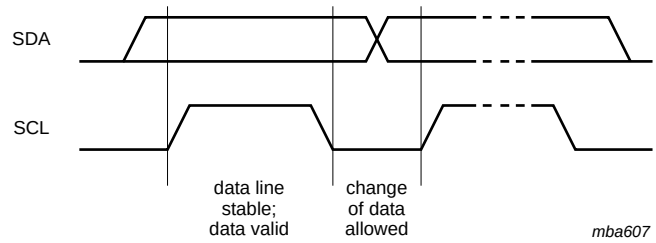


Fig 7. Bit transfer

7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 8).

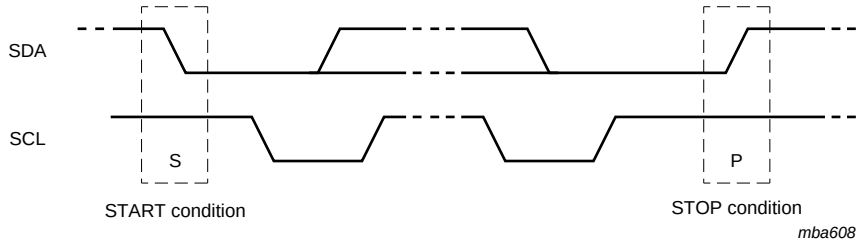


Fig 8. Definition of START and STOP conditions

7.3 System configuration

A device generating a message is a ‘transmitter’, a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 9).

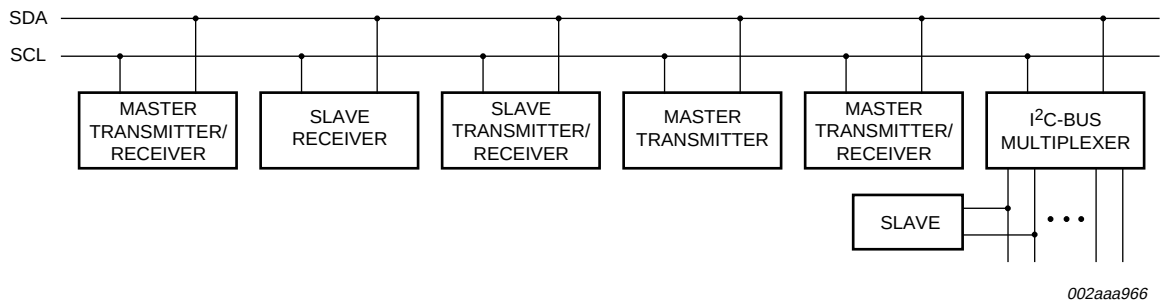


Fig 9. System configuration

7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

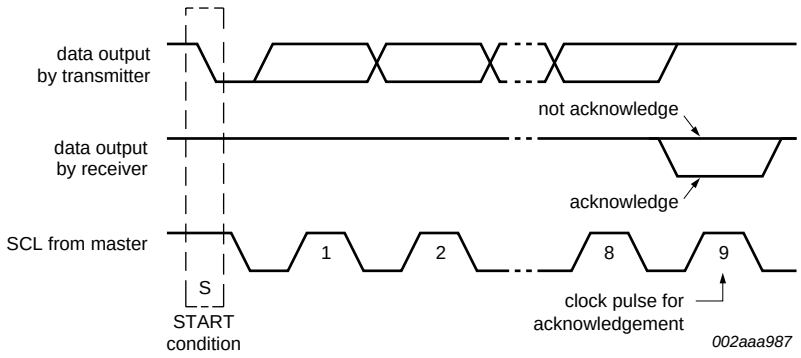


Fig 10. Acknowledgement on the I²C-bus

7.5 Bus transactions

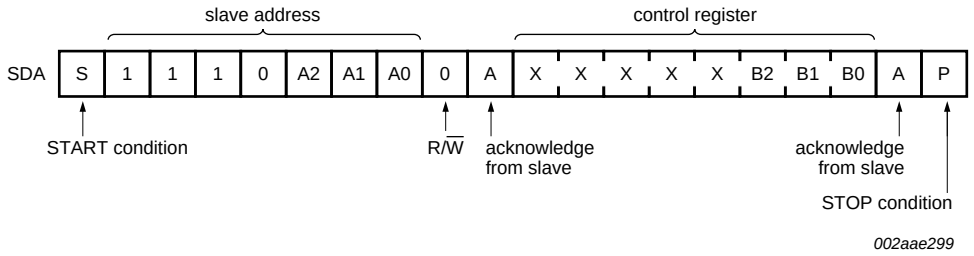


Fig 11. Write control register

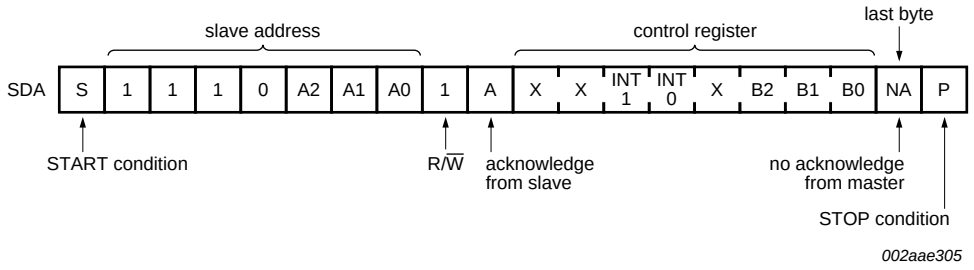
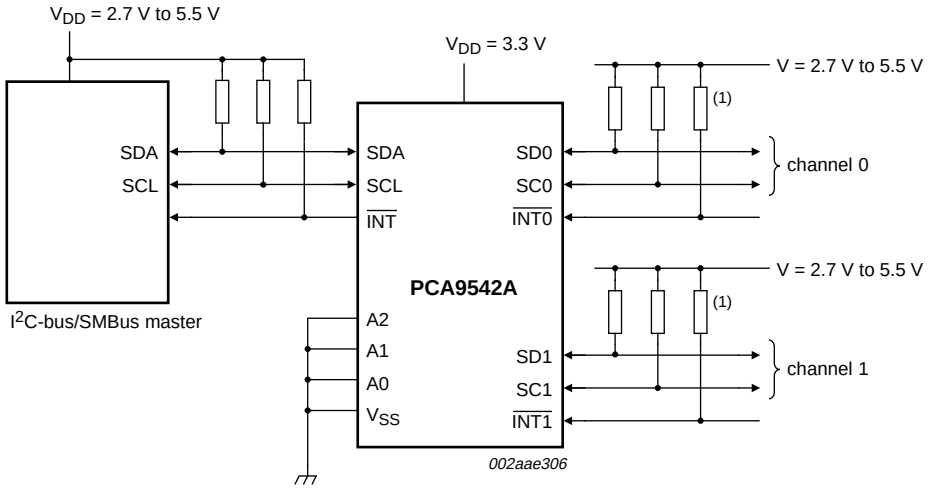


Fig 12. Read control register

8. Application design-in information



(1) If the device generating the interrupt has an open-drain output structure or can be 3-stated, a pull-up resistor is required.

If the device generating the interrupt has a totem pole output structure and cannot be 3-stated, a pull-up resistor is not required.

The interrupt inputs should not be left floating.

Fig 13. Typical application

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to ground (V_{SS} = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+7.0	V
V_I	input voltage		−0.5	+7.0	V
I_I	input current		-	±20	mA
I_O	output current		-	±25	mA
I_{DD}	supply current		-	±100	mA
I_{SS}	ground supply current		-	±100	mA
P_{tot}	total power dissipation		-	400	mW
$T_{j(max)}$	maximum junction temperature	[1]	-	125	°C
T_{stg}	storage temperature		−60	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

10. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO14 package	127	°C/W
		TSSOP14 package	175	°C/W

11. Static characteristics

Table 8. Static characteristics at V_{DD} = 2.3 V to 3.6 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. See Table 9 for V_{DD} = 4.5 V to 5.5 V.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		2.3	-	3.6	V
I_{DD}	supply current	operating mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	-	10	30	μA
I_{stb}	standby current	standby mode; V_{DD} = 3.6 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz	-	0.1	1	μA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS} [2]	-	1.6	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	7	-	mA
		V_{OL} = 0.6 V	6	10	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}	−1	-	+1	μA
C_i	input capacitance	V_I = V_{SS}	-	9	10	pF
Select inputs A0, A1, A2, $\overline{INT0}$, $\overline{INT1}$						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	6	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	-	+1	μA
C_i	input capacitance	V_I = V_{SS}	-	1.6	3	pF
Pass gate						
R_{on}	ON-state resistance	V_{DD} = 3.0 V to 3.6 V; V_O = 0.4 V; I_O = 15 mA	5	11	30	Ω
		V_{DD} = 2.3 V to 2.7 V; V_O = 0.4 V; I_O = 10 mA	7	16	55	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)}$ = V_{DD} = 3.3 V; $I_{o(sw)}$ = −100 μA	-	1.9	-	V
		$V_{i(sw)}$ = V_{DD} = 3.0 V to 3.6 V; $I_{o(sw)}$ = −100 μA	1.6	-	2.8	V
		$V_{i(sw)}$ = V_{DD} = 2.5 V; $I_{o(sw)}$ = −100 μA	-	1.5	-	V
		$V_{i(sw)}$ = V_{DD} = 2.3 V to 2.7 V; $I_{o(sw)}$ = −100 μA	1.1	-	2.0	V
I_L	leakage current	V_I = V_{DD} or V_{SS}	−1	-	+1	μA
C_{io}	input/output capacitance	V_I = V_{SS}	-	3	5	pF
$\overline{INT}$ output						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
I_{OH}	HIGH-level output current		-	-	+10	μA

[1] For operation between published voltage ranges, refer to worst case parameter in both ranges.

[2] V_{DD} must be lowered to 0.2 V for at least 5 μs in order to reset part.

Table 9. Static characteristics at V_{DD} = 4.5 V to 5.5 V

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified. See Table 8 for V_{DD} = 2.3 V to 3.6 V.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		4.5	-	5.5	V
I_{DD}	supply current	operating mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 100 kHz	-	25	100	μA
I_{stb}	standby current	standby mode; V_{DD} = 5.5 V; no load; V_I = V_{DD} or V_{SS}; f_{SCL} = 0 kHz	-	0.3	1	μA
V_{POR}	power-on reset voltage	no load; V_I = V_{DD} or V_{SS} [2]	-	1.7	2.1	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	6	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
		V_{OL} = 0.6 V	6	-	-	mA
I_L	leakage current	V_I = V_{DD} or V_{SS}	−1	-	+1	μA
C_i	input capacitance	V_I = V_{SS}	-	9	10	pF
Select inputs A0, A1, A2, $\overline{INT0}$, $\overline{INT1}$						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	6	V
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	-	+1	μA
C_i	input capacitance	V_I = V_{SS}	-	2	5	pF
Pass gate						
R_{on}	ON-state resistance	V_{DD} = 4.5 V to 5.5 V; V_O = 0.4 V; I_O = 15 mA	4	9	24	Ω
$V_{o(sw)}$	switch output voltage	$V_{i(sw)}$ = V_{DD} = 5.0 V; $I_{o(sw)}$ = −100 μA	-	3.6	-	V
		$V_{i(sw)}$ = V_{DD} = 4.5 V to 5.5 V; $I_{o(sw)}$ = −100 μA	2.6	-	4.5	V
I_L	leakage current	V_I = V_{DD} or V_{SS}	−1	-	+1	μA
C_{io}	input/output capacitance	V_I = V_{SS}	-	3	5	pF
$\overline{INT}$ output						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	3	-	-	mA
I_{OH}	HIGH-level output current		-	-	+10	μA

[1] For operation between published voltage ranges, refer to worst case parameter in both ranges.

[2] V_{DD} must be lowered to 0.2 V for at least 5 μs in order to reset part.

12. Dynamic characteristics

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Unit
			Min	Max	Min	Max	
t_{PD}	propagation delay	from SDA to SDx, or SCL to SCx	-	0.3[1]	-	0.3[1]	ns
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs
$t_{HD;STA}$	hold time (repeated) START condition	[2]	4.0	-	0.6	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	µs
$t_{HD;DAT}$	data hold time		0[3]	3.45	0[3]	0.9	µs
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$[4]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$[4]	300	ns
C_b	capacitive load for each bus line		-	400	-	400	pF
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
$t_{VD;DAT}$	data valid time	HIGH-to-LOW [5]	-	1	-	1	µs
		LOW-to-HIGH [5]	-	0.6	-	0.6	µs
$t_{VD;ACK}$	data valid acknowledge time		-	1	-	1	µs
$\overline{INT}$							
$t_{v(INTnN-INTN)}$	valid time from $\overline{INTn}$ to $\overline{INT}$ signal	[5]	-	4	-	4	µs
$t_{d(INTnN-INTN)}$	delay time from $\overline{INTn}$ to $\overline{INT}$ inactive	[5]	-	2	-	2	µs
$t_{w(rej)L}$	LOW-level rejection time	$\overline{INTn}$ inputs [5]	1	-	1	-	µs
$t_{w(rej)H}$	HIGH-level rejection time	$\overline{INTn}$ inputs [5]	0.5	-	0.5	-	µs

[1] Pass gate propagation delay is calculated from the 20 Ω typical R_{on} and the 15 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] C_b = total capacitance of one bus line in pF.

[5] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

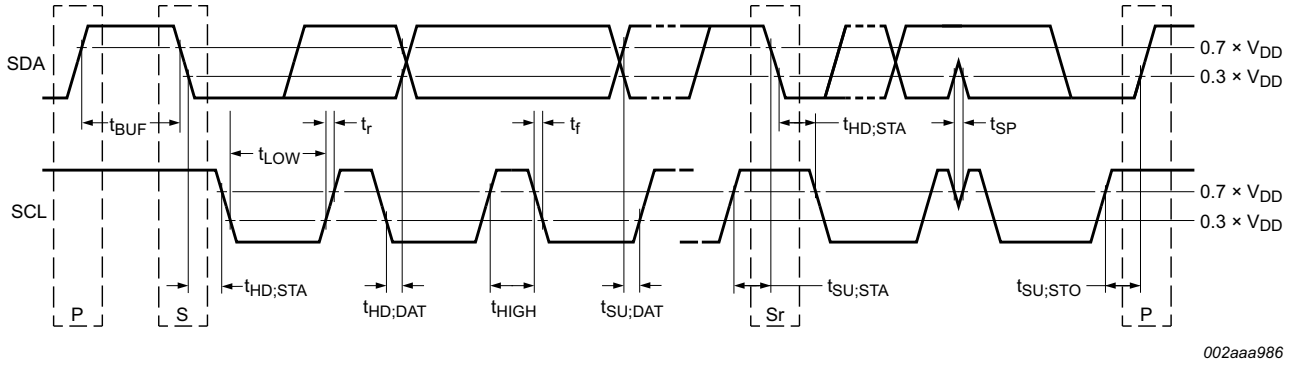
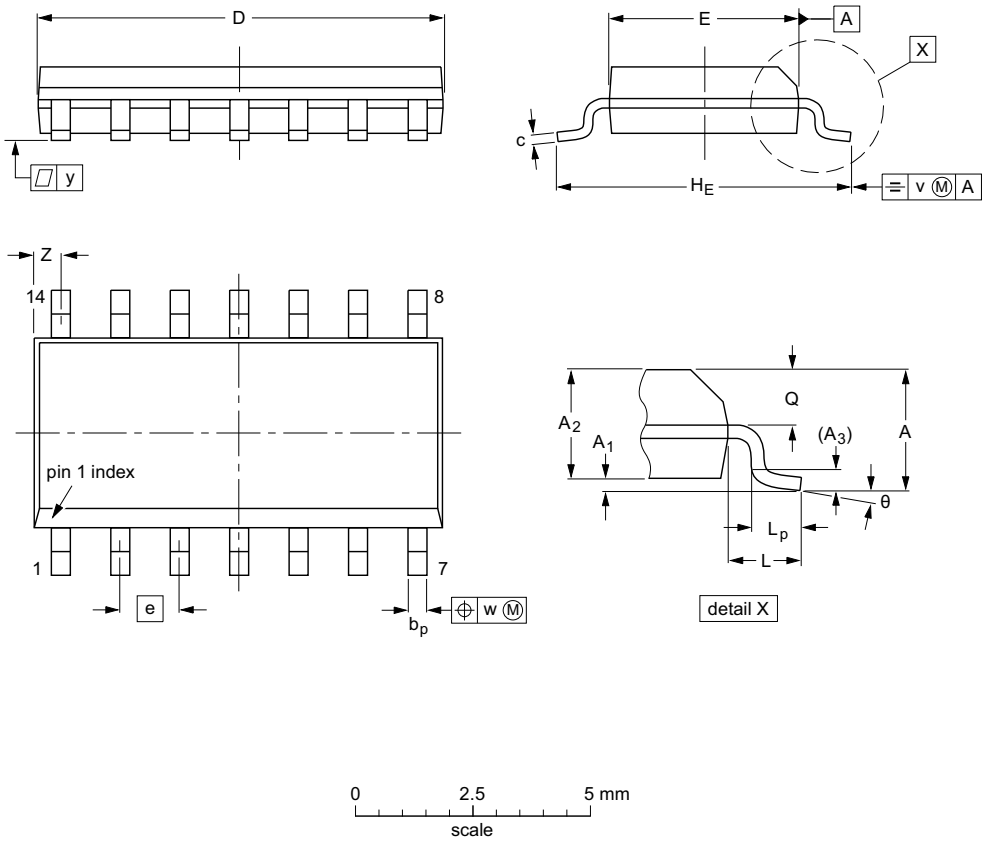


Fig 14. Definition of timing on the I²C-bus

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

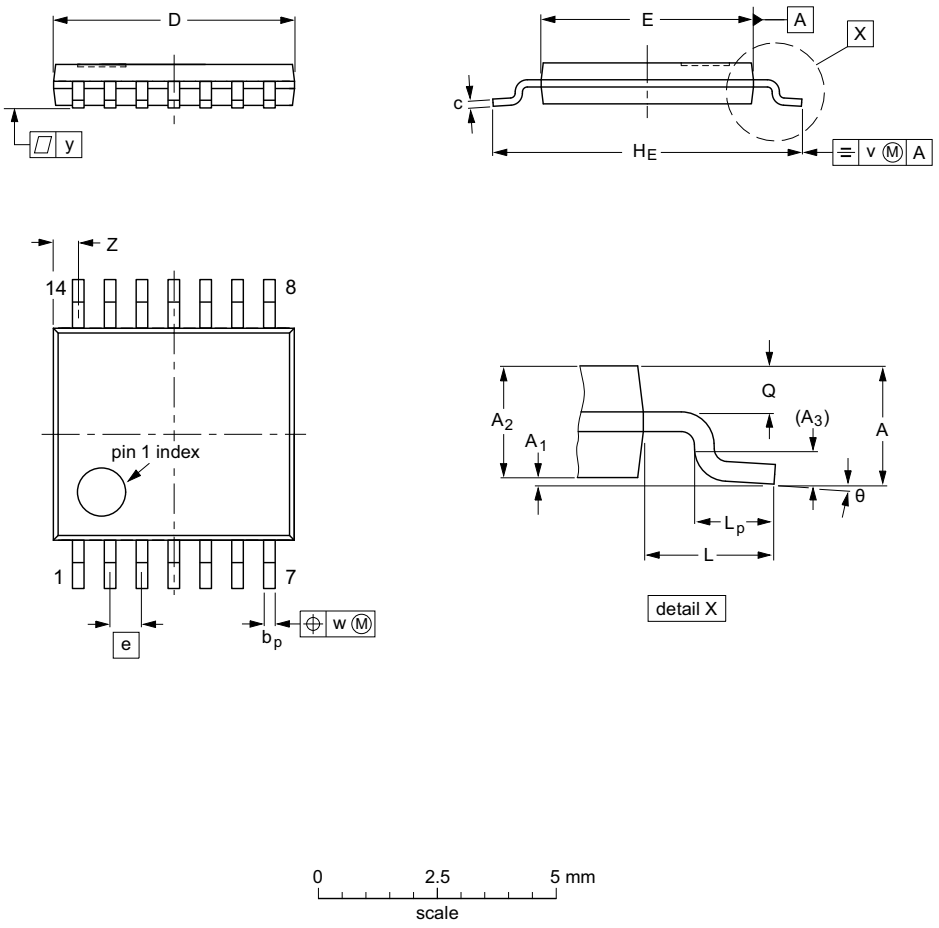
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT402-1 (TSSOP14)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020D)

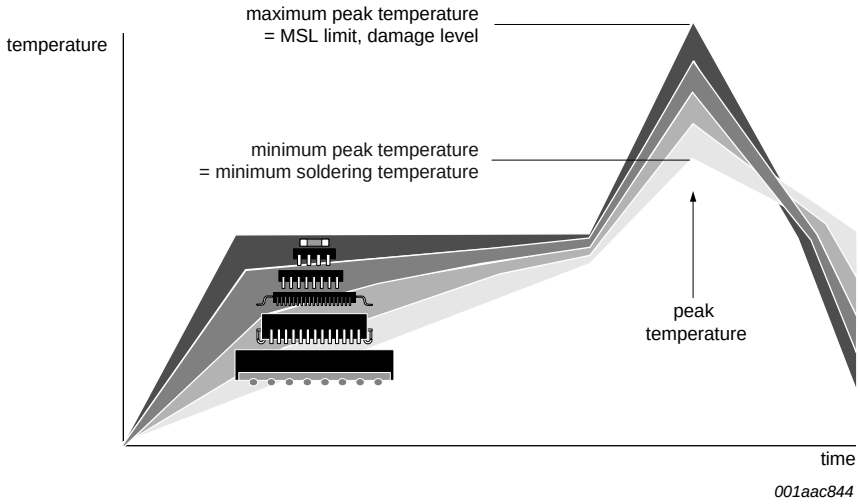
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.



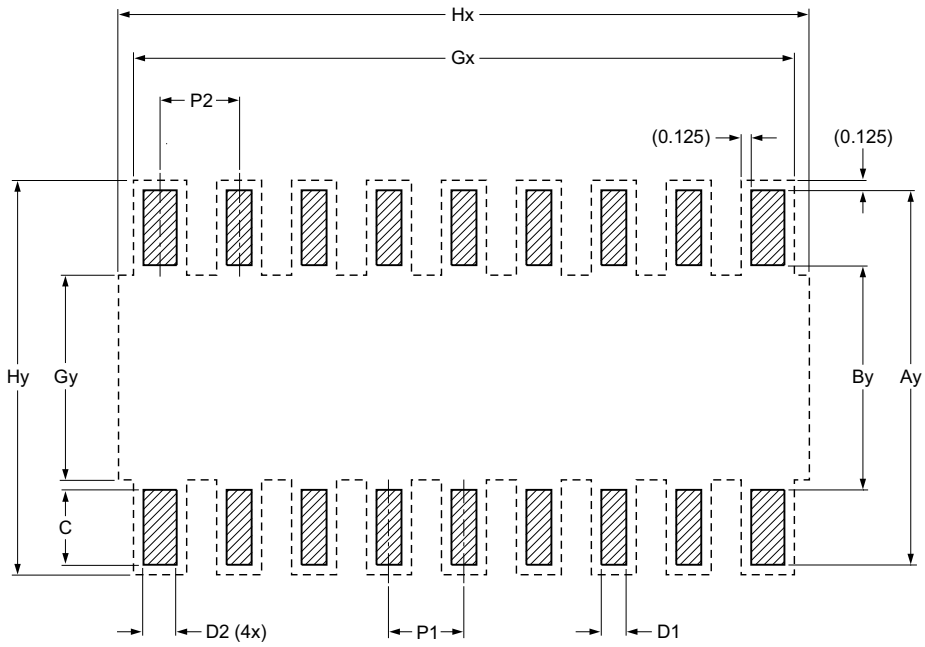
MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

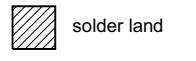
15. Soldering: PCB footprints

Footprint information for reflow soldering of SO14 package **SOT108-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout



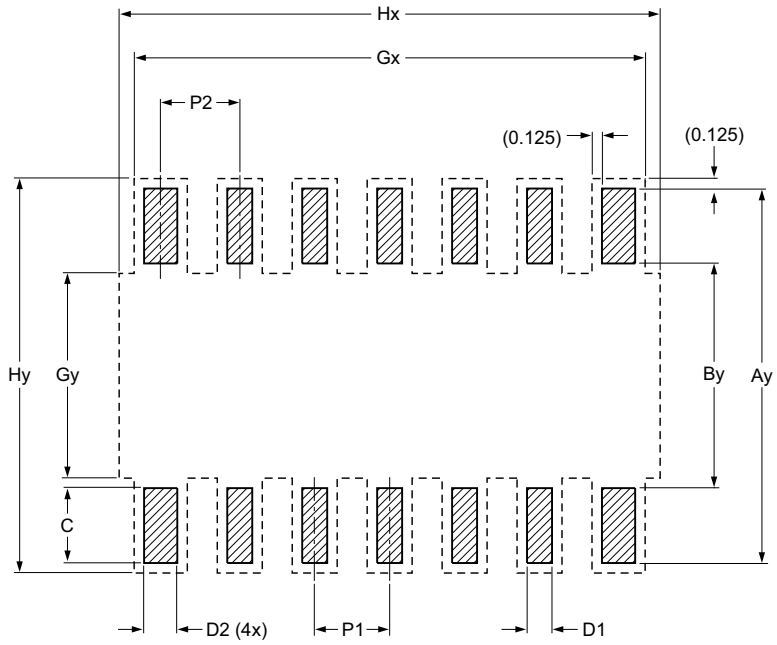
DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
1.270	1.320	7.400	3.900	1.750	0.700	0.800	8.770	5.200	11.900	7.650

sot108-1_fr

Fig 18. PCB footprint for SOT108-1 (SO14); reflow soldering

Footprint information for reflow soldering of TSSOP14 package **SOT402-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	4.950	5.300	5.800	7.450

sot402-1_fr

Fig 19. PCB footprint for SOT402-1 (TSSOP14); reflow soldering

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged-Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
LSB	Least Significant Bit
POR	Power-On Reset
SMBus	System Management Bus

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9542A v.5.1	20150715	Product data sheet	-	PCA9542A v.5
Modifications:	• Table 14 “Revision history”, corrected phrase “for at least 5 ms” to “for at least 5 μs” for Table 8 and Table 9 modifications			
PCA9542A v.5	20140407	Product data sheet	-	PCA9542A v.4
Modifications:	• Section 2 “Features and benefits”, 16th bullet item: deleted phrase “200 V MM per JESD22-A115” • Table 1 “Ordering information”: added column “Topside marking” (moved from Table 2) • Table 2 “Ordering options”: – deleted column “Topside mark” (moved to Table 1) – added columns “Orderable part number”, “Package”, “Packing method”, and “Minimum order quantity” • Figure 5 “Control register” updated: added notation ‘writable, but always read 0’ • Section 6.2.1 “Control register definition”: added second paragraph • Section 6.3 “Interrupt handling”, “Remark” paragraph (following Table 5): added second sentence • Section 6.4 “Power-on reset”: first paragraph, third sentence: corrected from “V_{DD} must be lowered below 0.2 V to reset the device” to “V_{DD} must be lowered below 0.2 V for at least 5 μs in order to reset the device” • Table 6 “Limiting values”: added limiting values for “$T_{j(max)}$” • Added Section 10 “Thermal characteristics” • Table 8 “Static characteristics at V_{DD} = 2.3 V to 3.6 V”, – Table note [2]: inserted phrase “for at least 5 μs” – sub-section “Select inputs A0, A1, A2, $\overline{INT0}$, $\overline{INT1}$”: Max value for V_{IH} corrected from “V_{DD} + 0.5 V” to “6 V” • Table 9 “Static characteristics at V_{DD} = 4.5 V to 5.5 V”, – Table note [2]: inserted phrase “for at least 5 μs” – sub-section “Select inputs A0, A1, A2, $\overline{INT0}$, $\overline{INT1}$”: Max value for V_{IH} corrected from “V_{DD} + 0.5 V” to “6 V” • Added Section 15 “Soldering: PCB footprints”			
PCA9542A v.4	20090615	Product data sheet	-	PCA9542A v.3
PCA9542A v.3	20081124	Product data sheet	-	PCA9542A v.2
PCA9542A v.2 (9397 750 13955)	20040929	Product data sheet	-	PCA9542A v.1
PCA9542A v.1 (9397 750 13307)	20040727	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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