



# PCA9540B

## 2-channel I<sup>2</sup>C-bus multiplexer

Rev. 7.1 — 19 January 2018

Product data sheet

## 1. General description

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The PCA9540B is a 1-of-2 bidirectional translating multiplexer, controlled via the I<sup>2</sup>C-bus. The SCL/SDA upstream pair fans out to two SCx/SDx downstream pairs, or channels. Only one SCx/SDx channel is selected at a time, determined by the contents of the programmable control register.

A power-on reset function puts the registers in their default state and initializes the I<sup>2</sup>C-bus state machine with no channels selected.

The pass gates of the multiplexer are constructed such that the V<sub>DD</sub> pin can be used to limit the maximum high voltage that is passed by the PCA9540B. This allows the use of different bus voltages on each SCx/SDx pair, so that 1.8 V, 2.5 V or 3.3 V parts can communicate with 5 V parts without any additional protection. External pull-up resistors can pull the bus up to the desired voltage level for this channel. All I/O pins are 5 V tolerant.

## 2. Features and benefits

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- 1-of-2 bidirectional translating multiplexer
- I<sup>2</sup>C-bus interface logic; compatible with SMBus standards
- Channel selection via I<sup>2</sup>C-bus
- Power-up with all multiplexer channels deselected
- Low R<sub>on</sub> switches
- Allows voltage level translation between 1.8 V, 2.5 V, 3.3 V and 5 V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8, XSON8



### 3. Ordering information

Table 1. Ordering information

| Type number     | Topside marking | Package |  |          |
|-----------------|-----------------|---------|--|----------|
|                 |                 | Name    | Description  | Version  |
| PCA9540BD       | PA9540B         | SO8     | plastic small outline package; 8 leads; body width 3.9 mm                                | SOT96-1  |
| PCA9540BDP      | 9540B           | TSSOP8  | plastic thin shrink small outline package; 8 leads; body width 3 mm                      | SOT505-1 |
| PCA9540BDP/Q900 | 9540B           | TSSOP8  | plastic thin shrink small outline package; 8 leads; body width 3 mm                      | SOT505-1 |
| PCA9540BGD      | 40B             | XSON8   | plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm | SOT996-2 |

[1] PCA9540BDP/Q900 is AEC-Q100 compliant. Contact your NXP account team, distribution partner or [i2c.support@nxp.com](mailto:i2c.support@nxp.com) for PPAP.

#### 3.1 Ordering options

Table 2. Ordering options

| Type number     | Orderable part number | Package | Packing method                       | Minimum order quantity | Temperature range                    |
|-----------------|-----------------------|---------|--------------------------------------|------------------------|--------------------------------------|
| PCA9540BD       | PCA9540BD,118         | SO8     | Reel 13" Q1/T1<br>*Standard mark SMD | 2500                   | T <sub>amb</sub> = -40 °C to +85 °C  |
| PCA9540BDP      | PCA9540BDP,118        | TSSOP8  | Reel 13" Q1/T1<br>*Standard mark SMD | 2500                   | T <sub>amb</sub> = -40 °C to +85 °C  |
| PCA9540BDP/Q900 | PCA9540BDP/Q900,118   | TSSOP8  | Reel 13" Q1/T1<br>*Standard mark SMD | 2500                   | T <sub>amb</sub> = -40 °C to +105 °C |
| PCA9540BGD      | PCA9540BGD,125        | XSON8   | Reel 7" Q3/T4<br>*Standard mark      | 3000                   | T <sub>amb</sub> = -40 °C to +85 °C  |

4. Block diagram

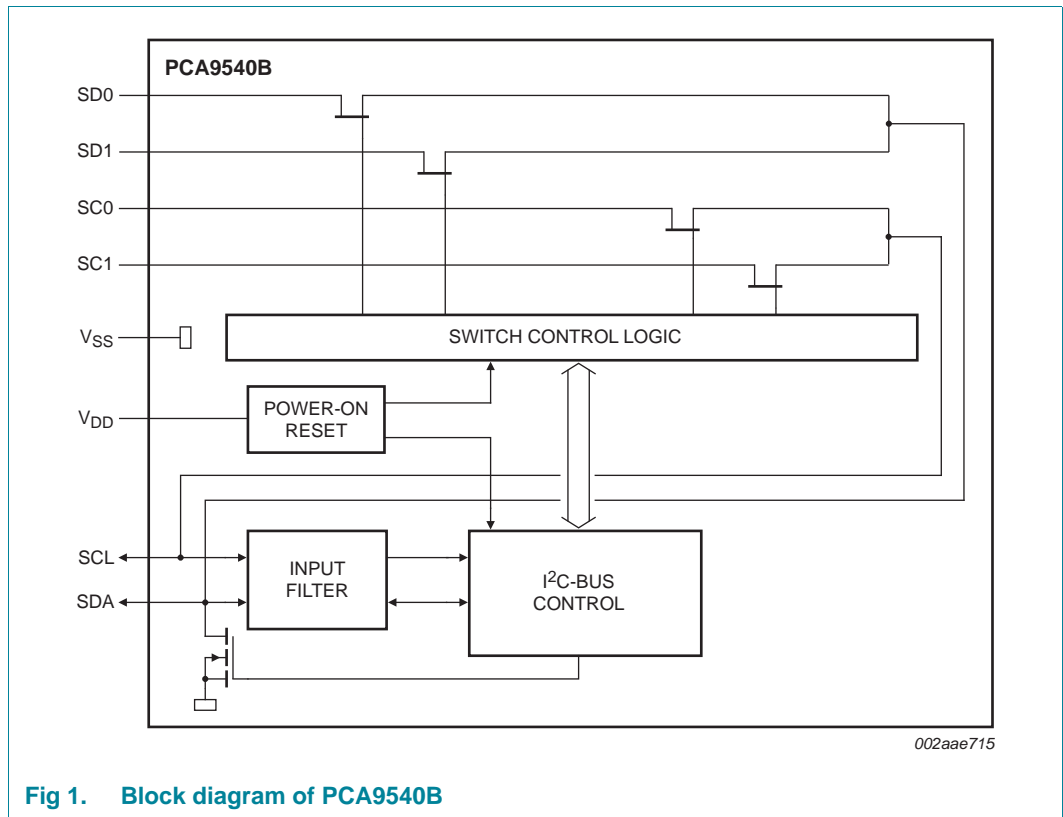


Fig 1. Block diagram of PCA9540B

## 5. Pinning information

### 5.1 Pinning

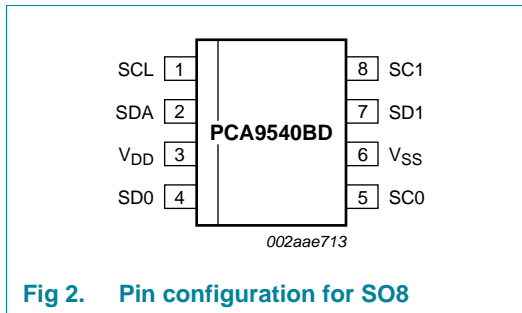


Fig 2. Pin configuration for SO8

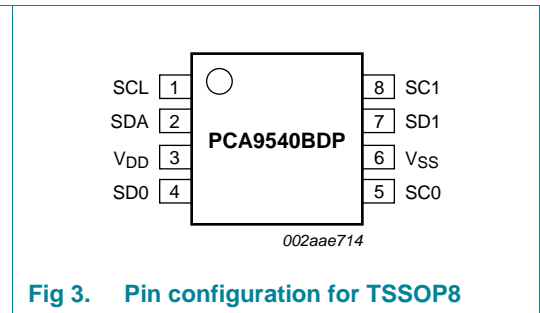


Fig 3. Pin configuration for TSSOP8

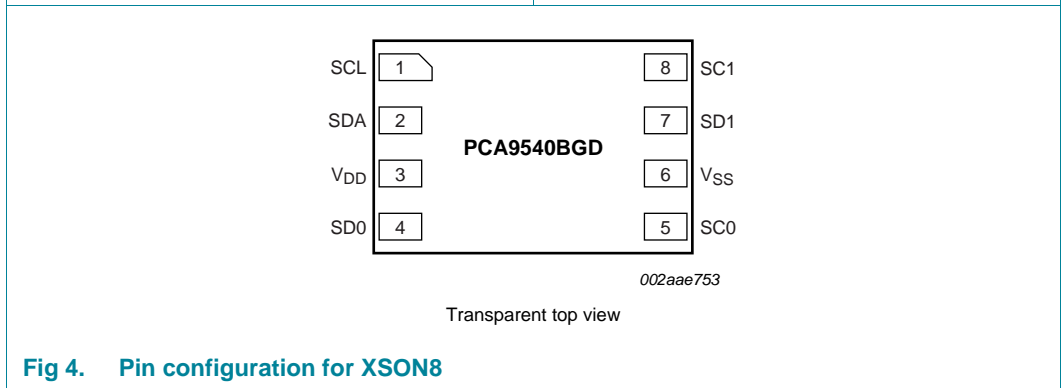


Fig 4. Pin configuration for XSON8

### 5.2 Pin description

Table 3. Pin description

| Symbol          | Pin | Description       |
|-----------------|-----|-------------------|
| SCL             | 1   | serial clock line |
| SDA             | 2   | serial data line  |
| V <sub>DD</sub> | 3   | supply voltage    |
| SD0             | 4   | serial data 0     |
| SC0             | 5   | serial clock 0    |
| V <sub>SS</sub> | 6   | supply ground     |
| SD1             | 7   | serial data 1     |
| SC1             | 8   | serial clock 1    |

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9540B”](#).

### 6.1 Device addressing

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9540B is shown in [Figure 5](#).

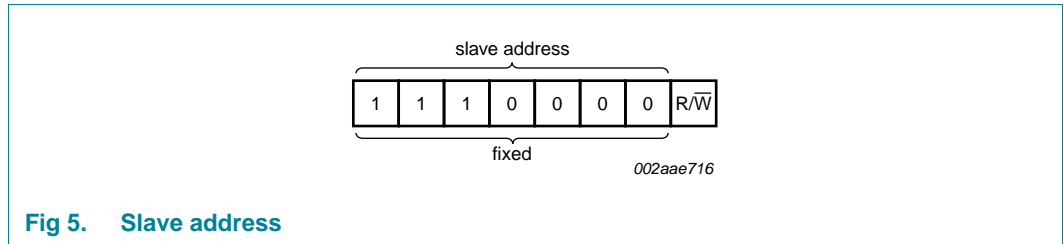


Fig 5. Slave address

The last bit of the slave address defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

### 6.2 Control register

Following the successful acknowledgement of the slave address, the bus master sends a byte to the PCA9540B which is stored in the Control register. If multiple bytes are received by the PCA9540B, it saves the last byte received. This register can be written and read via the I<sup>2</sup>C-bus.

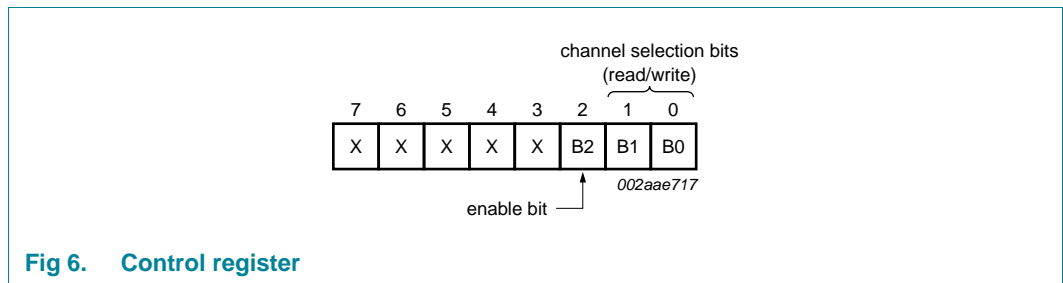


Fig 6. Control register

#### 6.2.1 Control register definition

A SCx/SDx downstream pair, or channel, is selected by the contents of the Control register. This register is written after the PCA9540B has been addressed. The 2 LSBs of the control byte are used to determine which channel is to be selected. When a channel is selected, it will become active after a STOP condition has been placed on the I<sup>2</sup>C-bus. This ensures that all SCx/SDx lines are in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

**Table 4. Control register: Write — channel selection; Read — channel status**

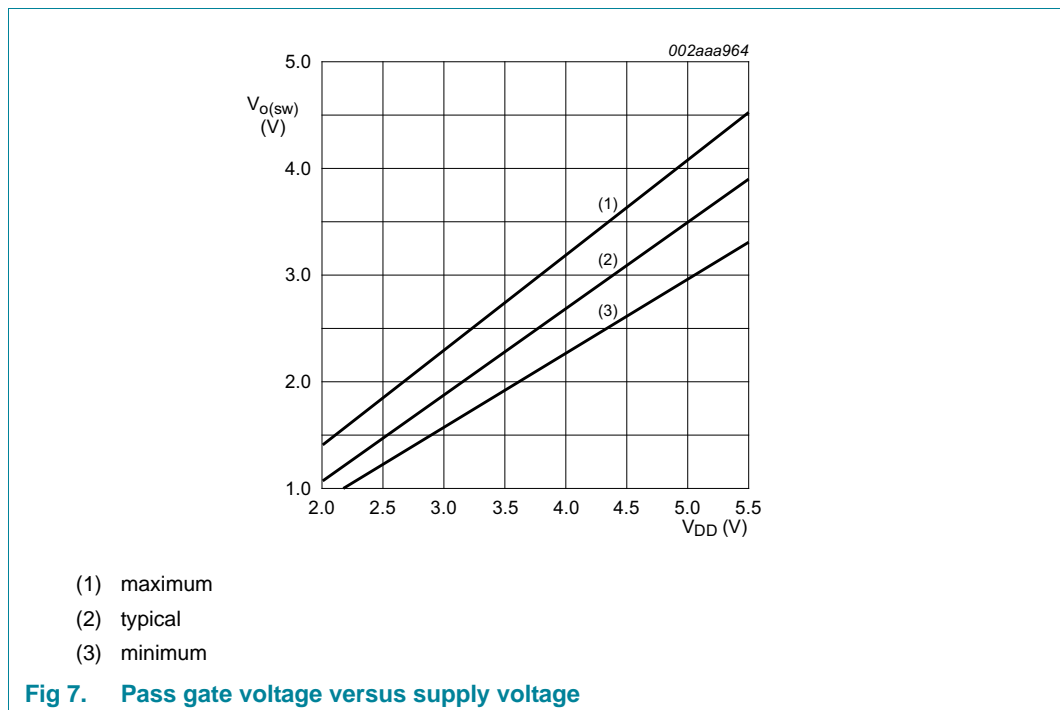
| D7 | D6 | D5 | D4 | D3 | B2 | B1 | B0 | Command  |
|----|----|----|----|----|----|----|----|--|
| X  | X  | X  | X  | X  | 0  | X  | X  | no channel selected                            |
| X  | X  | X  | X  | X  | 1  | 0  | 0  | channel 0 enabled                              |
| X  | X  | X  | X  | X  | 1  | 0  | 1  | channel 1 enabled                              |
| X  | X  | X  | X  | X  | 1  | 1  | X  | no channel selected                            |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | no channel selected;<br>power-up default state |

### 6.3 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9540B in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At this point, the reset condition is released and the PCA9540B registers and I<sup>2</sup>C-bus state machine are initialized to their default states (all zeroes), causing all the channels to be deselected. Thereafter,  $V_{DD}$  must be lowered below 0.2 V for at least 5  $\mu$ s in order to reset the device.

### 6.4 Voltage translation

The pass gate transistors of the PCA9540B are constructed such that the  $V_{DD}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C-bus to another.



**Figure 7** shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in [Section 11 “Static characteristics”](#) of this data sheet). In order for the PCA9540B to act as a voltage translator, the  $V_{o(sw)}$  voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then  $V_{o(sw)}$  should be equal to or below 2.7 V to clamp the downstream bus voltages effectively. Looking at

Figure 7, we see that  $V_{o(sw)(max)}$  is at 2.7 V when the PCA9540B supply voltage is 3.5 V or lower so the PCA9540B supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 14).

More Information can be found in application note AN262, "PCA954X family of I<sup>2</sup>C/SMBus multiplexers and switches".

## 7. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 8).

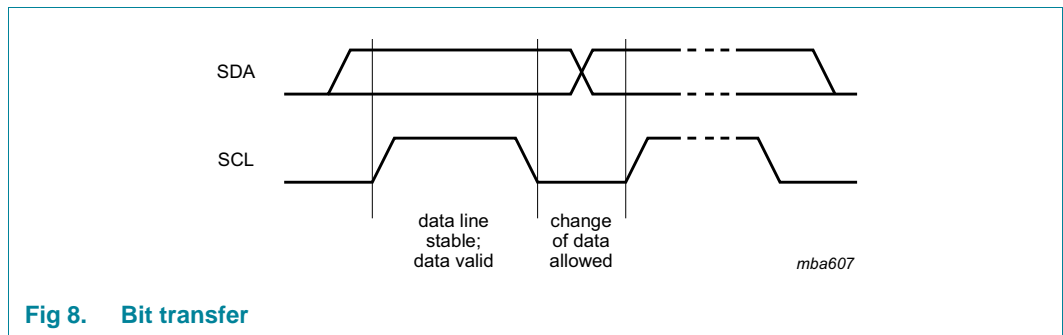


Fig 8. Bit transfer

### 7.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 9).

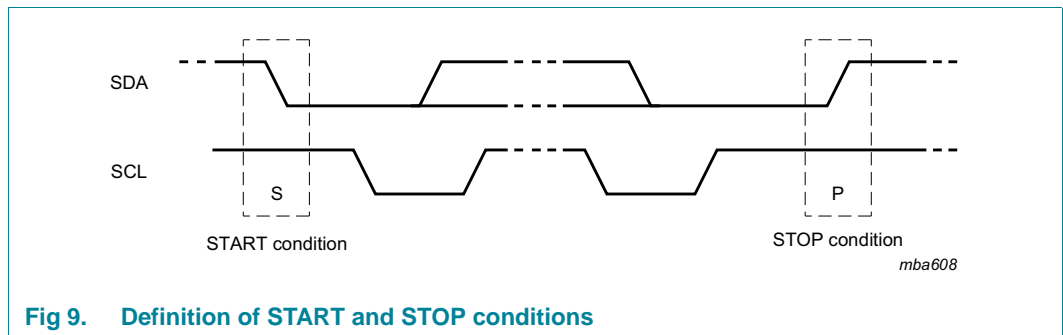


Fig 9. Definition of START and STOP conditions

### 7.3 System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see [Figure 10](#)).

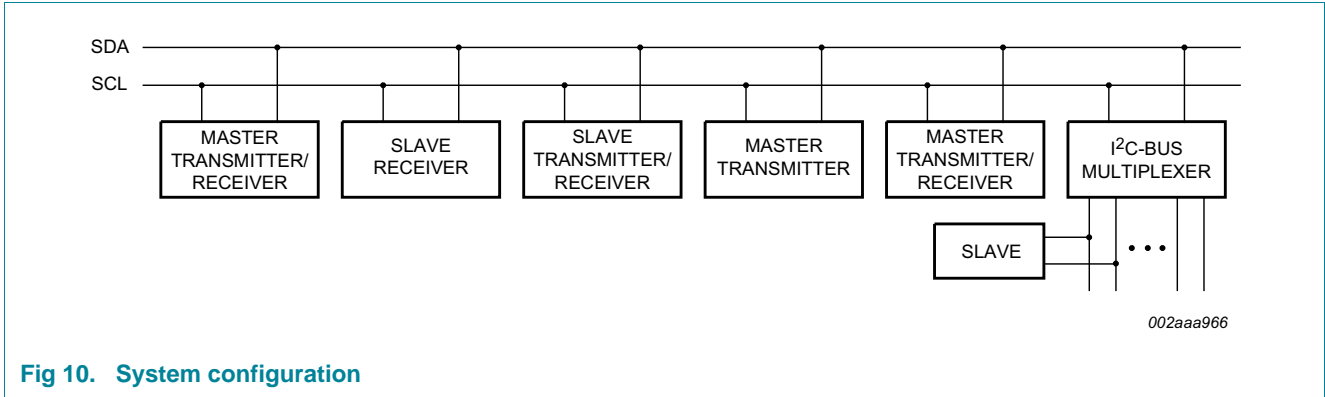


Fig 10. System configuration

### 7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of 8 bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

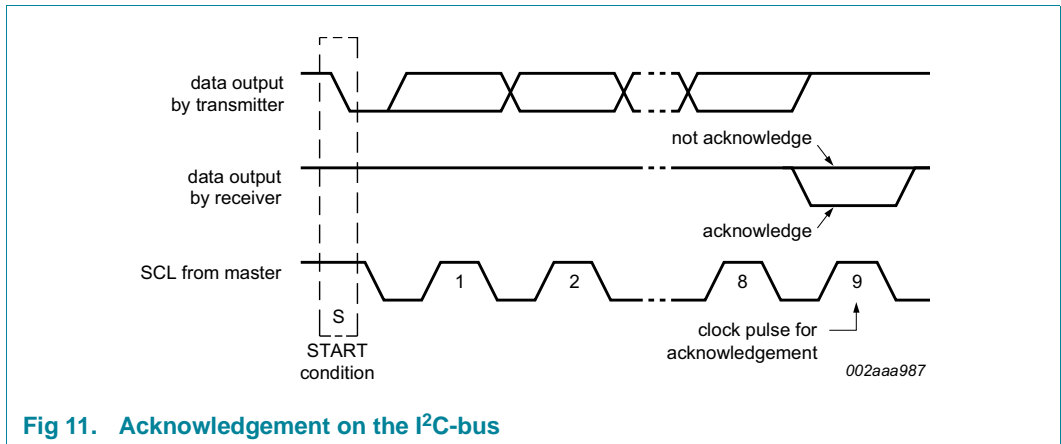


Fig 11. Acknowledgement on the I<sup>2</sup>C-bus



7.5 Bus transactions

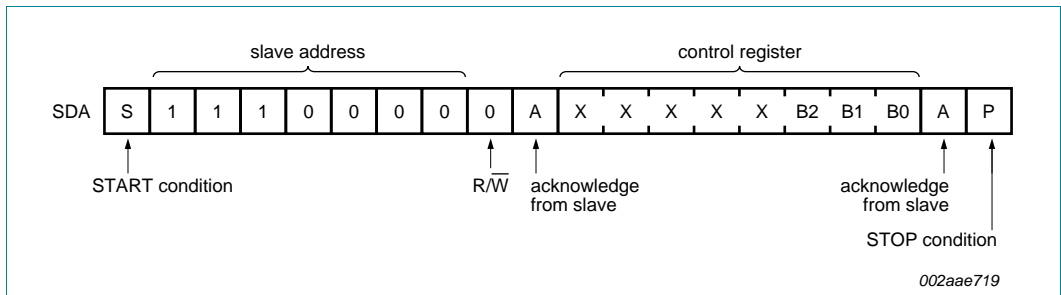


Fig 12. Write control register

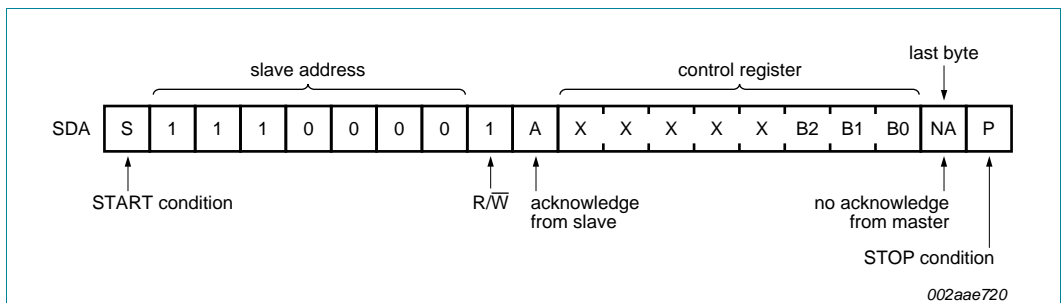


Fig 13. Read control register

8. Application design-in information

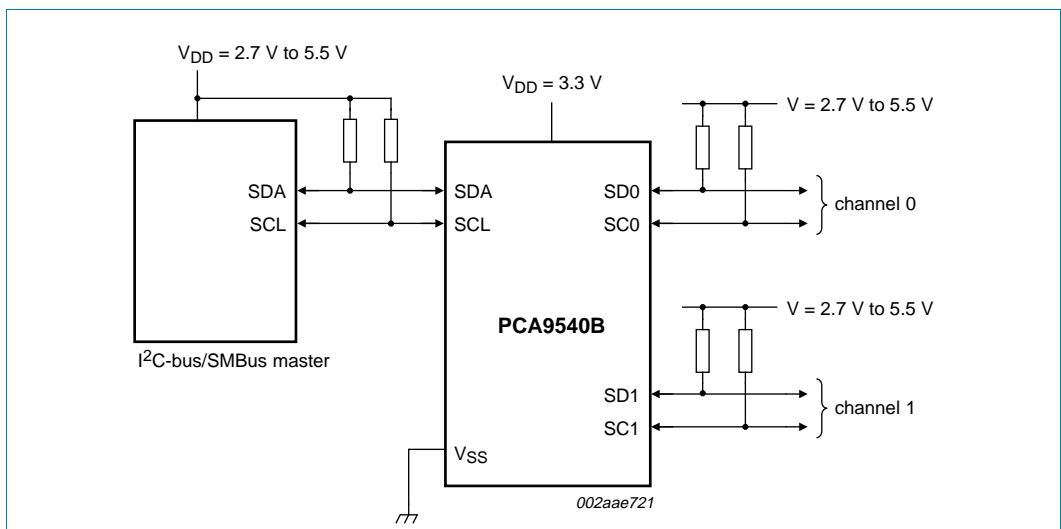


Fig 14. Typical application

## 9. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

*Voltages are referenced to ground ( $V_{SS} = 0$  V).*

| Symbol       | Parameter                    | Conditions | Min  | Max  | Unit |
|--------------|------------------------------|------------|------|------|------|
| $V_{DD}$     | supply voltage               |            | -0.5 | +7.0 | V    |
| $V_I$        | input voltage                |            | -0.5 | +7.0 | V    |
| $I_I$        | input current                |            | -    | ±20  | mA   |
| $I_O$        | output current               |            | -    | ±25  | mA   |
| $I_{DD}$     | supply current               |            | -    | ±100 | mA   |
| $I_{SS}$     | ground supply current        |            | -    | ±100 | mA   |
| $P_{tot}$    | total power dissipation      |            | -    | 400  | mW   |
| $T_{stg}$    | storage temperature          |            | -60  | +150 | °C   |
| $T_{amb}$    | ambient temperature          | operating  | -40  | +85  | °C   |
| $T_{j(max)}$ | maximum junction temperature | [1]        | -    | 125  | °C   |

- [1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 125 °C.

## 10. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol        | Parameter                                   | Conditions     | Typ | Unit |
|---------------|---|----------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | SO8 package    | 158 | °C/W |
|               |   | TSSOP8 package | 120 | °C/W |

## 11. Static characteristics

**Table 7. Static characteristics at V<sub>DD</sub> = 2.3 V to 3.6 V**

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.

See [Table 8](#) for V<sub>DD</sub> = 3.6 V to 5.5 V.

| Symbol                             | Parameter                | Conditions   | Min                | Typ | Max                 | Unit |
|------------------------------------|--------------------------|--|--------------------|-----|---------------------|------|
| <b>Supply</b>                      |                          |  |                    |     |                     |      |
| V <sub>DD</sub>                    | supply voltage           |  | 2.3                | -   | 3.6                 | V    |
| I <sub>DD</sub>                    | supply current           | operating mode; V <sub>DD</sub> = 3.6 V;<br>no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ;<br>f <sub>SCL</sub> = 100 kHz | -                  | 20  | 50                  | μA   |
| I <sub>stb</sub>                   | standby current          | standby mode; V <sub>DD</sub> = 3.6 V;<br>no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ;<br>f <sub>SCL</sub> = 0 kHz     | -                  | 0.1 | 1                   | μA   |
| V <sub>POR</sub>                   | power-on reset voltage   | no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>   | [1]                | 1.6 | 2.1                 | V    |
| <b>Input SCL; input/output SDA</b> |                          |  |                    |     |                     |      |
| V <sub>IL</sub>                    | LOW-level input voltage  |  | -0.5               | -   | +0.3V <sub>DD</sub> | V    |
| V <sub>IH</sub>                    | HIGH-level input voltage |  | 0.7V <sub>DD</sub> | -   | 6                   | V    |
| I <sub>OL</sub>                    | LOW-level output current | V <sub>OL</sub> = 0.4 V  | 3                  | -   | -                   | mA   |
|                                    |                          |  | 2.5[2]             | -   | -                   | mA   |
|                                    |                          | V <sub>OL</sub> = 0.6 V  | 6                  | -   | -                   | mA   |
|                                    |                          |  | 5.5[2]             | -   | -                   | mA   |
| I <sub>L</sub>                     | leakage current          | V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>  | -1                 | -   | +1                  | μA   |
| C <sub>i</sub>                     | input capacitance        | V <sub>I</sub> = V <sub>SS</sub>   | -                  | 7   | 8                   | pF   |
| <b>Pass gate</b>                   |                          |  |                    |     |                     |      |
| R <sub>on</sub>                    | ON-state resistance      | V <sub>DD</sub> = 3.0 V to 3.6 V; V <sub>O</sub> = 0.4 V;<br>I <sub>O</sub> = 15 mA  | 5                  | 11  | 31                  | Ω    |
|                                    |                          | V <sub>DD</sub> = 2.3 V to 2.7 V; V <sub>O</sub> = 0.4 V;<br>I <sub>O</sub> = 10 mA  | 7                  | 16  | 55                  | Ω    |
| V <sub>o(sw)</sub>                 | switch output voltage    | V <sub>i(sw)</sub> = V <sub>DD</sub> = 3.3 V; I <sub>o(sw)</sub> = -100 μA   | -                  | 1.9 | -                   | V    |
|                                    |                          | V <sub>i(sw)</sub> = V <sub>DD</sub> = 3.0 V to 3.6 V;<br>I <sub>o(sw)</sub> = -100 μA   | 1.6                | -   | 2.8                 | V    |
|                                    |                          | V <sub>i(sw)</sub> = V <sub>DD</sub> = 2.5 V; I <sub>o(sw)</sub> = -100 μA   | -                  | 1.5 | -                   | V    |
|                                    |                          | V <sub>i(sw)</sub> = V <sub>DD</sub> = 2.3 V to 2.7 V;<br>I <sub>o(sw)</sub> = -100 μA   | 1.1                | -   | 2.0                 | V    |
| I <sub>L</sub>                     | leakage current          | V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>  | -1                 | -   | +1                  | μA   |
| C <sub>io</sub>                    | input/output capacitance | V <sub>I</sub> = V <sub>SS</sub>   | -                  | 2.5 | 5                   | pF   |

[1] V<sub>DD</sub> must be lowered to 0.2 V for at least 5 μs in order to reset part.

[2] For PCA9540BDP/Q900 at -40 °C to +105 °C

**Table 8. Static characteristics at V<sub>DD</sub> = 3.6 V to 5.5 V**V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified.See [Table 7](#) for V<sub>DD</sub> = 2.3 V to 3.6 V.

| Symbol                             | Parameter                | Conditions   | Min                     | Typ | Max                 | Unit |
|------------------------------------|--------------------------|--|-------------------------|-----|---------------------|------|
| <b>Supply</b>                      |                          |  |                         |     |                     |      |
| V <sub>DD</sub>                    | supply voltage           |  | 3.6                     | -   | 5.5                 | V    |
| I <sub>DD</sub>                    | supply current           | operating mode; V <sub>DD</sub> = 5.5 V;<br>no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ;<br>f <sub>SCL</sub> = 100 kHz | -                       | 65  | 100                 | μA   |
| I <sub>stb</sub>                   | standby current          | standby mode; V <sub>DD</sub> = 5.5 V;<br>no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>                                   | -                       | 0.3 | 1                   | μA   |
| V <sub>POR</sub>                   | power-on reset voltage   | no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> <a href="#">[1]</a>   | -                       | 1.6 | 2.1                 | V    |
| <b>Input SCL; input/output SDA</b> |                          |  |                         |     |                     |      |
| V <sub>IL</sub>                    | LOW-level input voltage  |  | -0.5                    | -   | +0.3V <sub>DD</sub> | V    |
| V <sub>IH</sub>                    | HIGH-level input voltage |  | 0.7V <sub>DD</sub>      | -   | 6                   | V    |
| I <sub>OL</sub>                    | LOW-level output current | V <sub>OL</sub> = 0.4 V  | 3                       | -   | -                   | mA   |
|                                    |                          |  | 2.5 <a href="#">[2]</a> | -   | -                   | mA   |
|                                    |                          | V <sub>OL</sub> = 0.6 V  | 6                       | -   | -                   | mA   |
|                                    |                          |  | 5.5 <a href="#">[2]</a> | -   | -                   | mA   |
| I <sub>IL</sub>                    | LOW-level input current  | V <sub>I</sub> = V <sub>SS</sub>   | -1                      | -   | +1                  | μA   |
| I <sub>IH</sub>                    | HIGH-level input current | V <sub>I</sub> = V <sub>DD</sub>   | -1                      | -   | +1                  | μA   |
| C <sub>i</sub>                     | input capacitance        | V <sub>I</sub> = V <sub>SS</sub>   | -                       | 6   | 8                   | pF   |
| <b>Pass gate</b>                   |                          |  |                         |     |                     |      |
| R <sub>on</sub>                    | ON-state resistance      | V <sub>DD</sub> = 4.5 V to 5.5 V; V <sub>O</sub> = 0.4 V;<br>I <sub>O</sub> = 15 mA  | 4                       | 9   | 24                  | Ω    |
| V <sub>o(sw)</sub>                 | switch output voltage    | V <sub>i(sw)</sub> = V <sub>DD</sub> = 5.0 V; I <sub>o(sw)</sub> = -100 μA   | -                       | 3.6 | -                   | V    |
|                                    |                          | V <sub>i(sw)</sub> = V <sub>DD</sub> = 4.5 V to 5.5 V;<br>I <sub>o(sw)</sub> = -100 μA   | 2.6                     | -   | 4.5                 | V    |
| I <sub>L</sub>                     | leakage current          | V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>  | -1                      | -   | +1                  | μA   |
| C <sub>io</sub>                    | input/output capacitance | V <sub>I</sub> = V <sub>SS</sub>   | -                       | 2.5 | 5                   | pF   |

[1] V<sub>DD</sub> must be lowered to 0.2 V for at least 5 μs in order to reset part.

[2] For PCA9540BDP/Q900 at -40 °C to +105 °C

## 12. Dynamic characteristics

Table 9. Dynamic characteristics

| Symbol              | Parameter   | Conditions                        | Standard-mode I <sup>2</sup> C-bus |                    | Fast-mode I <sup>2</sup> C-bus        |                    | Unit |
|---------------------|---|-----------------------------------|------------------------------------|--------------------|---------------------------------------|--------------------|------|
|                     |   |                                   | Min                                | Max                | Min                                   | Max                |      |
| t <sub>PD</sub>     | propagation delay   | from SDA to SDx,<br>or SCL to SCx | -                                  | 0.3 <sup>[1]</sup> | -                                     | 0.3 <sup>[1]</sup> | ns   |
| f <sub>SCL</sub>    | SCL clock frequency   |                                   | 0                                  | 100                | 0                                     | 400                | kHz  |
| t <sub>BUF</sub>    | bus free time between a STOP and START condition                  |                                   | 4.7                                | -                  | 1.3                                   | -                  | μs   |
| t <sub>HD;STA</sub> | hold time (repeated) START condition                              | <sup>[2]</sup>                    | 4.0                                | -                  | 0.6                                   | -                  | μs   |
| t <sub>LOW</sub>    | LOW period of the SCL clock                                       |                                   | 4.7                                | -                  | 1.3                                   | -                  | μs   |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock                                      |                                   | 4.0                                | -                  | 0.6                                   | -                  | μs   |
| t <sub>SU;STA</sub> | set-up time for a repeated START condition                        |                                   | 4.7                                | -                  | 0.6                                   | -                  | μs   |
| t <sub>SU;STO</sub> | set-up time for STOP condition                                    |                                   | 4.0                                | -                  | 0.6                                   | -                  | μs   |
| t <sub>HD;DAT</sub> | data hold time  |                                   | 0 <sup>[3]</sup>                   | 3.45               | 0 <sup>[3]</sup>                      | 0.9                | μs   |
| t <sub>SU;DAT</sub> | data set-up time  |                                   | 250                                | -                  | 100                                   | -                  | ns   |
| t <sub>r</sub>      | rise time of both SDA and SCL signals                             |                                   | -                                  | 1000               | 20 + 0.1C <sub>b</sub> <sup>[4]</sup> | 300                | ns   |
| t <sub>f</sub>      | fall time of both SDA and SCL signals                             |                                   | -                                  | 300                | 20 + 0.1C <sub>b</sub> <sup>[4]</sup> | 300                | ns   |
| C <sub>b</sub>      | capacitive load for each bus line                                 |                                   | -                                  | 400                | -                                     | 400                | pF   |
| t <sub>SP</sub>     | pulse width of spikes that must be suppressed by the input filter |                                   | -                                  | 50                 | -                                     | 50                 | ns   |
| t <sub>VD;DAT</sub> | data valid time   | HIGH-to-LOW <sup>[5]</sup>        | -                                  | 1                  | -                                     | 1                  | μs   |
|                     |   | LOW-to-HIGH <sup>[5]</sup>        | -                                  | 0.6                | -                                     | 0.6                | μs   |
| t <sub>VD;ACK</sub> | data valid acknowledge time                                       |                                   | -                                  | 1                  | -                                     | 1                  | μs   |

[1] Pass gate propagation delay is calculated from the 20 Ω typical R<sub>on</sub> and the 15 pF load capacitance.

[2] After this period, the first clock pulse is generated.

[3] A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH(min)</sub> of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[4] C<sub>b</sub> = total capacitance of one bus line in pF.

[5] Measurements taken with 1 kΩ pull-up resistor and 50 pF load.

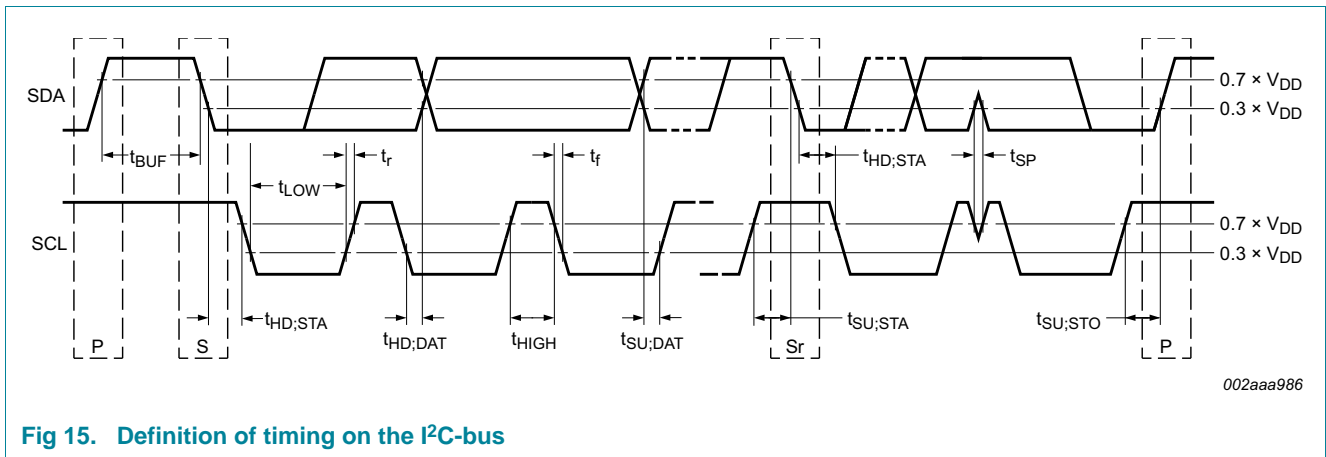


Fig 15. Definition of timing on the I<sup>2</sup>C-bus

### 13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



Fig 16. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

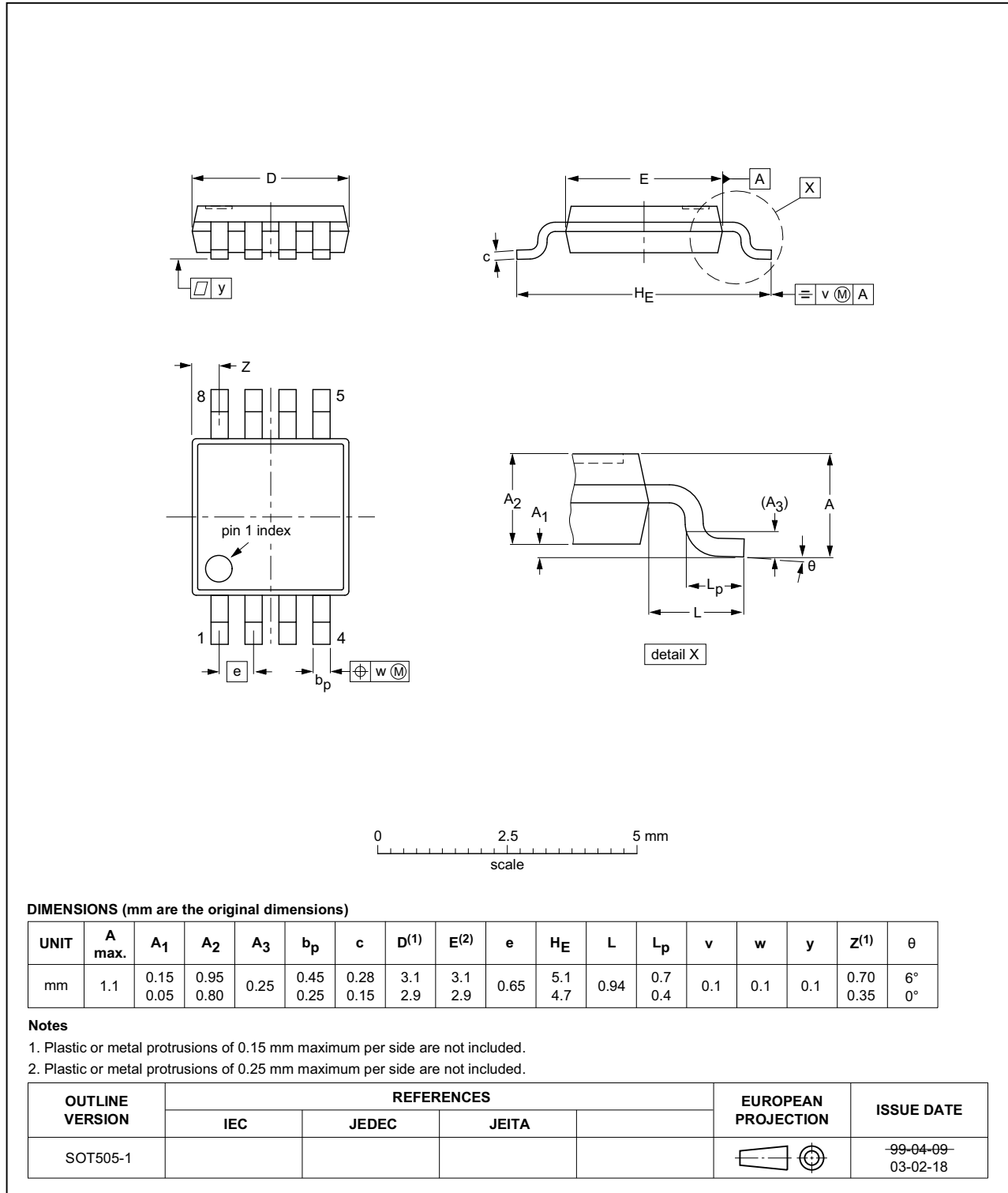


Fig 17. Package outline SOT505-1 (TSSOP8)



XSON8: plastic extremely thin small outline package; no leads;  
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

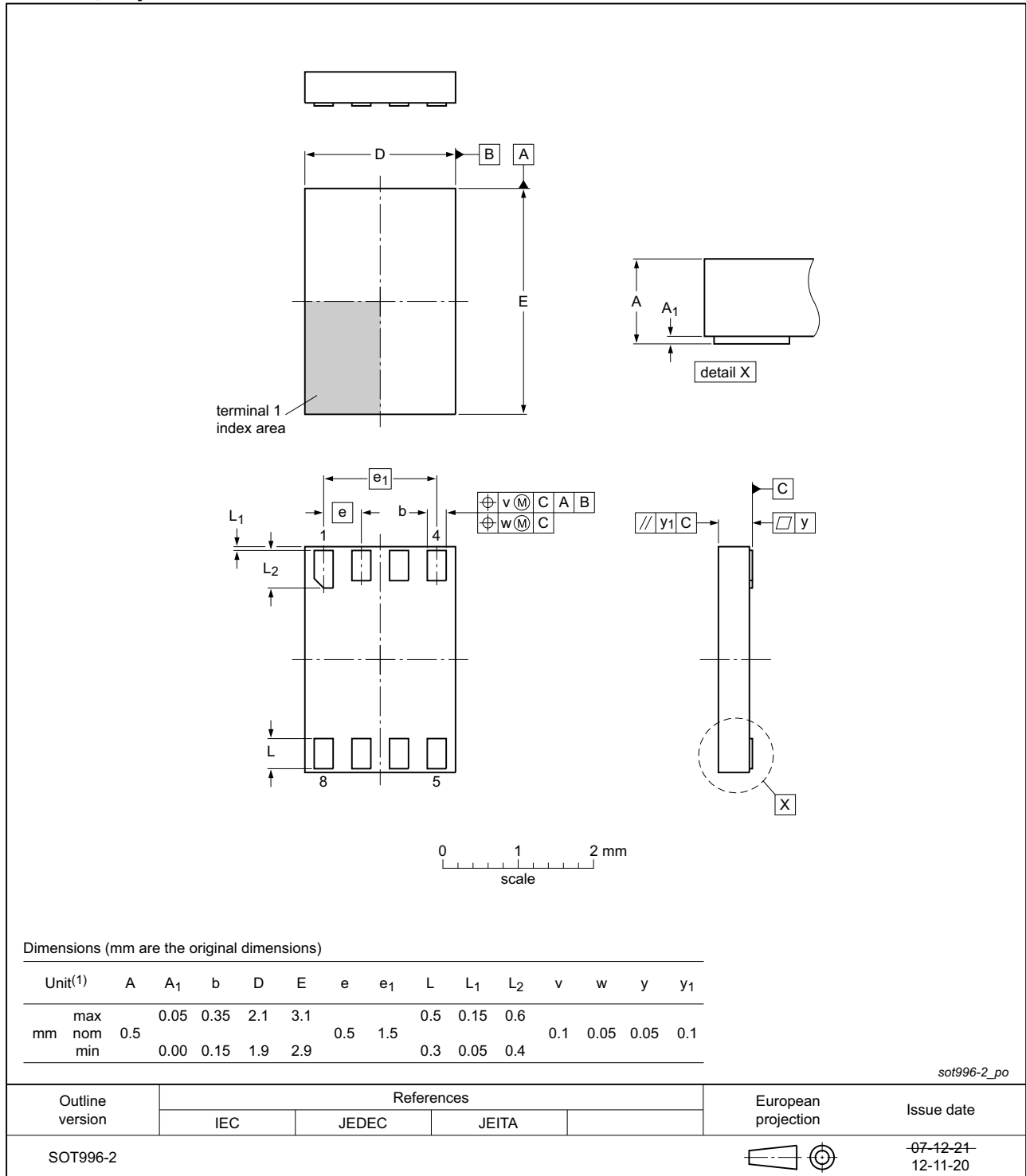


Fig 18. Package outline SOT996-2 (XSON8)

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 19](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 10](#) and [11](#)

**Table 10. SnPb eutectic process (from J-STD-020D)**

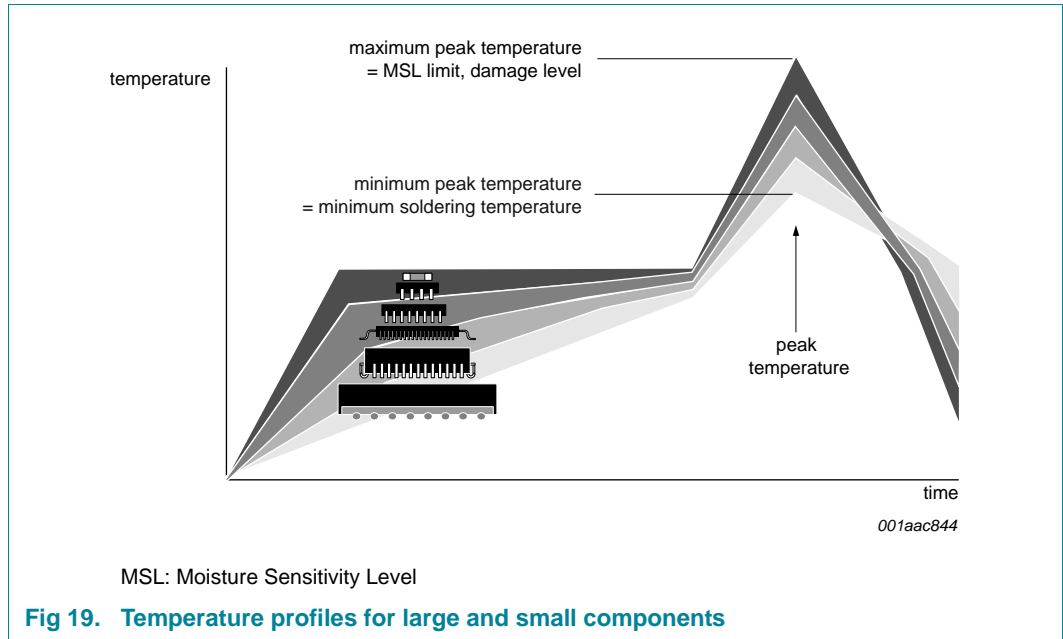
| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

**Table 11. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

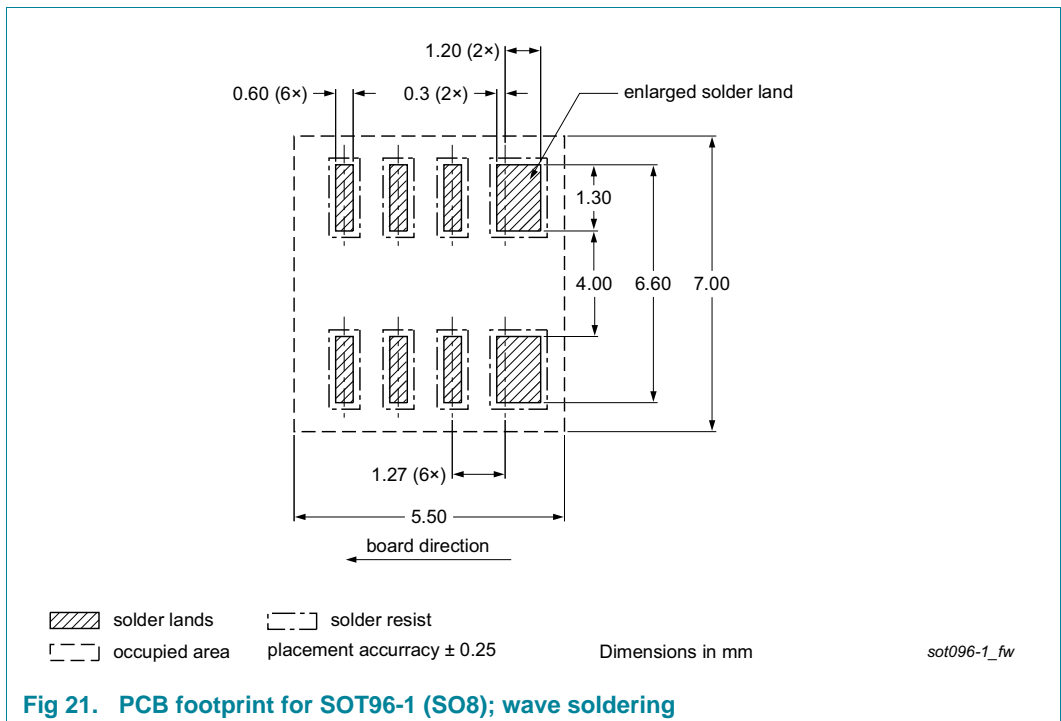
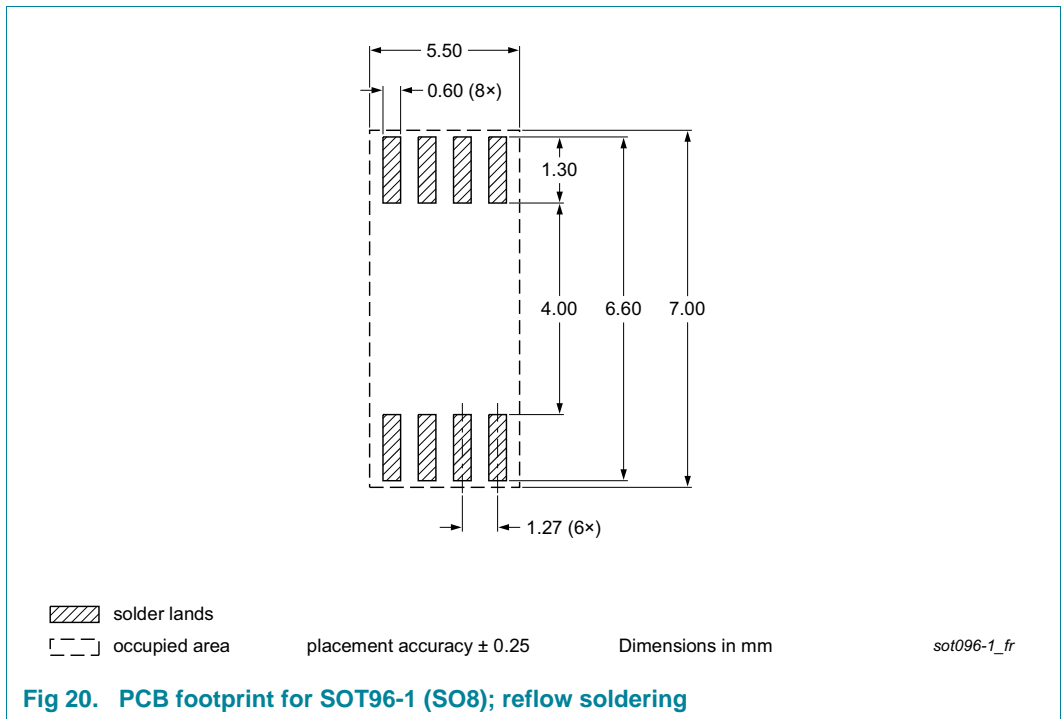
Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

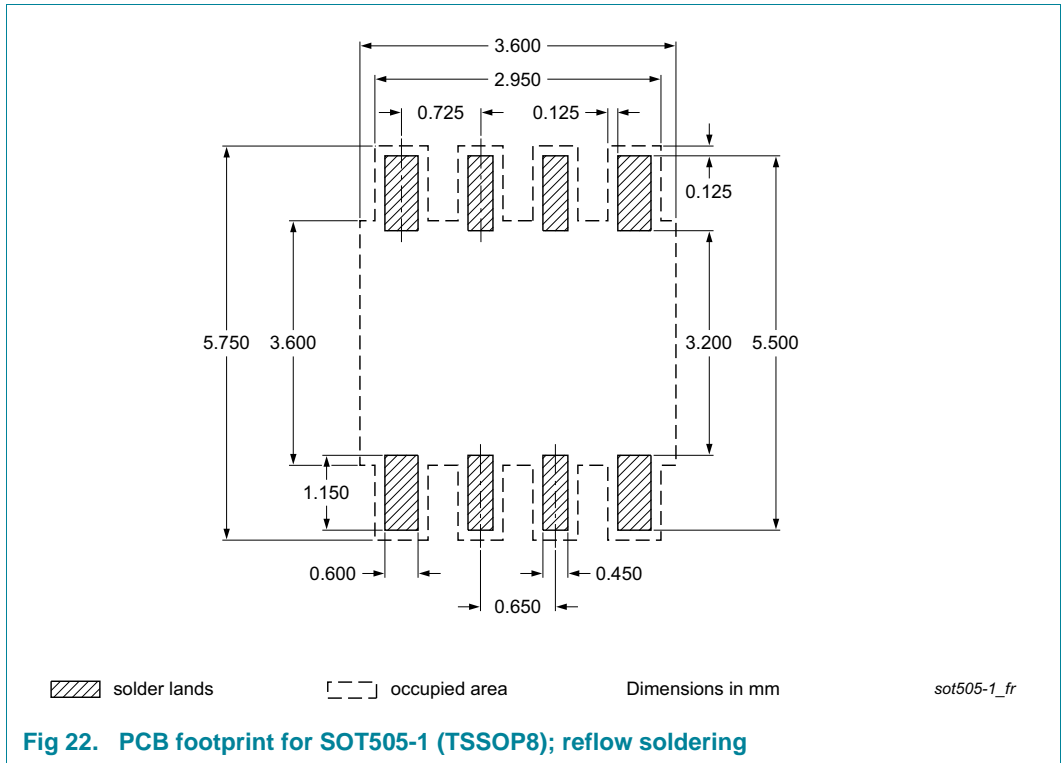
Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 19](#).

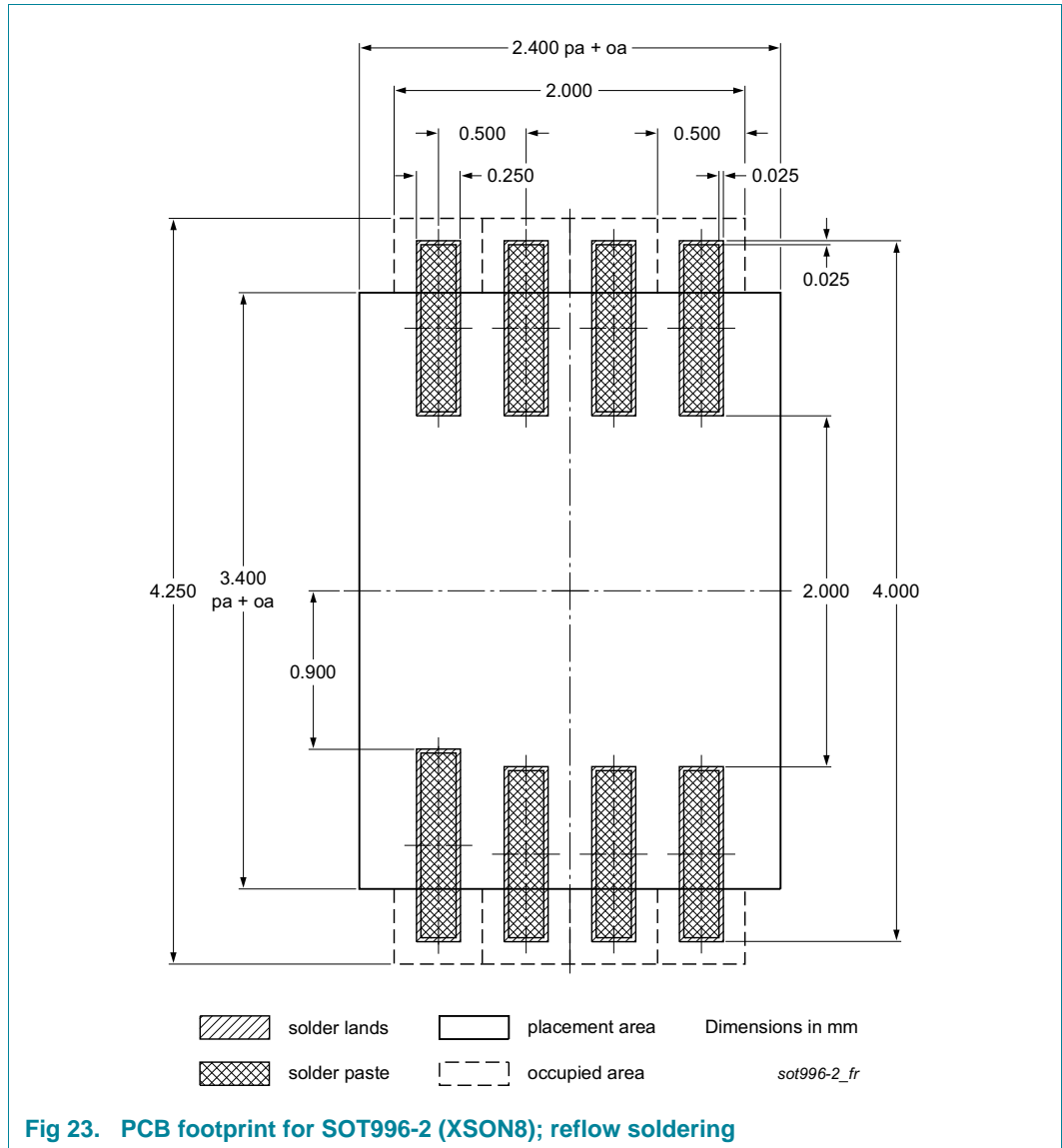


For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

### 15. Soldering: PCB footprints







## 16. Abbreviations

Table 12. Abbreviations

| Acronym              | Description                  |
|----------------------|------------------------------|
| CDM                  | Charged-Device Model         |
| ESD                  | ElectroStatic Discharge      |
| HBM                  | Human Body Model             |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus |
| I/O                  | Input/Output                 |
| IC                   | Integrated Circuit           |
| LSB                  | Least Significant Bit        |
| POR                  | Power-On Reset               |
| SMBus                | System Management Bus        |

## 17. Revision history

Table 13. Revision history

| Document ID    | Release date  | Data sheet status  | Change notice | Supersedes   |
|----------------|---|--------------------|---------------|--------------|
| PCA9540B v.7.1 | 20180119  | Product data sheet | -             | PCA9540B v.7 |
| Modifications: | <ul style="list-style-type: none"> <li>• <a href="#">Table 1 “Ordering information”</a>, <a href="#">Table note 1</a>: Corrected “PCA9538PW/Q900 to “PCA9540BDP/Q900”; added additional contact information</li> <li>• <a href="#">Table 2 “Ordering options”</a>: Removed DOD part numbers PCA9540BD,112 and PCA9540BDP/DG,118</li> </ul>  |                    |               |              |
| PCA9540B v.7   | 20161031  | Product data sheet | -             | PCA9540B v.6 |
| Modifications: | <ul style="list-style-type: none"> <li>• Added PCA9540BDP/Q900</li> <li>• <a href="#">Table 7 “Static characteristics at V<sub>DD</sub> = 2.3 V to 3.6 V”</a>: Added I<sub>OL</sub> char data for PCA9540BDP/Q900</li> <li>• <a href="#">Table 8 “Static characteristics at V<sub>DD</sub> = 3.6 V to 5.5 V”</a>: Added I<sub>OL</sub> char data for PCA9540BDP/Q900</li> </ul>   |                    |               |              |
| PCA9540B v.6   | 20140505  | Product data sheet | -             | PCA9540B v.5 |
| Modifications: | <ul style="list-style-type: none"> <li>• Corrected “XSON8U” to “XSON8” throughout data sheet (correction to documentation only; no change to device)</li> <li>• <a href="#">Table 1 “Ordering information”</a>: corrected package description for XSON8 by deleting phrase “UTLP based” (correction to documentation only; no change to device)</li> <li>• <a href="#">Table 2 “Ordering options”</a>: ‘Packing method’ descriptions are updated (text only, no change to packing method)</li> <li>• <a href="#">Section 6.3 “Power-on reset”</a>, first paragraph, third sentence corrected: from “Thereafter, V<sub>DD</sub> must be lowered below 0.2 V to reset the device.” to “Thereafter, V<sub>DD</sub> must be lowered below 0.2 V for at least 5 μs in order to reset the device.” (correction to documentation only; no change to device)</li> <li>• <a href="#">Table 7 “Static characteristics at V<sub>DD</sub> = 2.3 V to 3.6 V”</a>: <a href="#">Table note [1]</a> corrected by inserting phrase “for at least 5 μs” (correction to documentation only; no change to device)</li> <li>• <a href="#">Table 8 “Static characteristics at V<sub>DD</sub> = 3.6 V to 5.5 V”</a>: <a href="#">Table note [1]</a> corrected by inserting phrase “for at least 5 μs” (correction to documentation only; no change to device)</li> </ul> |                    |               |              |
| PCA9540B v.5   | 20130212  | Product data sheet | -             | PCA9540B v.4 |



Table 13. Revision history ...continued

| Document ID                      | Release date | Data sheet status  | Change notice | Supersedes   |
|----------------------------------|--------------|--------------------|---------------|--------------|
| PCA9540B v.4                     | 20090903     | Product data sheet | -             | PCA9540B v.3 |
| PCA9540B v.3                     | 20090528     | Product data sheet | -             | PCA9540B v.2 |
| PCA9540B v.2<br>(9397 750 13731) | 20040929     | Product data sheet | -             | PCA9540B v.1 |
| PCA9540B v.1<br>(9397 750 12918) | 20040413     | Product data       | -             | -            |

## 18. Legal information

### 18.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

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