



PCA9538

8-bit I²C-bus and SMBus low power I/O port with interrupt and reset

Rev. 8 — 8 November 2017

Product data sheet

1. General description

The PCA9538 is a 16-pin CMOS device that provides 8 bits of General Purpose parallel Input/Output (GPIO) expansion with interrupt and reset for I²C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push-buttons, LEDs, fans, etc.

The PCA9538 consists of an 8-bit Configuration register (input or output selection), 8-bit Input Port register, 8-bit Output Port register and an 8-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The PCA9538 is identical to the PCA9554 except for the removal of the internal I/O pull-up resistor which greatly reduces power consumption when the I/Os are held LOW, replacement of A2 with RESET and different address range.

The PCA9538 open-drain interrupt output (INT) is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine. The RESET pin causes the same reset/initialization to occur without de-powering the device.

Two hardware pins (A0 and A1) vary the fixed I²C-bus address and allow up to four devices to share the same I²C-bus/SMBus.

2. Features and benefits

- 8-bit I²C-bus GPIO with interrupt and reset
- Operating power supply voltage range of 2.3 V to 5.5 V (3.0 V to 5.5 V for PCA9538PW/Q900)
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Active LOW reset input
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up



- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Offered in three different packages: SO16, TSSOP16 and HVQFN16

3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package			Version
		Name	Description		
PCA9538BS	9538	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm		SOT629-1
PCA9538D	PCA9538D	SO16	plastic small outline package; 16 leads; body width 7.5 mm		SOT162-1
PCA9538PW	PCA9538	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm		SOT403-1
PCA9538PW/Q900 ^[1]	PCA9538	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm		SOT403-1

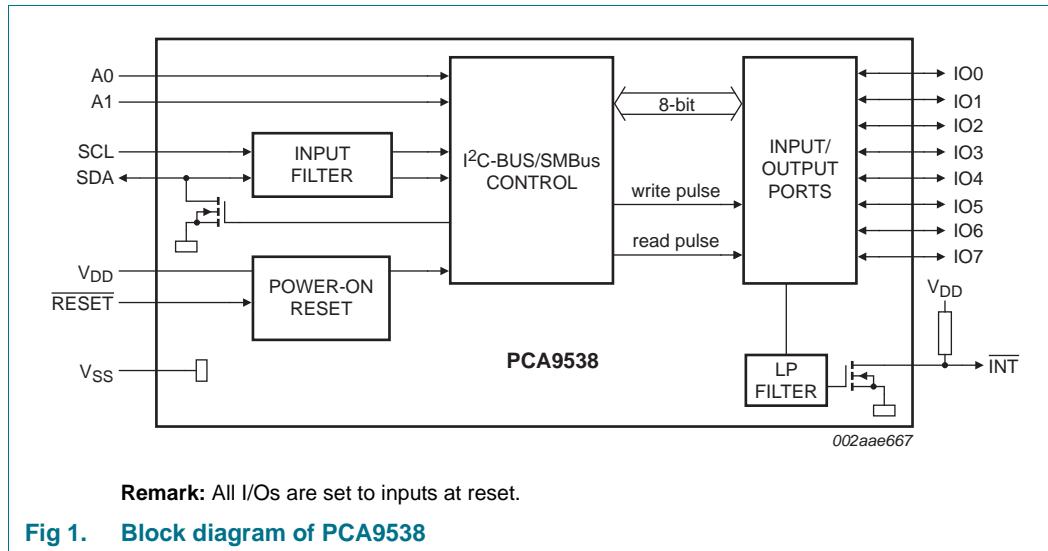
[1] PCA9538PW/Q900 is AEC-Q100 compliant. Contact i2c.support@nxp.com for PPAP.

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9538BS	PCA9538BS,118	HVQFN16	Reel pack, SMD, 13-inch	6000	T _{amb} = -40 °C to +85 °C
PCA9538D	PCA9538D,112	SO16	Tube, bulk pack	1920	T _{amb} = -40 °C to +85 °C
	PCA9538D,118	SO16	Reel pack, SMD, 13-inch	1000	T _{amb} = -40 °C to +85 °C
PCA9538PW	PCA9538PW,112	TSSOP16	Tube, bulk pack	2400	T _{amb} = -40 °C to +85 °C
	PCA9538PW,118	TSSOP16	Reel pack, SMD, 13-inch	2500	T _{amb} = -40 °C to +85 °C
PCA9538PW/Q900	PCA9538PW/Q900,118	TSSOP16	Reel pack, SMD, 13-inch	2500	T _{amb} = -40 °C to +125 °C

4. Block diagram



5. Pinning information

5.1 Pinning

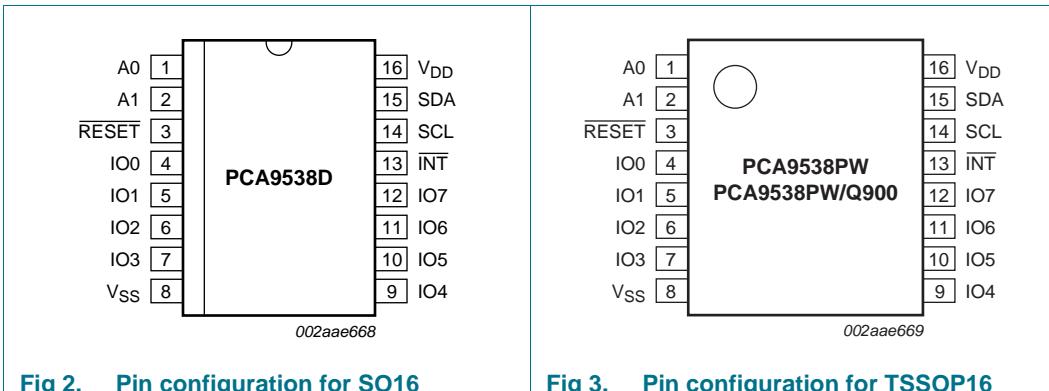


Fig 2. Pin configuration for SO16

Fig 3. Pin configuration for TSSOP16

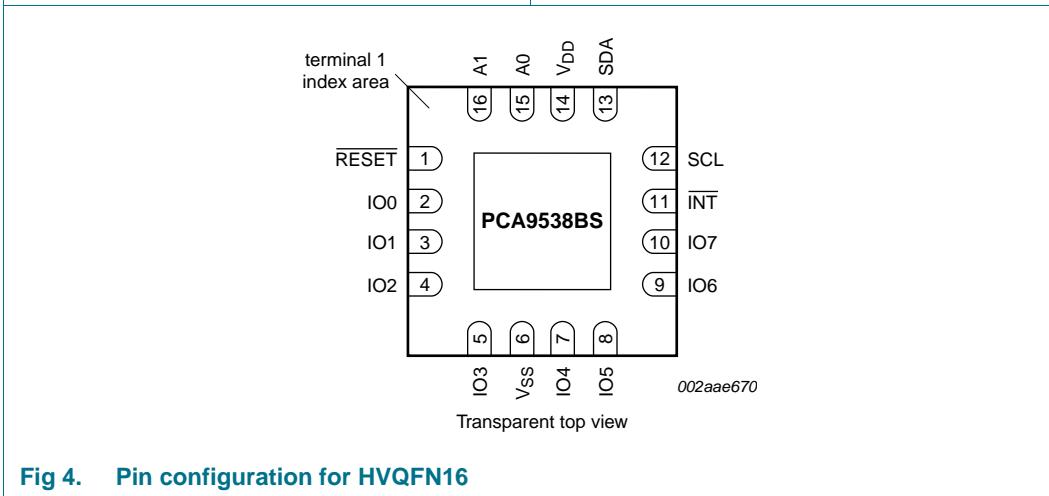


Fig 4. Pin configuration for HVQFN16

5.2 Pin description

Table 3. Pin description

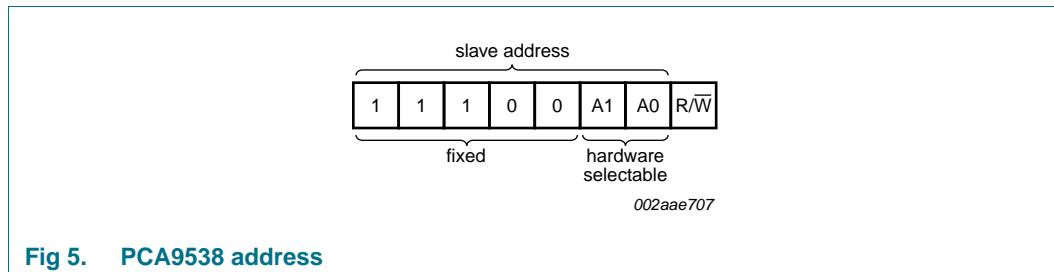
Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
A0	1	15	address input 0
A1	2	16	address input 1
RESET	3	1	active LOW reset input
IO0	4	2	input/output 0
IO1	5	3	input/output 1
IO2	6	4	input/output 2
IO3	7	5	input/output 3
V _{SS}	8	6 ^[1]	supply ground
IO4	9	7	input/output 4
IO5	10	8	input/output 5
IO6	11	9	input/output 6
IO7	12	10	input/output 7
INT	13	11	interrupt output (open-drain)
SCL	14	12	serial clock line
SDA	15	13	serial data line
V _{DD}	16	14	supply voltage

[1] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board, and for proper heat conduction through the board thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

6. Functional description

Refer to [Figure 1 “Block diagram of PCA9538”](#).

6.1 Device address



6.2 Registers

6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the registers will be written or read.

Table 4. Command byte

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

6.2.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default value 'X' is determined by the externally applied logic level.

Table 5. Register 0 - Input Port register bit description

Legend: * default value

Bit	Symbol	Access	Value	Description
7	I7	read only	X*	value 'X' is determined by externally applied logic level
6	I6	read only	X*	
5	I5	read only	X*	
4	I4	read only	X*	
3	I3	read only	X*	
2	I2	read only	X*	
1	I1	read only	X*	
0	I0	read only	X*	

6.2.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 6. Register 1 - Output Port register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	O7	R	1*	
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

6.2.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with 1), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a 0), the Input Port data polarity is retained.

Table 7. Register 2 - Polarity Inversion register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

6.2.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs.

Table 8. Register 3 - Configuration register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	configures the directions of the I/O pins 0 = corresponding port pin enabled as an output 1 = corresponding port pin configured as an input (default value)
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

6.3 Power-on reset

When power is applied to V_{DD} , an internal Power-On Reset (POR) holds the PCA9538 in a reset condition until V_{DD} has reached V_{POR} . At that point, the reset condition is released and the PCA9538 registers and state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

6.4 RESET input

A reset can be accomplished by holding the RESET pin LOW for a minimum of $t_{w(rst)}$. The PCA9538 registers and SMBus/I²C-bus state machine will be held in their default state until the RESET input is once again HIGH. This input requires a pull-up resistor to V_{DD} if no active connection is used.

6.5 Interrupt output

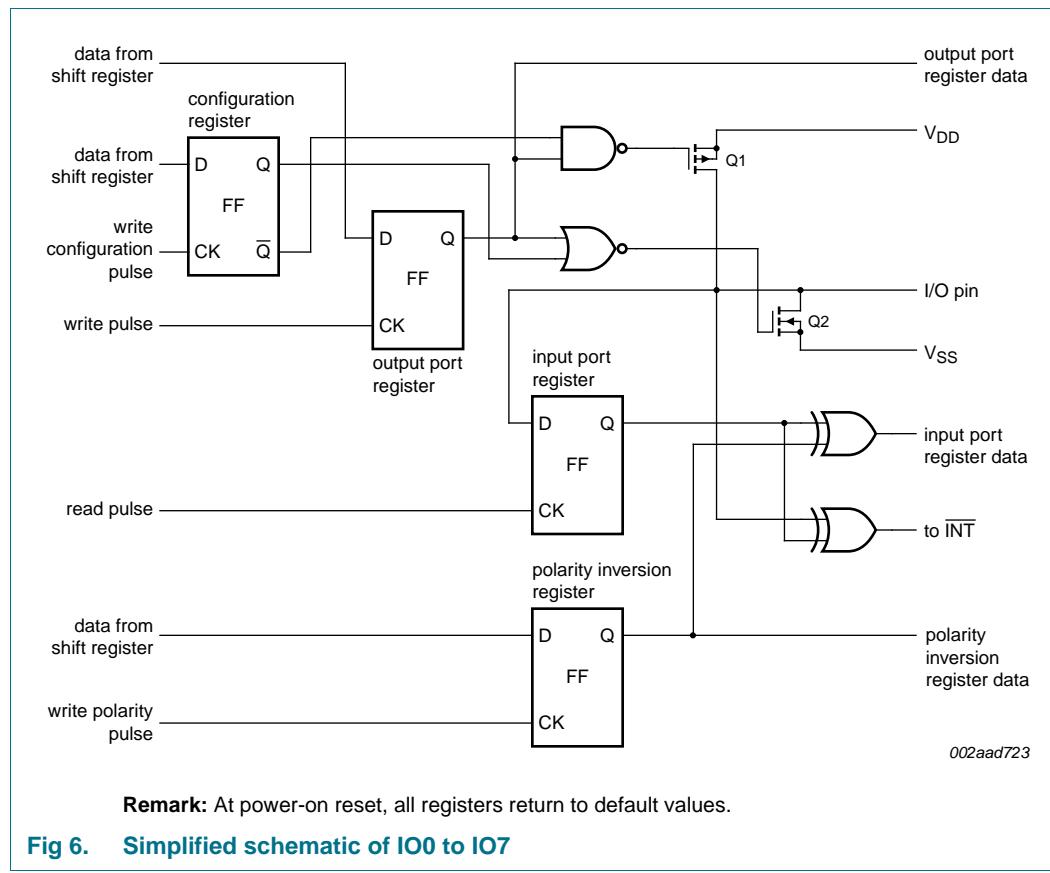
The open-drain interrupt output (INT) is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is de-activated when the input returns to its previous state or the Input Port register is read.

Note that changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

6.6 I/O port

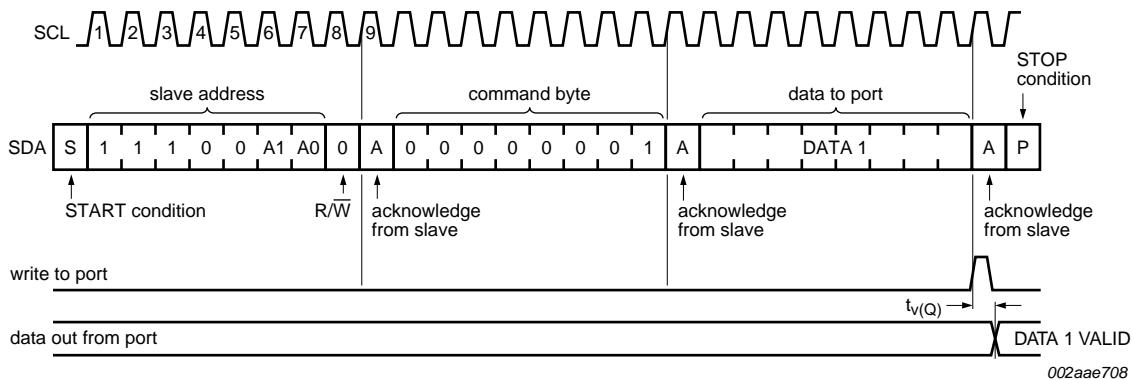
When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V_{DD} or V_{SS}.



6.7 Bus transactions

Data is transmitted to the PCA9538 registers using the write mode as shown in [Figure 7](#) and [Figure 8](#). Data is read from the PCA9538 registers using the read mode as shown in [Figure 9](#) and [Figure 10](#). These devices do not implement an auto-increment function so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.



Expanded diagram is shown in [Figure 18](#).

Fig 7. Write to output port register

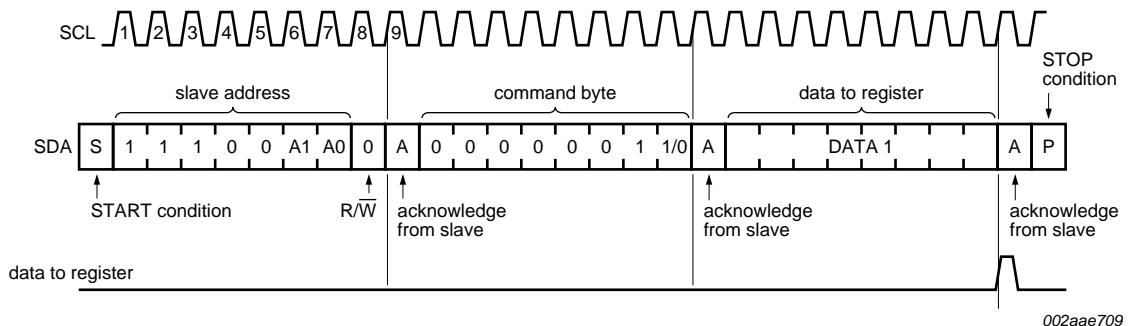


Fig 8. Write to configuration or polarity inversion registers

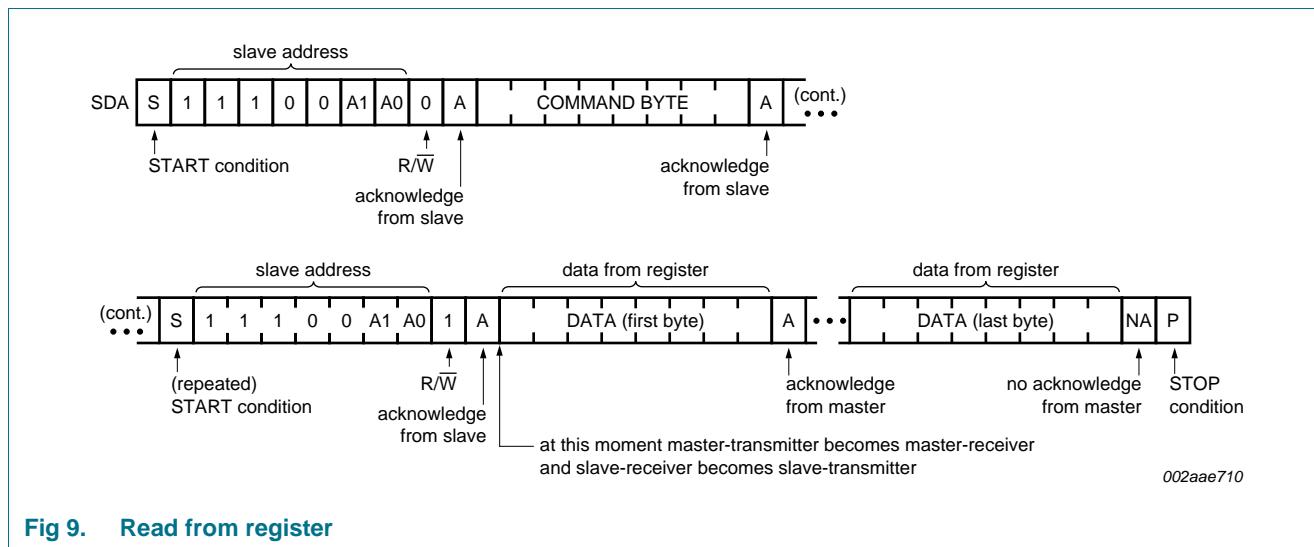


Fig 9. Read from register

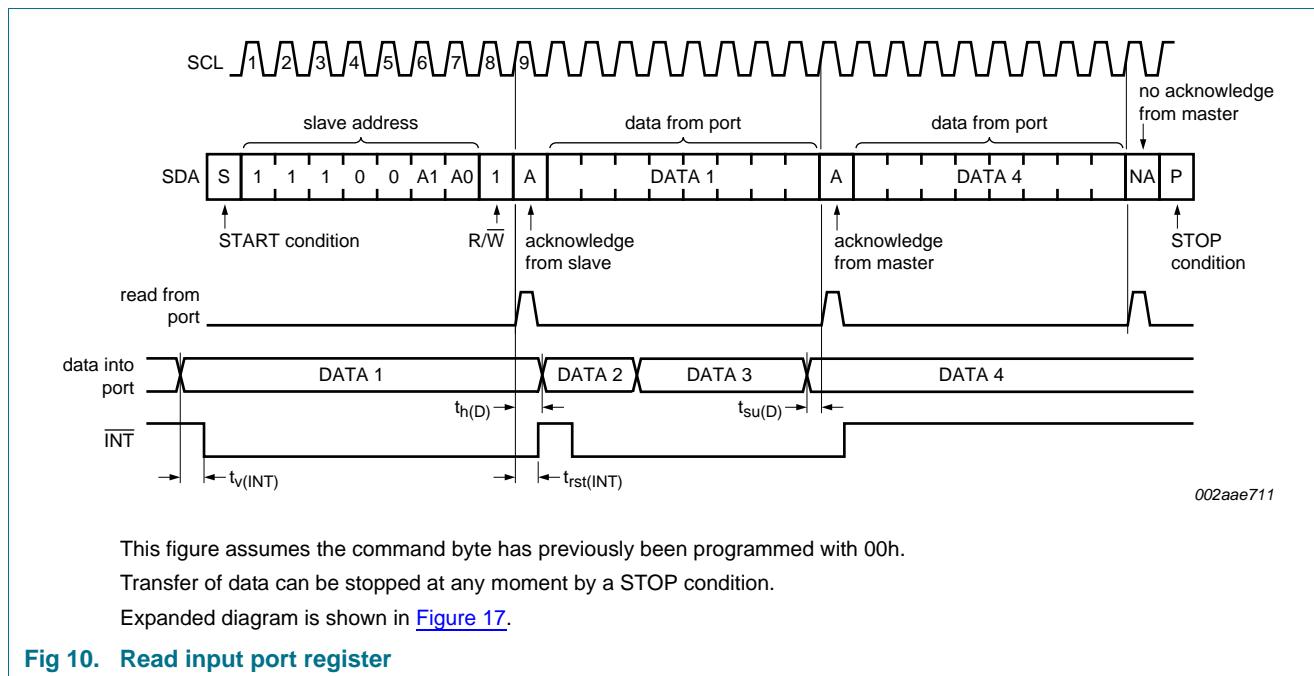
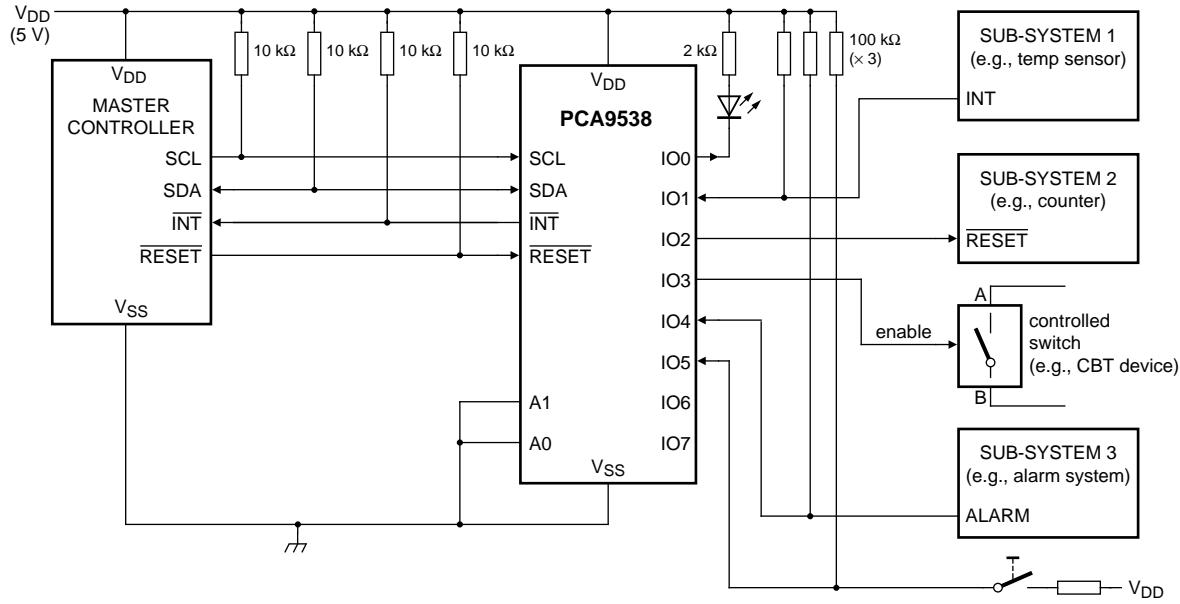


Fig 10. Read input port register

7. Application design-in information



Device address is 1110 000x for this example.

IO0, IO2, IO3 configured as outputs.

IO1, IO4, IO5 configured as inputs.

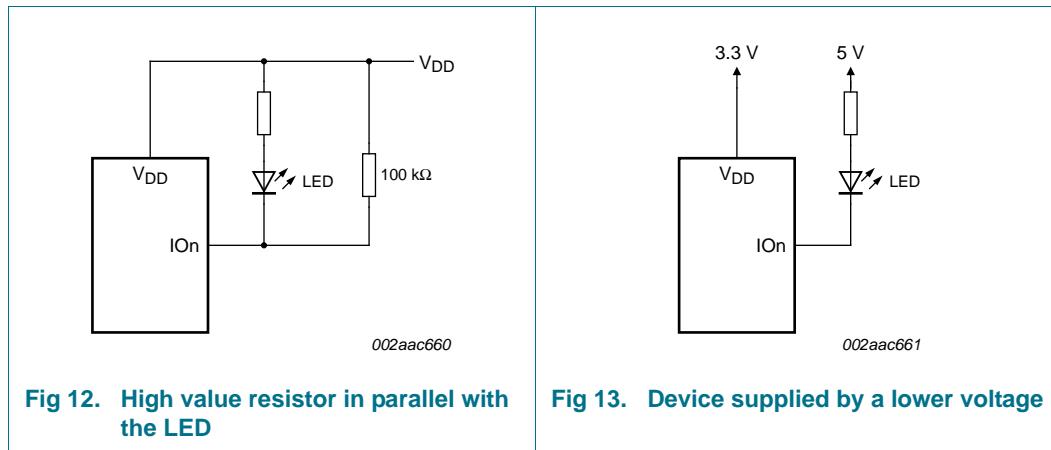
IO6, IO7 are not used and need 100 kΩ pull-up resistors to protect them from floating.

Fig 11. Typical application

7.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in [Figure 11](#). Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. [Figure 12](#) shows a high value resistor in parallel with the LED. [Figure 13](#) shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.



8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		-0.5	+6.0	V
I _I	input current		-	± 20	mA
V _{I/O}	voltage on an input/output pin		V _{SS} - 0.5	5.5	V
I _O (I _{On})	output current on pin I _{On}		-	± 50	mA
I _{DD}	supply current		-	85	mA
I _{SS}	ground supply current		-	100	mA
P _{tot}	total power dissipation		-	200	mW
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature	operating			
		all devices except PCA9538PW/Q900	-40	+85	°C
		PCA9538PW/Q900	-40	+125	°C
T _{j(max)}	maximum junction temperature		-	+125	°C

9. Static characteristics

Table 10. Static characteristics for all devices except PCA9538PW/Q900

$V_{DD} = 2.3\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Supplies							
V_{DD}	supply voltage		2.3	-	5.5	V	
I_{DD}	supply current	operating mode; $V_{DD} = 5.5\text{ V}$; no load; $f_{SCL} = 100\text{ kHz}$	-	104	175	μA	
I_{stbL}	LOW-level standby current	Standby mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{SS}$; $f_{SCL} = 0\text{ kHz}$; I/O = inputs	-	0.25	1	μA	
I_{stbH}	HIGH-level standby current	Standby mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{DD}$; $f_{SCL} = 0\text{ kHz}$; I/O = inputs	-	0.25	1	μA	
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[1]	-	1.7	2.2	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V	
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V	
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	7	-	mA	
I_L	leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA	
C_i	input capacitance	$V_I = V_{SS}$	-	5	10	pF	
I/Os							
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V	
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V	
I_{OL}	LOW-level output current	$V_{OL} = 0.5\text{ V}$					
		$V_{DD} = 2.3\text{ V}$	[2]	8	10	-	mA
		$V_{DD} = 3.0\text{ V}$	[2]	8	14	-	mA
		$V_{DD} = 4.5\text{ V}$	[2]	8	17	-	mA
		$V_{OL} = 0.7\text{ V}$					
		$V_{DD} = 2.3\text{ V}$	[2]	10	13	-	mA
		$V_{DD} = 3.0\text{ V}$	[2]	10	19	-	mA
		$V_{DD} = 4.5\text{ V}$	[2]	10	24	-	mA
V_{OH}	HIGH-level output voltage	$I_{OH} = -8\text{ mA}$					
		$V_{DD} = 2.3\text{ V}$	[3]	1.8	-	-	V
		$V_{DD} = 3.0\text{ V}$	[3]	2.6	-	-	V
		$V_{DD} = 4.5\text{ V}$	[3]	4.1	-	-	V
		$I_{OH} = -10\text{ mA}$					
		$V_{DD} = 2.3\text{ V}$	[3]	1.7	-	-	V
		$V_{DD} = 3.0\text{ V}$	[3]	2.5	-	-	V
		$V_{DD} = 4.5\text{ V}$	[3]	4.0	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA	
C_i	input capacitance		-	5	10	pF	

Table 10. Static characteristics for all devices except PCA9538PW/Q900 ...continued $V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}; V_{SS} = 0 \text{ V}; T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}; \text{unless otherwise specified.}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Interrupt INT						
I_{OL}	LOW-level output current	$V_{OL} = 0.4 \text{ V}$	3	13	-	mA
Select inputs A0, A1, RESET						
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
I_{LI}	input leakage current		-1	-	+1	μA

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

Table 11. Static characteristics for PCA9538PW/Q900 AEC-Q100 compliant device $V_{DD} = 3.0 \text{ V to } 5.5 \text{ V}; V_{SS} = 0 \text{ V}; T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}; \text{unless otherwise specified.}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Supplies							
V_{DD}	supply voltage		3.0	-	5.5	V	
I_{DD}	supply current	operating mode; $V_{DD} = 5.5 \text{ V}$; no load; $f_{SCL} = 100 \text{ kHz}$	-	104	175	μA	
I_{stbL}	LOW-level standby current	Standby mode; $V_{DD} = 5.5 \text{ V}$; no load; $V_I = V_{SS}$; $f_{SCL} = 0 \text{ kHz}$; I/O = inputs	-	0.25	1	μA	
I_{stbH}	HIGH-level standby current	Standby mode; $V_{DD} = 5.5 \text{ V}$; no load; $V_I = V_{DD}$; $f_{SCL} = 0 \text{ kHz}$; I/O = inputs	-	0.25	1	μA	
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[1]	-	1.7	2.2	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V	
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V	
I_{OL}	LOW-level output current, SDA	$V_{OL} = 0.4 \text{ V}$					
		$V_{DD} = 5.5 \text{ V}$	3	7	-	mA	
		$V_{DD} = 3.0 \text{ V}$	2.5	-	-	mA	
I_L	leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA	
C_i	input capacitance	$V_I = V_{SS}$	-	5	10	pF	
I/Os							
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V	
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V	
I_{OL}	LOW-level output current	$V_{OL} = 0.5 \text{ V}$					
		$V_{DD} = 4.5 \text{ V}$	[2]	8	17	mA	
		$V_{DD} = 3.0 \text{ V}$	[2]	7.5	-	mA	
		$V_{OL} = 0.7 \text{ V}$					
		$V_{DD} = 4.5 \text{ V}$	[2]	10	24	mA	
		$V_{DD} = 3.0 \text{ V}$	[2]	9.5	-	mA	

Table 11. Static characteristics for PCA9538PW/Q900 AEC-Q100 compliant device ...continued $V_{DD} = 3.0 \text{ V to } 5.5 \text{ V}; V_{SS} = 0 \text{ V}; T_{amb} = -40 \text{ }^{\circ}\text{C to } +125 \text{ }^{\circ}\text{C}; \text{unless otherwise specified.}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$I_{OH} = -8 \text{ mA}$				
		$V_{DD} = 4.5 \text{ V}$	[3] 4.1	-	-	V
		$V_{DD} = 3.0 \text{ V}$	[3] 2.5	-	-	V
		$I_{OH} = -10 \text{ mA}$				
		$V_{DD} = 4.5 \text{ V}$	[3] 4.0	-	-	V
		$V_{DD} = 3.0 \text{ V}$	[3] 2.4	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA
C_i	input capacitance		-	5	10	pF
Interrupt INT						
I_{OL}	LOW-level output current	$V_{OL} = 0.4 \text{ V}$	3	13	-	mA
Select inputs A0, A1, RESET						
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
I_{LI}	input leakage current		-1	-	+1	μA

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

10. Dynamic characteristics

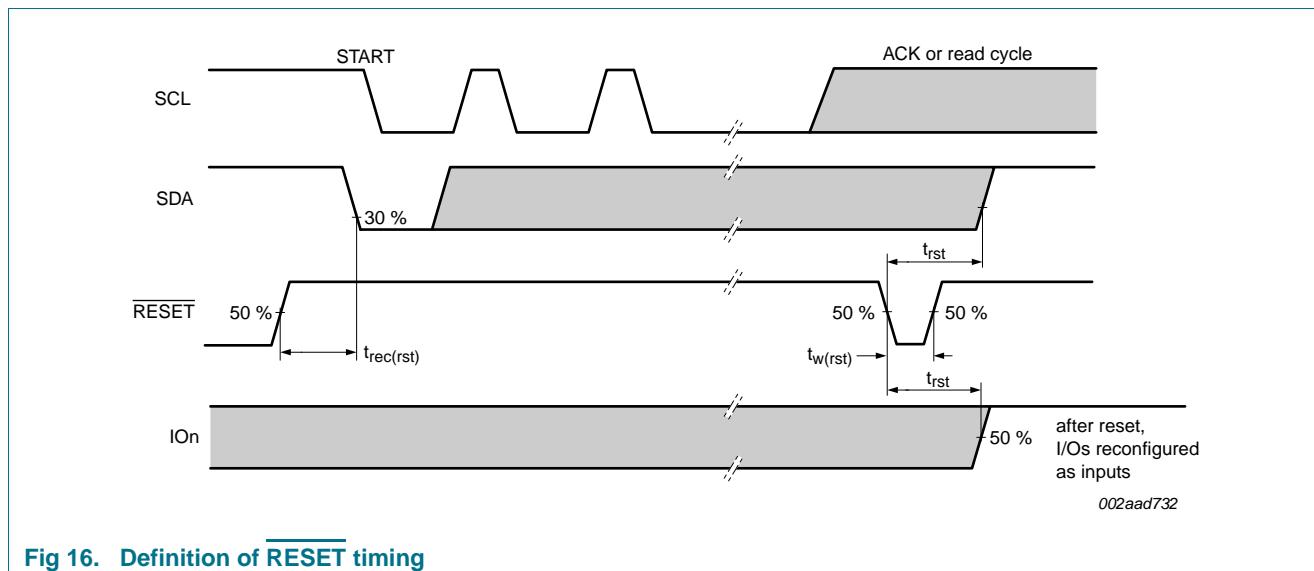
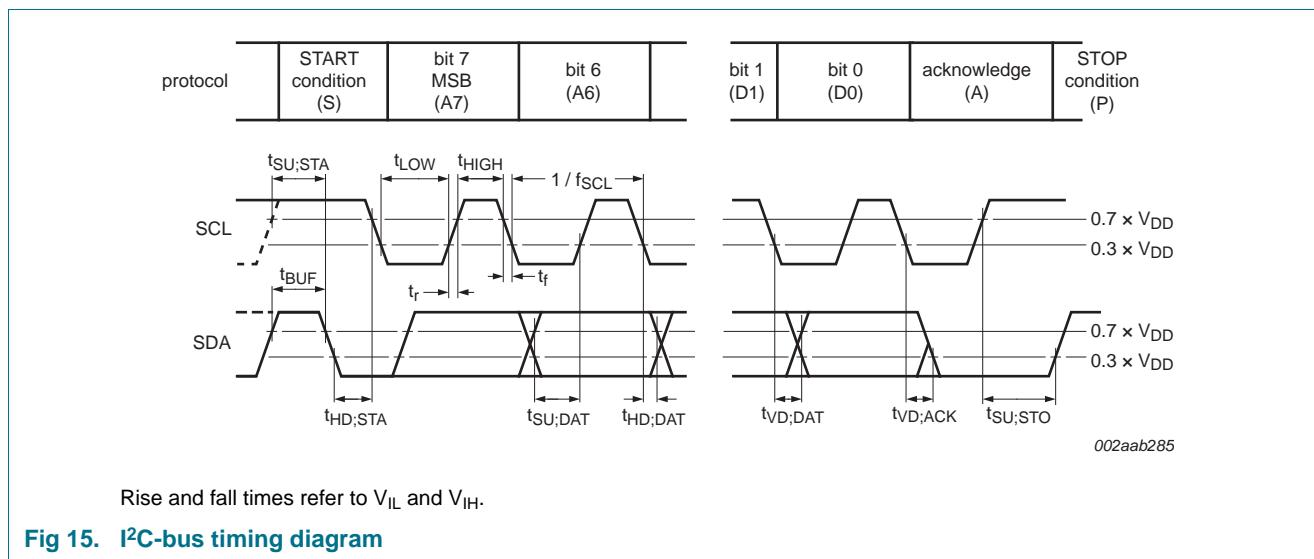
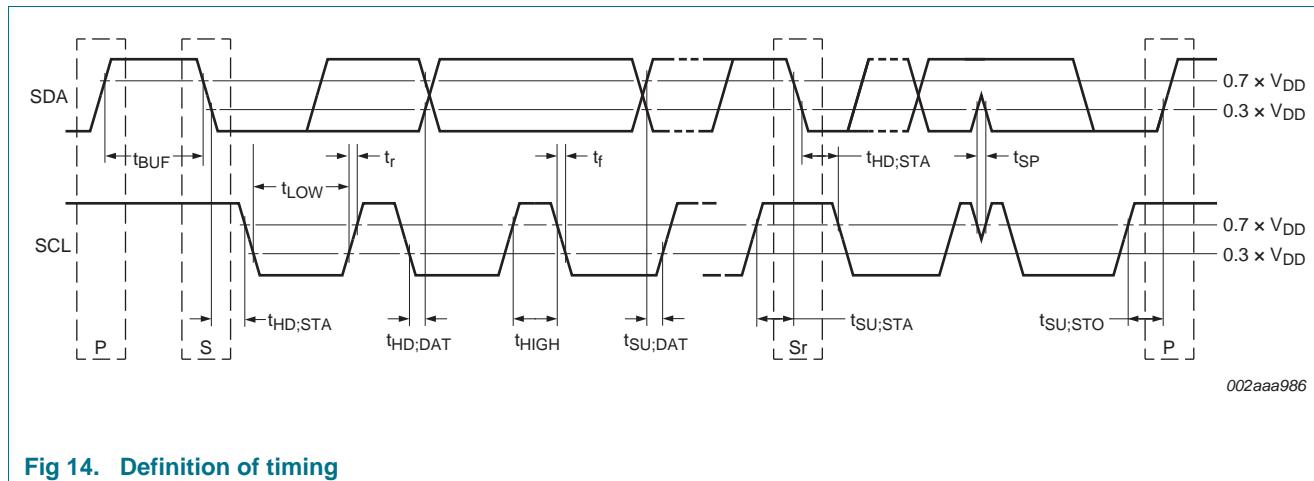
Table 12. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I ² C-bus		Fast-mode I ² C-bus		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	μs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	μs
$t_{HD;DAT}$	data hold time		0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	μs
$t_{VD;DAT}$	data valid time	[2]	300	-	50	-	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	μs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t_r	rise time of both SDA and SCL signals		-	1000	$20 + 0.1C_b$ [3]	300	ns
t_f	fall time of both SDA and SCL signals		-	300	$20 + 0.1C_b$ [3]	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
$t_{V(Q)}$	data output valid time		-	200	-	200	ns
$t_{SU(D)}$	data input set-up time		100	-	100	-	ns
$t_{H(D)}$	data input hold time		1	-	1	-	μs
Interrupt timing							
$t_{V(INT)}$	valid time on pin <u>INT</u>		-	4	-	4	μs
$t_{rst(INT)}$	reset time on pin <u>INT</u>		-	4	-	4	μs
RESET							
$t_{W(rst)}$	reset pulse width		4	-	4	-	ns
$t_{rec(rst)}$	reset recovery time		0	-	0	-	ns
t_{rst}	reset time		400	-	400	-	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for the SDA data out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line in pF.



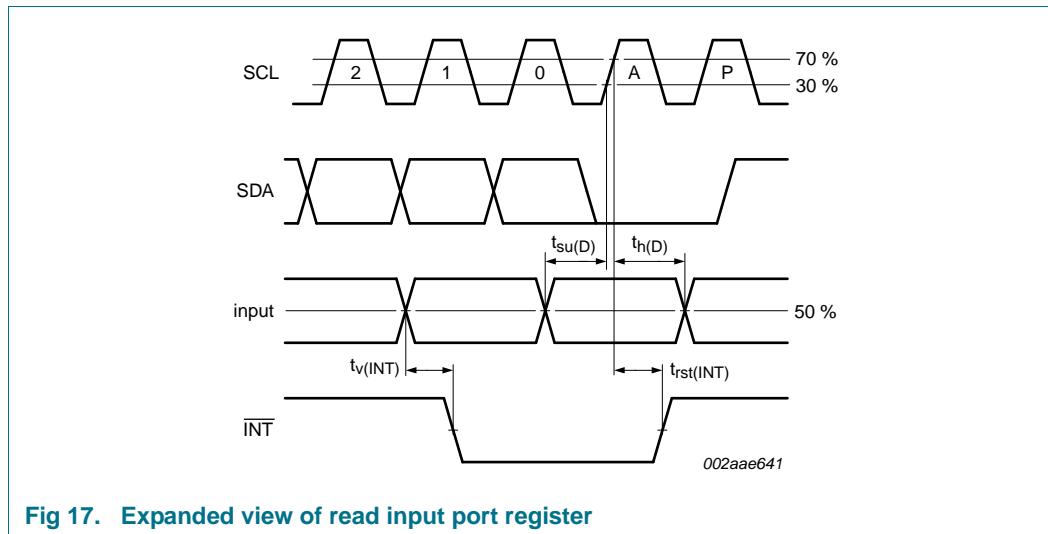


Fig 17. Expanded view of read input port register

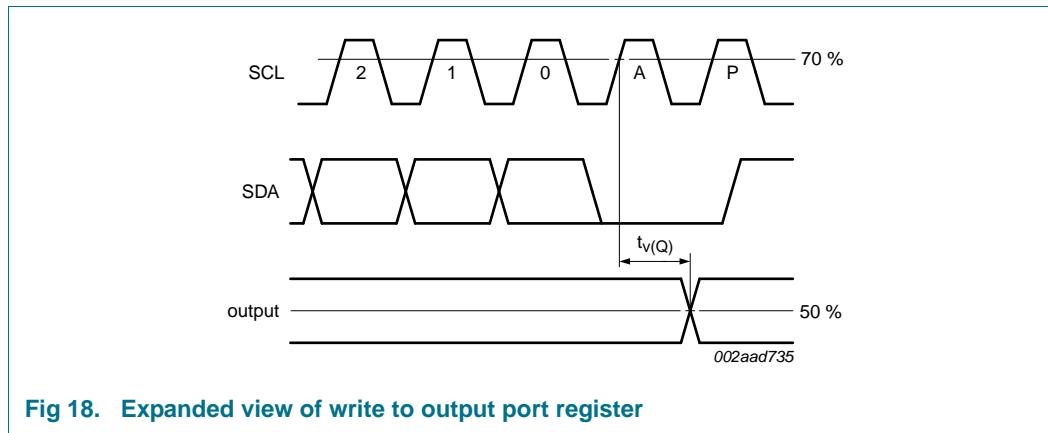


Fig 18. Expanded view of write to output port register

11. Test information

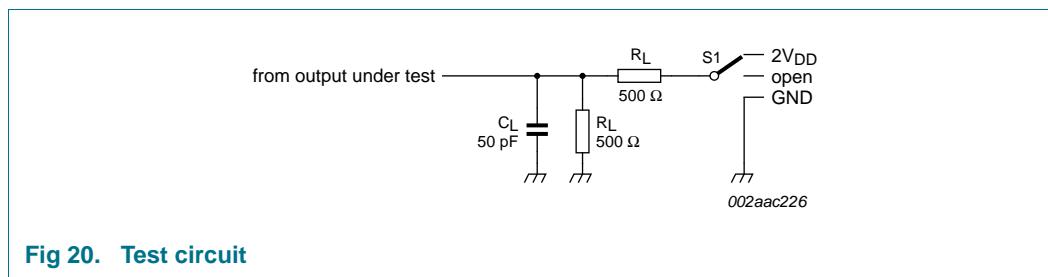
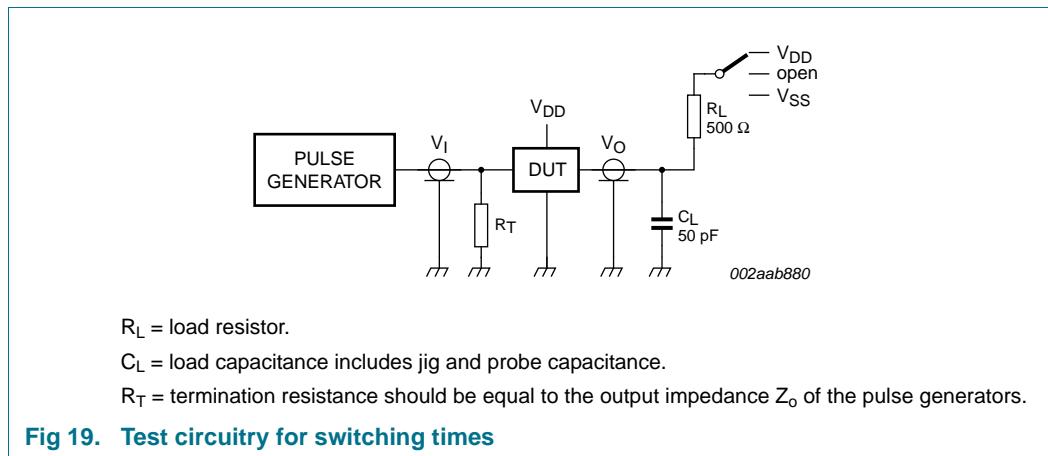


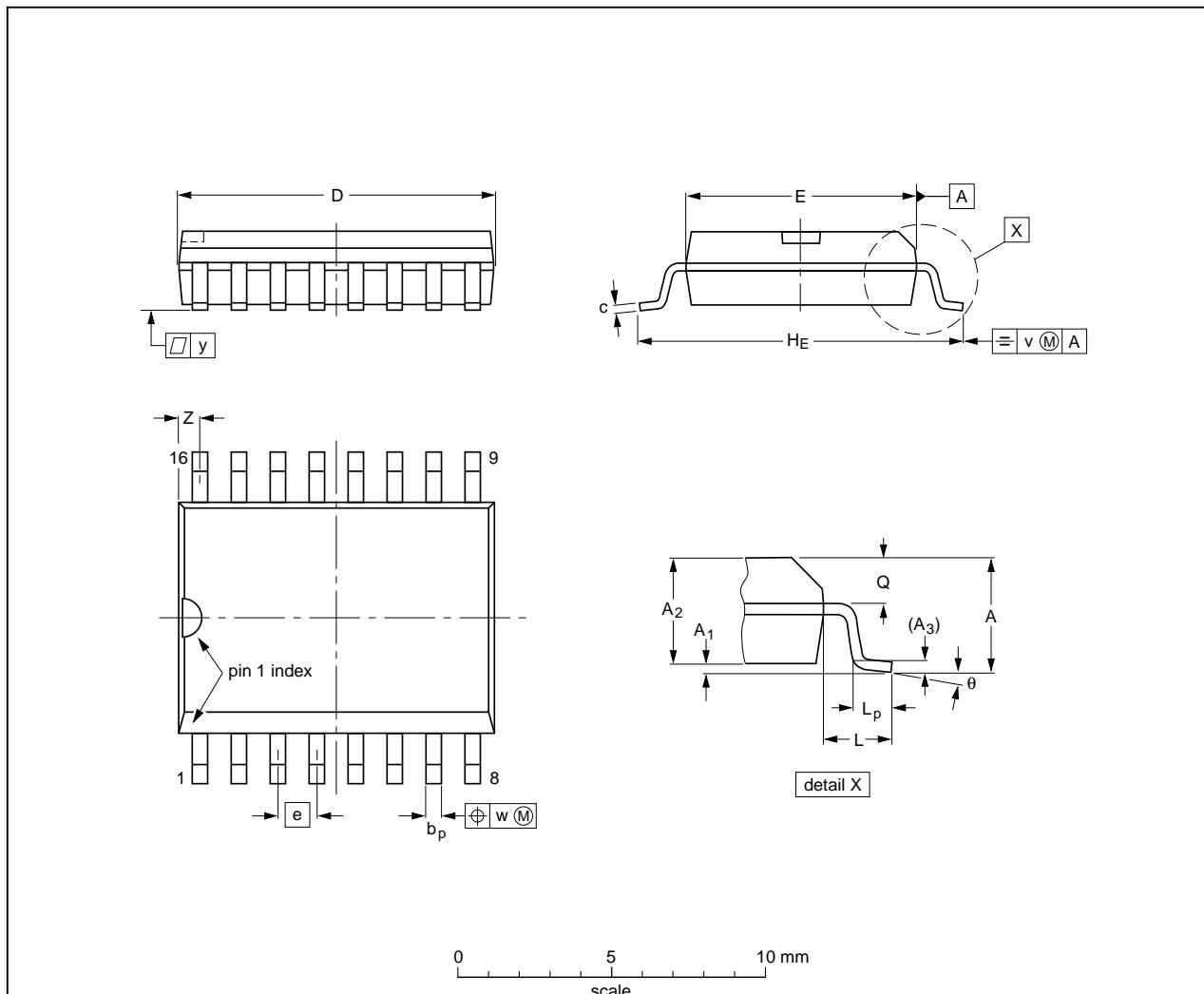
Table 13. Test data

Test	Load		Switch
	R_L	C_L	
$t_{V(Q)}$	500 Ω	50 pF	$2 \times V_{DD}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65 0.1	0.3 2.25	2.45 0.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1 0.004	0.012 0.089	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0° 0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT162-1	075E03	MS-013				99-12-27 03-02-19

Fig 21. Package outline SOT162-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

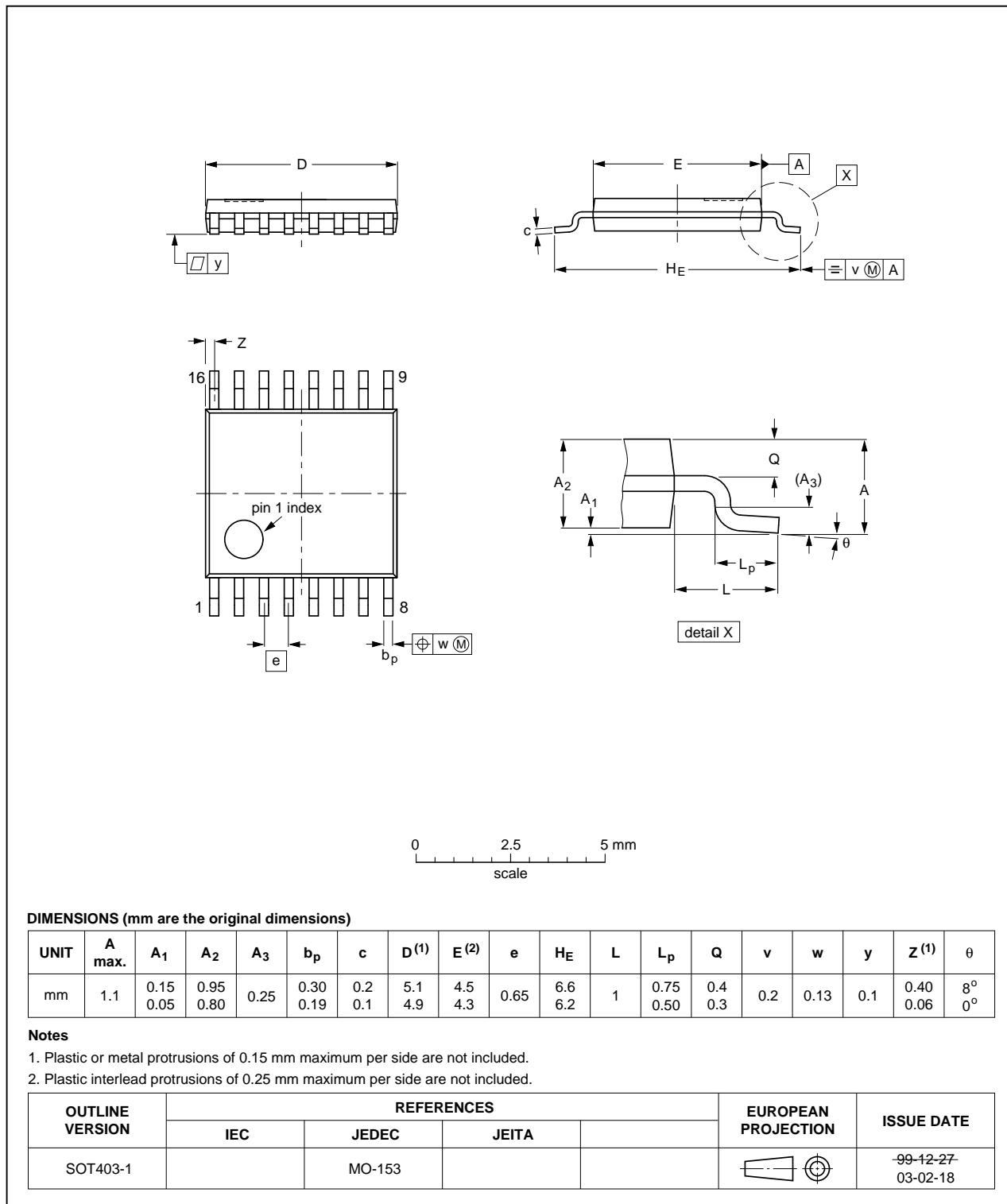


Fig 22. Package outline SOT403-1 (TSSOP16)

**HVQFN16: plastic thermal enhanced very thin quad flat package; no leads;
16 terminals; body 4 x 4 x 0.85 mm**

SOT629-1

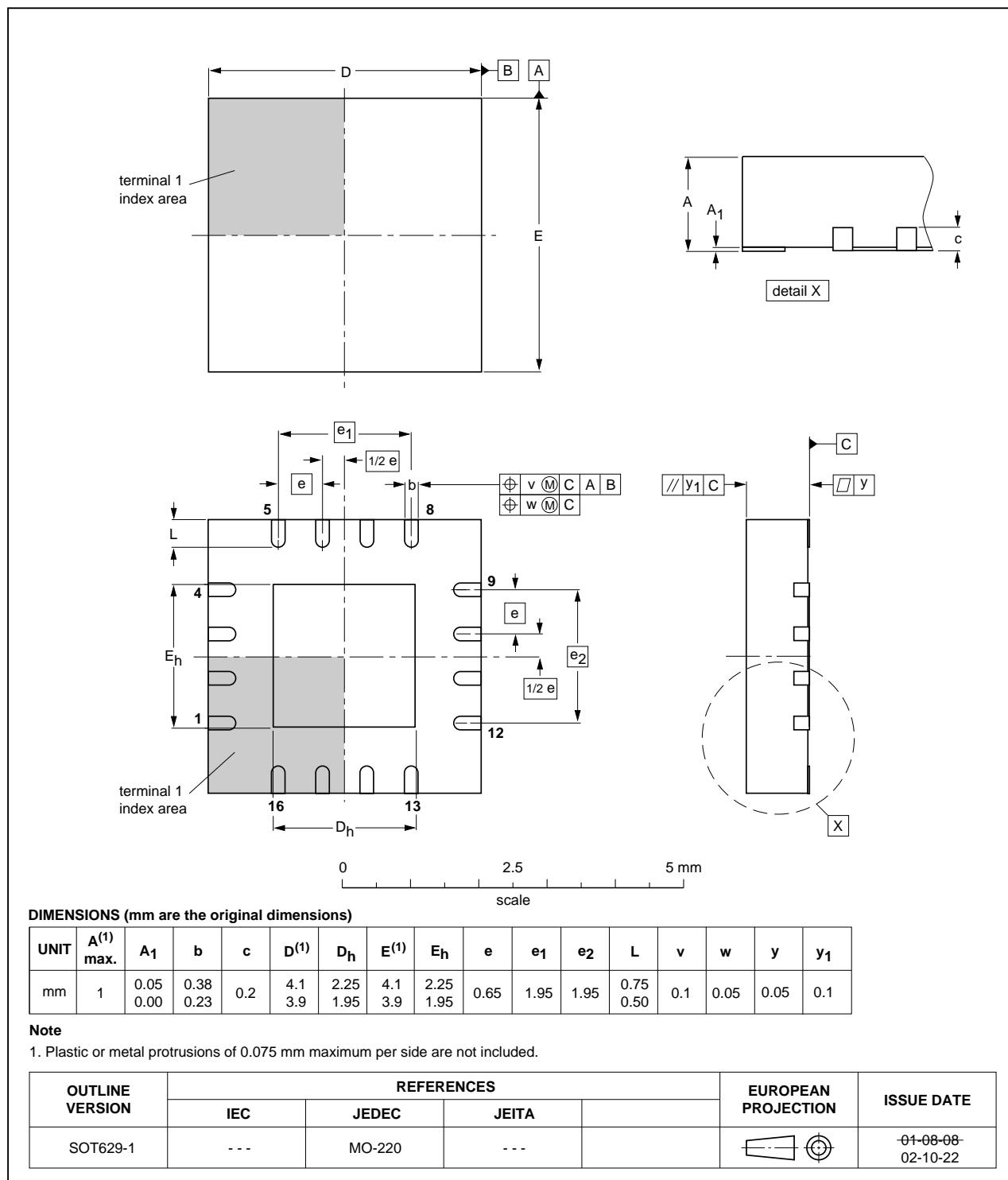


Fig 23. Package outline SOT629-1 (HVQFN16)

13. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365* “*Surface mount reflow soldering description*”.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 24](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [15](#)

Table 14. SnPb eutectic process (from J-STD-020D)

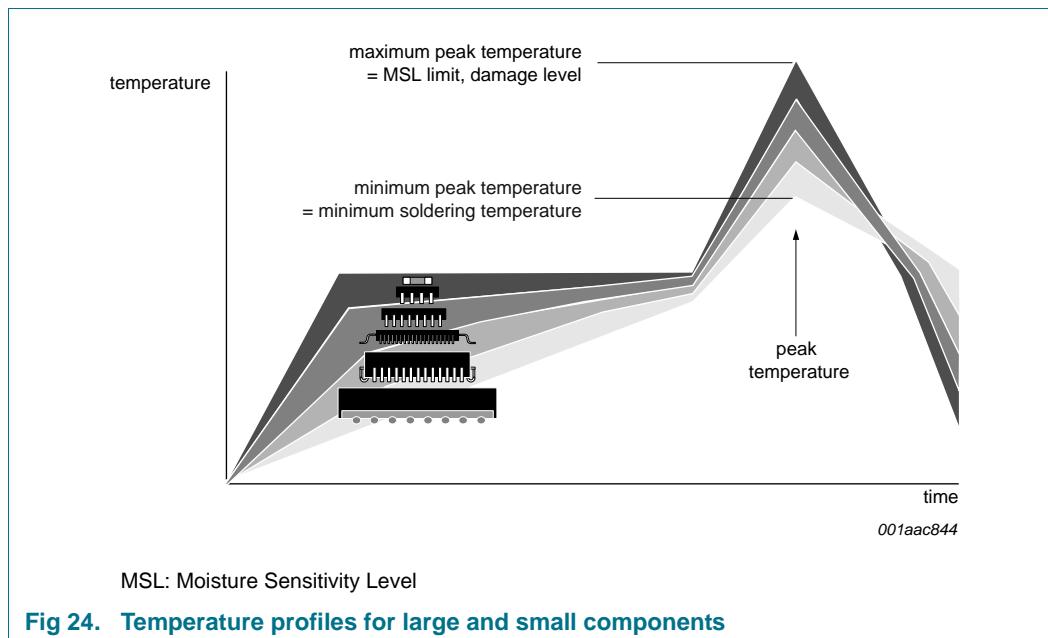
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 24](#).

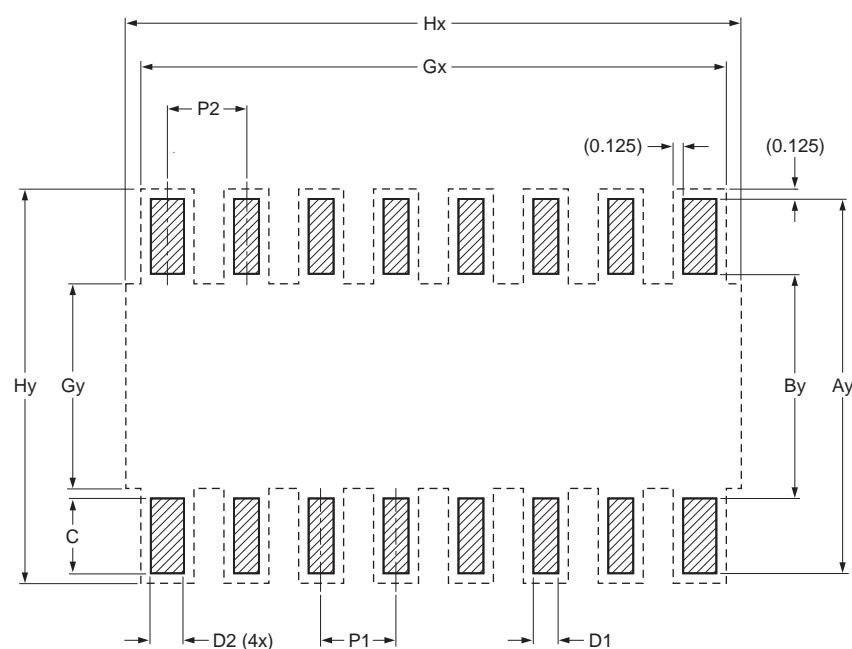


For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

15. Soldering: PCB footprints

Footprint information for reflow soldering of SO16 package

SOT162-1



solder land

----- occupied area

DIMENSIONS in mm

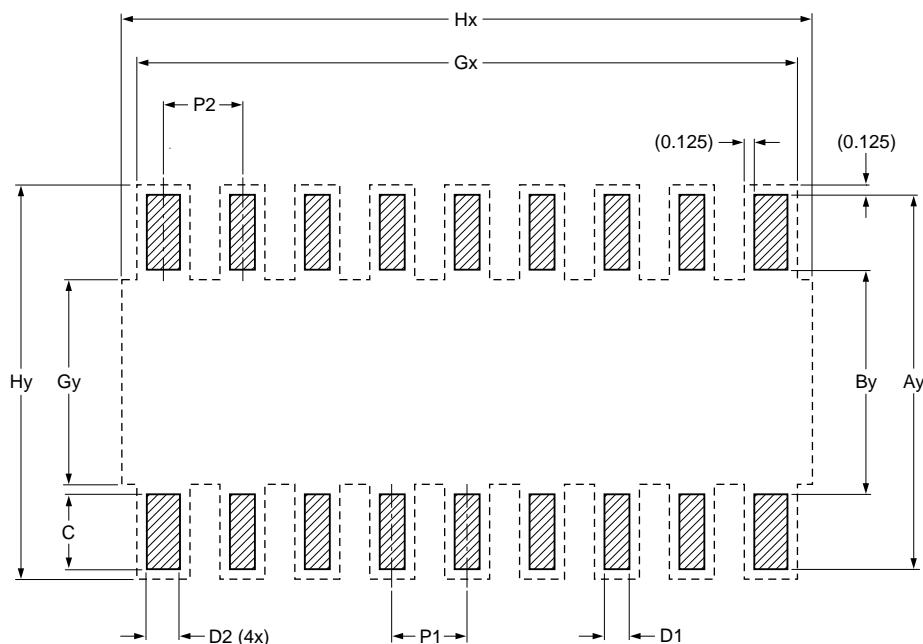
P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
1.270	1.320	11.200	6.400	2.400	0.700	0.800	10.040	8.600	11.900	11.450

sot162-1_fr

Fig 25. PCB footprint for SOT162-1 (SO16); reflow soldering

Footprint information for reflow soldering of TSSOP16 package

SOT403-1



Generic footprint pattern

Refer to the package outline drawing for actual layout

 solder land

 occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	5.600	5.300	5.800	7.450

sot403-1_fr

Fig 26. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

Footprint information for reflow soldering of HVQFN16 package

SOT629-1

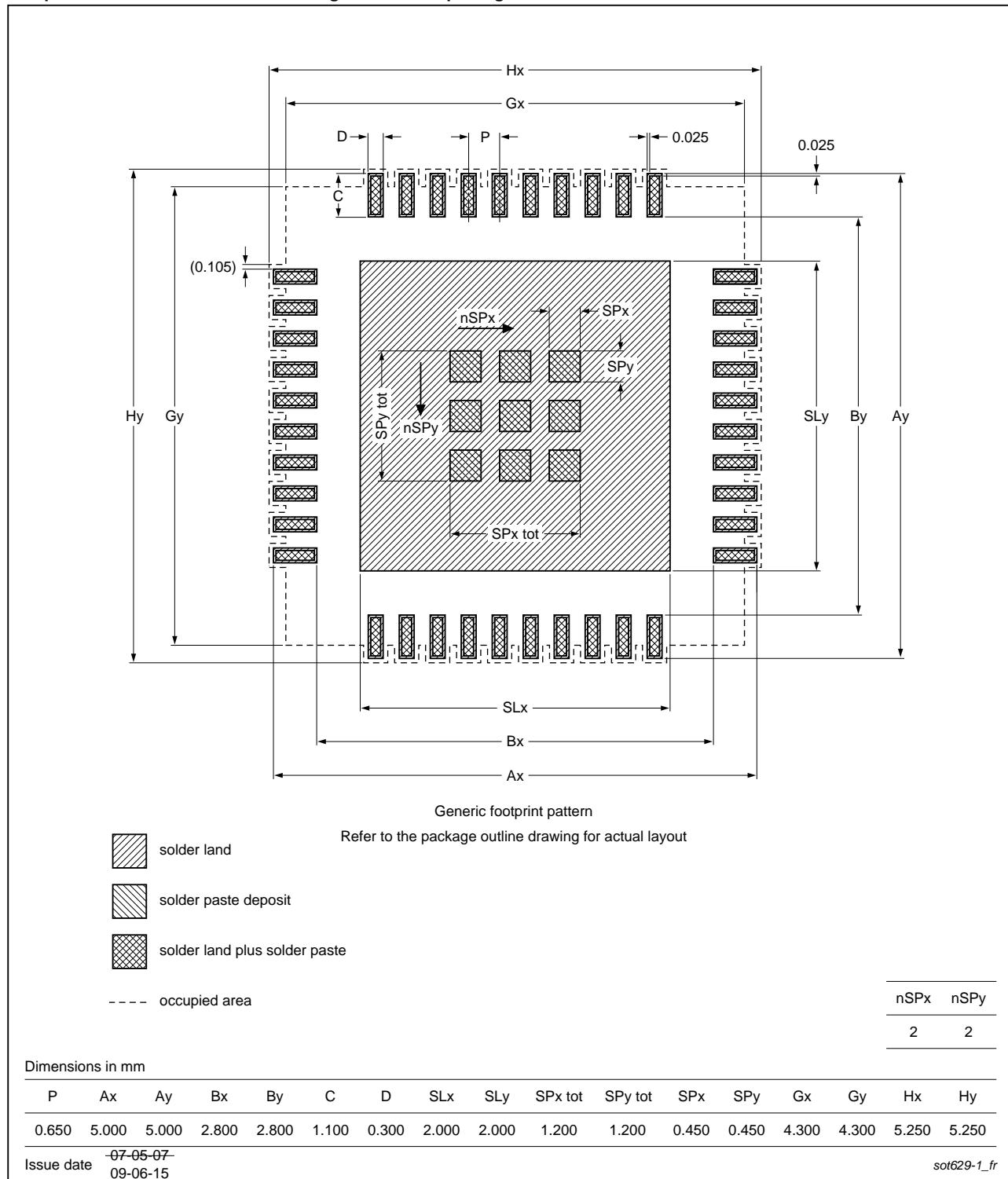


Fig 27. PCB footprint for SOT629-1 (HVQFN16); reflow soldering

16. Abbreviations

Table 16. Abbreviations

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General Purpose Input/Output
HBM	Human Body Model
I ² C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
LP	Low-Pass
POR	Power-On Reset
SMBus	System Management Bus

17. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9538 v.8	20171108	Product data sheet	201710002I	PCA9538 v.7
Modifications:	<ul style="list-style-type: none"> • Table 10 "Static characteristics for all devices except PCA9538PW/Q900", Table 11 "Static characteristics for PCA9538PW/Q900 AEC-Q100 compliant device": Corrected V_{POR} typ and max limit 			
PCA9538 v.7	20141126	Product data sheet		PCA9538 v.6
Modifications:	<ul style="list-style-type: none"> • Table 11 "Static characteristics for PCA9538PW/Q900 AEC-Q100 compliant device": updated I_{OL} and V_{OH}; changed operating power supply voltage range from "5.0 V ± 10 %" to "3.0 V to 5.5 V" for PCA9538PW/Q900 			
PCA9538 v.6	20130206	Product data sheet		PCA9538 v.5
PCA9538 v.5	20090528	Product data sheet	-	PCA9538 v.4
PCA9538 v.4	20060921	Product data sheet	-	PCA9538 v.3
PCA9538 v.3 (9397 750 14176)	20041005	Product data sheet	-	PCA9538 v.2
PCA9538 v.2 (9397 750 14049)	20040930	Objective data sheet	-	PCA9538 v.1
PCA9538 v.1 (9397 750 12881)	20040820	Objective data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I²C-bus — logo is a trademark of NXP Semiconductors N.V.

19. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

20. Contents

1	General description	1	20	Contents	34
2	Features and benefits	1			
3	Ordering information	2			
3.1	Ordering options	2			
4	Block diagram	3			
5	Pinning information	4			
5.1	Pinning	4			
5.2	Pin description	5			
6	Functional description	6			
6.1	Device address	6			
6.2	Registers	6			
6.2.1	Command byte	6			
6.2.2	Register 0 - Input Port register	6			
6.2.3	Register 1 - Output Port register	7			
6.2.4	Register 2 - Polarity Inversion register	7			
6.2.5	Register 3 - Configuration register	8			
6.3	Power-on reset	8			
6.4	RESET input	8			
6.5	Interrupt output	8			
6.6	I/O port	9			
6.7	Bus transactions	10			
7	Application design-in information	12			
7.1	Minimizing I _{DD} when the I/Os are used to control LEDs	13			
8	Limiting values	13			
9	Static characteristics	14			
10	Dynamic characteristics	17			
11	Test information	20			
12	Package outline	21			
13	Handling information	24			
14	Soldering of SMD packages	24			
14.1	Introduction to soldering	24			
14.2	Wave and reflow soldering	24			
14.3	Wave soldering	24			
14.4	Reflow soldering	25			
15	Soldering: PCB footprints	27			
16	Abbreviations	30			
17	Revision history	31			
18	Legal information	32			
18.1	Data sheet status	32			
18.2	Definitions	32			
18.3	Disclaimers	32			
18.4	Trademarks	33			
19	Contact information	33			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP](#):

[PCA9538BS,118](#) [PCA9538D,112](#) [PCA9538D,118](#) [PCA9538PW,112](#) [PCA9538PW,118](#) [PCA9538PW/Q900,118](#)